KMV11 Programmable

Communications Controller

Technical Manual

digital

Computer Special Systems

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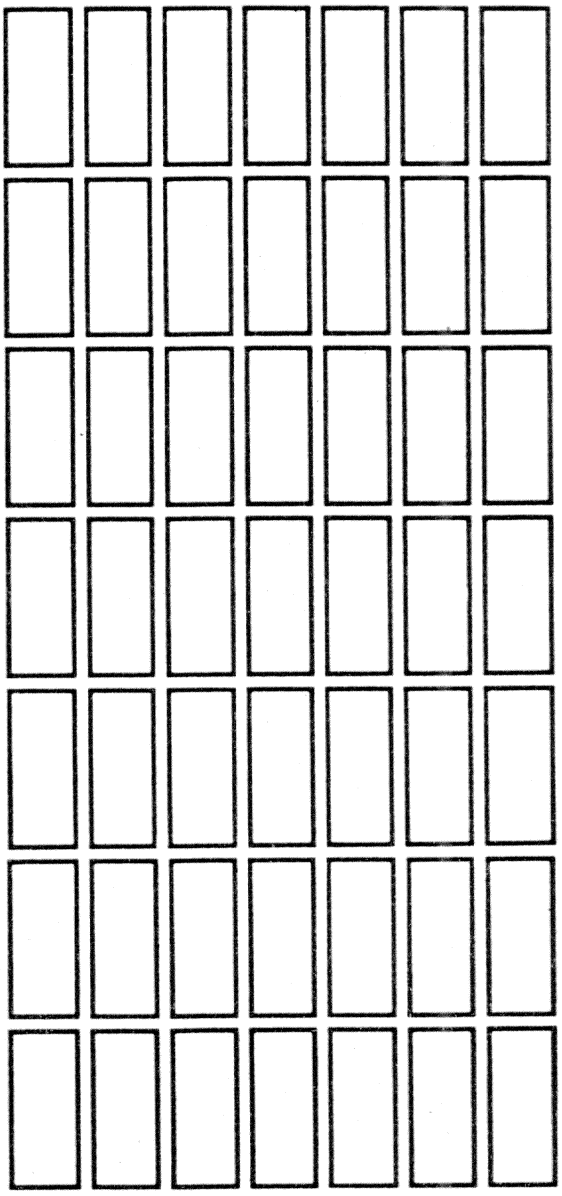

KMV11 Programmable Communications Controller

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ANNECY

EK-KMV11-TM-001

KMV11 Programmable Communications Controller Technical Manual

Course Prepared by Educational Services
of
Digital Equipment Corporation

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FIGURES

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PREFACE

This manual describes in detail the installation requirements and servicing procedures, including diagnostic support, for the KMV11 programmable communications controller.

It is organized into five chapters and one appendix.

Chapter 1 – Introduction
Chapter 2 – Installation
Chapter 3 – Programming
Chapter 4 – Functional Description
Chapter 5 – Service
Appendix A – Basic HDLC SDLC Framing Firmware

Other documents which support the KMV11 programmable communications controller are:

- KMV11 User's Guide (EK-KMV11-UG-001)
- KMV11-A printset (MP01173)
- Electronic Industries Association (EIA) specifications

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter contains an introduction to the operation of the KMV11. The term KMV11, as used in this manual, means the programmable communications controller for the Q-bus.

1.2 KMV11 GENERAL DESCRIPTION

The KMV11 is a medium speed programmable data communications interface for Q-bus-based systems.

It features:

- Direct memory access (DMA) across the Q-bus for medium-speed transmission and reception with minimum programming overhead
- A DCT11 microprocessor executing the PDP-11 base level instruction set
- A multi-protocol serial controller chip
- 4K words of EPROM with boot firmware and power up self test diagnostics
- Application mode operation for customer developed firmware using the PDP-11 instruction set
- 32K bytes of RAM space for implementation of data link protocols
- Synchronous (bit-oriented or byte-oriented) as well as asynchronous capabilities for the application firmware
- Extensive modem signal support
- Versions available with interfaces for

  RS 232-C (V28)
  RS 422-A (V11)
  RS 423-A (V10)

- On board programmable null modem clock
- Support for Q 22 (extended LSI bus)
- A compact multilayer quad height module

The KMV11-AA, KMV11-AE, or KMV11-AF unit contains a M7500 quad module and a cable assembly with an RS-232-C or RS-449-A connector. The cable between the connector of the cable assembly and the modem is not included.

Figure 1-1 is a block diagram of the main KMV11 components and the related data flow.

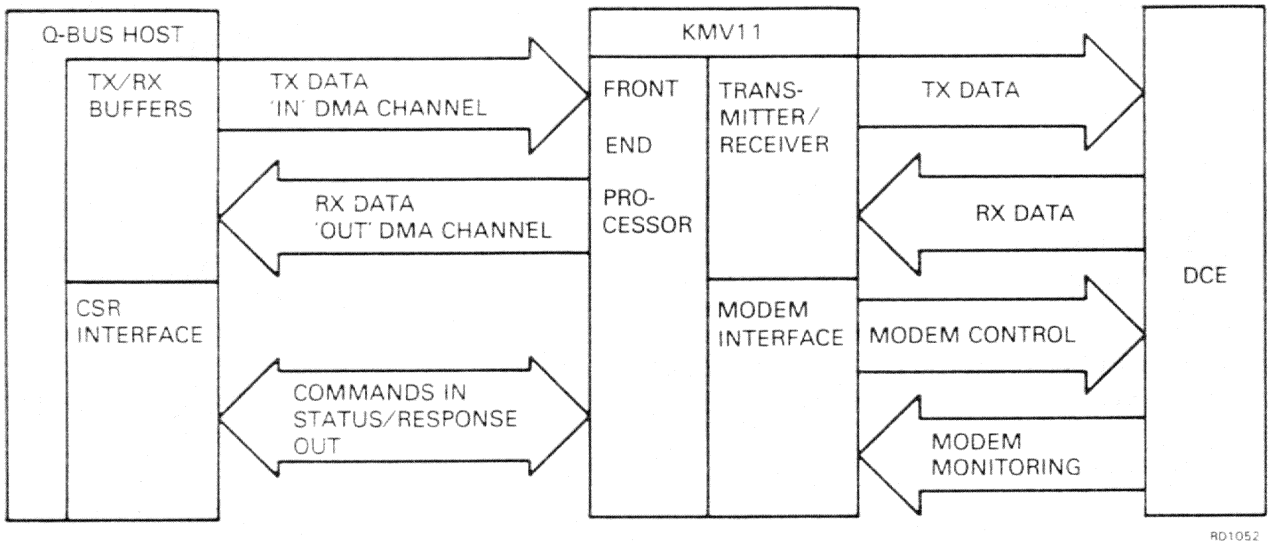


Figure 1-1 KMV11 Block Diagram

To define the direction of data transfer between the host and the KMV11 the terms 'IN' and 'OUT' are used throughout this manual in the following way:

- 'IN' applies to transfer from the host to the KMV11
- 'OUT' applies to transfer from the KMV11 to the host

The terms 'TRANSMIT' and 'RECEIVE' ('TX' and 'RX') are used for data, and timing or control information transmitted to or received from the DCE (Data Circuit-terminating Equipment), modem, null modem, or local link.

The KMV11 has four options:

1. KMV11-AA: single line with RS-232-C (V.28) interface
2. KMV11-AE: single line with RS-422-A (V.11) interface
3. KMV11-AF: single line with RS-423-A (V.10) interface
4. KMV11-B: double line with RS-232-C and RS-422-A interface

1.3 HOST/KMV11 COMMUNICATION

The host communicates with the KMV11 via eight command and status registers (CSRs) (SEL0 to SEL16 if addressed as words, or BSEL0 to BSEL17 if addressed as bytes) and a Direct Memory Access (DMA) channel. The CSRs are a group of RAM locations and may be referred to as registers, locations, or files.

NOTE

In this manual the terms BSEL and SEL will be used to indicate the CSRs. If a bit in a register needs to be defined, it will be indicated by the register name followed by a dot and the bit name or number.

Examples: BSEL1, SEL2, BSEL1.RUN or BSEL1.7 or SEL0.15

The Read-Only Memory (ROM) that is part of the KMV11 option is provided with instructions that, once it gets control after power-up or reset of the Q-bus, will prepare the KMV11 option to communicate with the host via one defined byte (BSEL1).

1.4 MODES OF OPERATION

The user may select one of four modes of operation:

1. Application mode
2. Maintenance mode 1
3. Reserved for future use
4. Maintenance mode 2

The modes of operation are selected by bits 3 and 4 of BSEL1.

1.4.1 Application Mode

In this mode the user has the capability to:

- Load instructions or data into the Random Access Memory (RAM) of the KMV11
- Read the contents of the RAM or ROM for maintenance purposes
- Start the execution of firmware at any word address.

The same byte in the CSR file is used to perform these functions as is used to select the mode of operation.

Once the firmware is loaded and the DCT11 microprocessor used by the KMV11 is given control to execute the loaded firmware, the firmware defines the other 15 bytes of the CSR file.

Byte 0 and byte 2 may cause an interrupt in the DCT11 when the host accesses these bytes for a write.

See Chapter 3 for a detailed CSR description.

Application mode makes use of the KMV11's RAM space and the versatility of the line controller chip for implementing any communications protocol.

Refer to the KMV11 User's Guide for the design and implementation of application firmware.

1.4.2 Maintenance Mode

This mode is normally used by the repair-level diagnostics. It contains two submodes:

1. Maintenance Mode 1: The KMV11 loops in a NOP sequence, to allow the host-resident diagnostic to perform data integrity tests on the CSR file.

2. Maintenance Mode 2: The KMV11 executes test routines as requested by the host-resident diagnostic using a special CSR handshaking protocol for test selection, parameter definition, and test result reporting.

1.5 GENERAL SPECIFICATIONS

The following paragraphs contain electrical and environmental specifications for all KMV11 configurations.

1.5.1 Power Requirements

+5 V @ 2.6 A
+12 V @ 0.2 A

1.5.2 Environmental Requirements

The KMV11 is designed to operate in a Class B environment as outlined in DEC standard 102.

- Operating temperature range 10°C to 40°C (50°F to 105°F)

- Relative humidity 10% to 90% with a maximum wet bulb of 28°C (82°F) and a minimum dew point of 2°C (36°F).

1.5.3 Bus Loading

Q-bus DC LOAD = 1
Q-bus AC LOAD = 3

1.5.4 Performance Specifications

The maximum line speed in application mode depends on the efficiency of the firmware. It is expected that a firmware package supporting HDLC framing only will be able to handle frames of 128 bytes to 1030 bytes without loss of information, up to speeds of 64 kbits/s in full duplex mode. Where the HDLC or the X.25 link-level protocol with the same frame limitations is implemented in the KMV the line speed that can be sustained will drop to about 19.2 kbits/s.

1.5.5 Modem Signal Supported

Table 1-1 contains a list of all the modem signals that are supported by the KMV11.

Table 1-1 List of Supported Modem Signals

CCITT	RS449	RS232	DIN 66020	DEC STD 52	REMARK
101	(none)	AA	E1	PRT GND	
102	SG	AB	E2	SIG GND	
103	SD	BA	D1	TxD	D
104	RD	BB	D2	RxD	D
105	RS	CA	S2	RTS	D
106	CS	CB	M2	CTS	I,D
107	DM	CC	M1	DSR	IA,D
108/2	TR	CD	S1.2	DTR	D
109	RR	CF	MF	CD	I
111	SR	CH	S4	DSRS	A
112	SI	CI	(none)	SPDMI	A
113	TT	DA	T1	TxClock(DTE)	D
114	ST	DB	T2	TxClock(DCE)	D
115	RT	DD	T4	RxClock(DCE)	D
140	RL	(none)	PS2	Rem LPBK	A
141	LL	(none)	PS3	Local LP REQ	A
142	TM	(none)	PM1	Test Indicator	A
125	IC	CE	M3	RI	A
(none)	IS	(none)	(none)	(none)	*

SG = Signal Ground
SD = Send Data
RD = Receive Data
RS = Request to Send
CS = Clear to Send
DM = Data Mode
TR = Terminal Ready
RR = Receiver Ready
SR = Signaling Rate selector
SI = Signaling Indicator
TT = Terminal Timing
ST = Send Timing
RT = Receive Timing
RL = Remote Loopback
LL = Local Loopback
TM = Test Mode
IC = Incoming Call
IS = In Service (terminal)

COMMENTS

A = Available on KMV11-A only

D = Transmitted class 1 circuit available as either RS-422 or RS-423 signal

I = Interrupts from both KMV11-B channels

IA = Causes interrupts (KMV11-A only)

* = There is no approved CCITT equivalent circuit (it may become CCITT 135)

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides all the information necessary for installing and testing the KMV11. A checklist, which can be used to verify the installation process, is also included.

2.2 UNPACKING AND CHECKOUT

The KMV11 is packed according to commercial packing practices. When unpacking, remove all packing material and check the equipment against the shipping list (Table 2-1 contains a list of items shipped with each configuration). Examine all parts and carefully check the M7500 module for obvious signs of damage. Check the received components against the shipping list. Where necessary, report damages or shortages to the shipper and inform the DIGITAL representative.

Table 2-1 KMV11 Packing Lists

KMV11-A Suboption Packing List

Part Number	Description
M7500	Line unit module
H3255	Module test connector
EK-KMV11-TM-001	KMV11 Technical Manual
EK-KMV11-UG-001	KMV11 User's Guide
MP01173	Customer print set

KMV11-AA RS-232 Option Packing List

Part Number	Description
KMV11-A	Basic suboption
BC55H	RS-232 cable assembly
H325	Cable loopback connector RS-232

KMV11-AE RS-422 Option Packing List

Part Number	Description
KMV11-A	Basic suboption
BC55U	RS-422 cable assembly
H3251	Cable loopback connector RS-449

Table 2-1 KMV11 Packing Lists (Cont)

KMV11-AF RS-423 Option Packing List

Part Number	Description
KMV11-A	Basic suboption
BC55P	RS-423 cable assembly
H3251	Cable loopback connector RS-449

The diagnostics for the KMV11 are released through the Software Distribution Center (SDC). The following options can be ordered separately by self-maintenance customers:

- ZJ-360-RZ diagnostic documentation kit
- ZJ-360-FR diagnostic fiche kit
- ZJ-360-PY diagnostic RX01 kit

2.3 INSTALLATION PHASES

Installation of the KMV11 should be done in four phases:

1. Phase I – Preinstallation

   Verify KMV11 requirements with respect to power and location within the system.

2. Phase II – M7500 installation

   Configure the M7500 module for the customer application.
   Install the M7500 module and verify its operation, using the appropriate diagnostics.

3. Phase III – Modem cable assembly installation

   Install the cable, lay the cable, and verify cable and module via the appropriate diagnostics.

4. Phase IV – KMV11 system testing

   Verify the complete KMV11 subsystem operation with the functional diagnostics and system exercise programs.

2.4 PREINSTALLATION CONSIDERATIONS

The preinstallation phase checks that the host system is capable of receiving the KMV11 option.

2.4.1 Mounting Space

The KMV11 needs one quad slot with the Q-bus connected to slots A and B. The Q-bus signals may also be connected to slots C and D but will not be used there. BDMG and BIAK lines are connected through on the C and D module connector.

2.4.2 Power Requirement

+5 V @ 2.6 A
+12 V @ 0.2 A

2.4.3 Modem Cable Assembly Requirements

The BC55H, BC55U, and BC55P modem cable assemblies are designed to be mounted on the H349 bulkhead connector panel. This bulkhead panel is normally provided with PDP-11/23+ or PDP-11/23B systems.

In conditions where the H349 is not available, the BC55H, BC55U, and BC55P modem cable assemblies may be screwed onto the vertical cabinet mounting rails, normally drilled at EIA spacings.

2.5 M7500 INSTALLATION

2.5.1 Voltage Check

Before installing the M7500 module:

- Verify that the +5 V supply voltage at backplane pin AA2 is between +4.85 V and +5.15 V
- Verify that the +12 V supply voltage at backplane pin AD2 is between +11.64 V and +12.36V.

2.5.2 Switch Settings

Check that the switch settings and jumper configurations meet the system and customer requirements.

2.5.2.1 Address Switches:

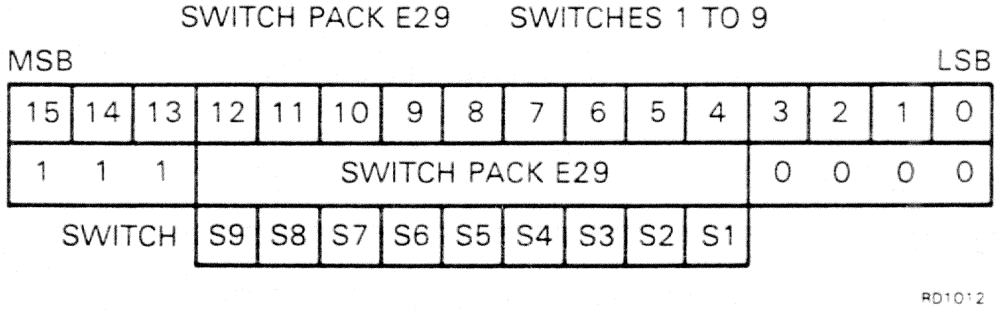


Figure 2-1 Address Switch Register Mapping

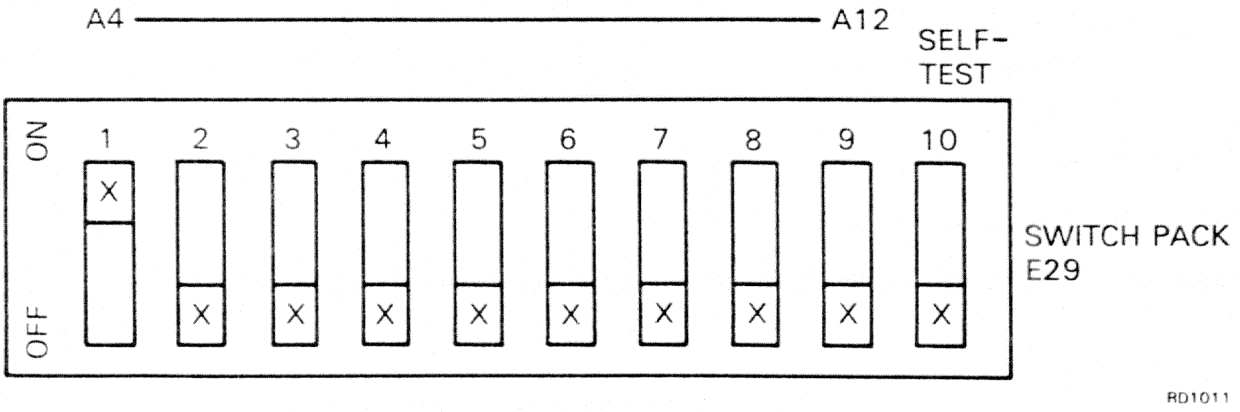


Figure 2-2 Address Switch Setting Example: 760020_8

An 'on' switch matches an asserted address bit.

The KMV11 address is to be assigned within the floating address space at rank 31. It occupies eight CSR addresses (for example, 760020_8 to 760036_8).

NOTE

The term 'rank' has no hardware significance. It denotes the position of the address in a table used by auto-configuration programs.

2.5.2.2 Vector Switches

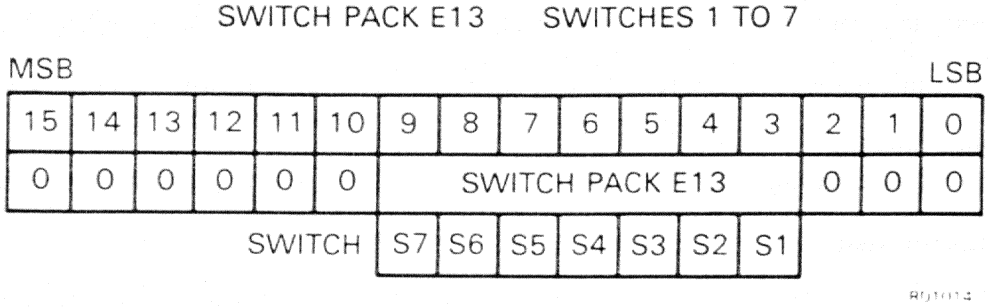


Figure 2-3 Vector Switch Register Mapping

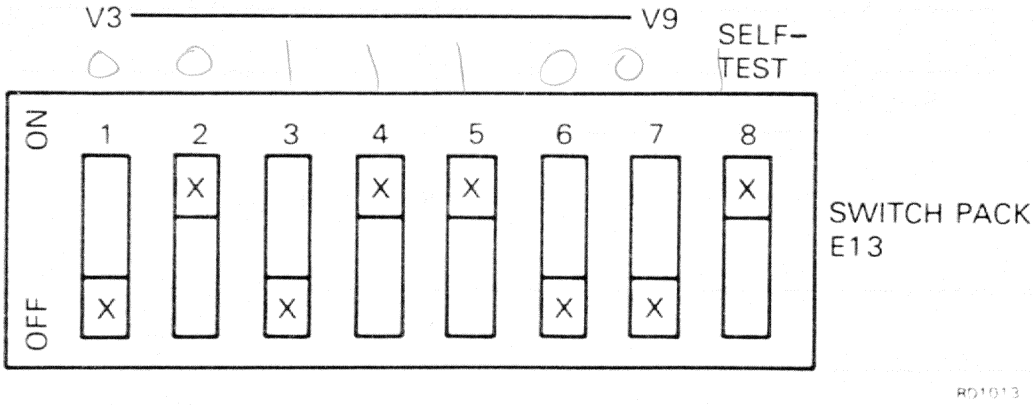


Figure 2-4 Vector Switch Setting Example: 320

An 'on' switch gives an asserted vector bit.

The KMV11 vector is to be assigned within the floating vector space at rank 54.

NOTE

The term 'rank' has no hardware significance. It denotes the position of the address in a table used by auto-configuration programs.

BENJY = 00111101 = 740

FRANK1 = 00111001 = 340

CSR = 760020 (Both)

The other two switches on E13 and E29 affect self-test operation in the following way:

E13 SW8	E29 SW10		Self-Test Operation
ON	ON	=	Self-test disabled
ON	OFF	=	Self-test enabled (start via CSR command or at power up, for one pass)
OFF	OFF	=	Self-test manual start for continuous loop
OFF	ON	=	Extended self-test start for continuous loop

2.5.3 Jumper Configurations

1. Extended address jumpers

   Links W3, W4, and W7 to W10 are normally installed to allow extended addressing (BDAL 16 to 21). They should only be removed when the extended address lines (SPARE lines on older LSI configurations) are in contention with other signals.

2. BDMG and BIAK jumpers

   Links W11 and W13 are normally installed to provide BDMG and BIAK continuity in the C and D slots. They should only be removed when the corresponding backplane pins are used for other purposes.

3. Factory test jumpers

   Links W2 and W12 are only removed during factory module testing. They must be installed for normal KMV11 operation.

The other switches and jumpers depend on the modem interface characteristics as shown in the following notes and in Figure 2-5.

All other combinations of switches 1 to 8 are illegal.

E85 switch 9 OFF isolates pin 29 of the connector assemblies (CCITT 107). It should normally be ON, and only OFF when a modem connects a different signal to this pin.

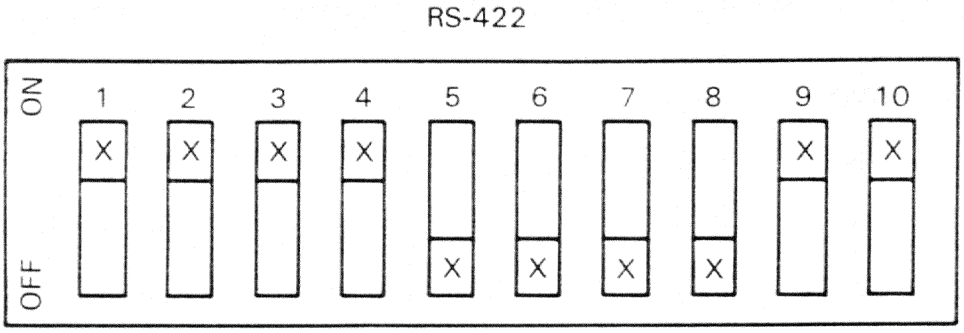
E85 switch 10 OFF isolates pin 2 of the connector assemblies (CCITT 112). It should normally be ON, and only OFF when a modem connects a different signal to this pin.

Jumper W15 forces modem signal CCITT 109 (Carrier Detect) permanently to the active (1) state . This link is normally not installed.

Jumper W14 installed connects modem signal Terminal In Service to connector assemblies pin 28. This signal is not used by most modems, but is needed for loopback testing using the H3251 loopback connector. It should therefore only be removed in situations where its presence causes a problem with the modem.

KMV11-AE, RS-422

SWITCH	
1	ON
2	ON
3	ON
4	ON
5	OFF
6	OFF
7	OFF
8	OFF



KMV11-AA/AF, RS-423, RS-232-C

SWITCH	
1	OFF
2	OFF
3	OFF
4	OFF
5	ON
6	ON
7	ON
8	ON

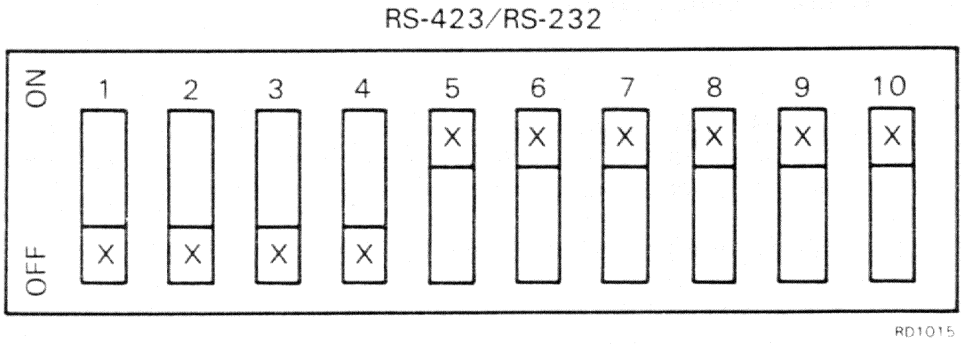


Figure 2-5 RS-422 Versus RS-423 (RS-232) on Switch Pack E85.

2.5.4 Standard Switch Setting and Jumper Configuration for KMV11-A

Table 2-2 KMV11-A Switch Register and Jumper Settings

E29	Switch	1	ON	Address = 776020
		2	OFF	
		3	OFF	
		4	OFF	
		5	OFF	
		6	OFF	
		7	OFF	
		8	OFF	
		9	OFF	
E13	Switch	1	OFF	Vector = 320
		2	ON	
		3	OFF	
		4	ON	
		5	ON	
		6	OFF	
		7	OFF	
E29	Switch	10	OFF	Self-test enabled
E13	Switch	8	ON	Runs for one pass at power-up or via CSR command

Table 2-2 KMV11-A Switch Register and Jumper Settings (Cont)

W3	IN	Extended address bits 16 to 21 connected to Q-Bus
W4	IN	
W7	IN	
W8	IN	
W9	IN	
W10	IN	
W6	OUT	Not used
W11	IN	BDMG and BIAK continuity made in slots C and D
W13	IN	
W2	IN	DMA clock enabled
W12	IN	Microprocessor clock enabled

Table 2-3 KMV11-AA/AF Additional Switch and Jumper Settings

E85	Switch	1	OFF	RS-423-A/RS-232-C selected
		2	OFF	
		3	OFF	
		4	OFF	
		5	ON	
		6	ON	
		7	ON	
		8	ON	
		9	ON	CCITT 107, connected
		10	ON	CCITT 112, connected
W15	OUT			CCITT 109 (Carrier Detect) follows input
W14	IN			Terminal In Service connected.

Table 2-4 KMV11-AE Additional Switch and Jumper Settings

E85	Switch	1	ON	RS-422-A selected
		2	ON	
		3	ON	
		4	ON	
		5	OFF	
		6	OFF	
		7	OFF	
		8	OFF	
		9	ON	CCITT 107, connected
		10	ON	CCITT 112, connected
W15	OUT			CCITT 109 (Carrier Detect) follows input
W14	IN			Terminal In Service connected.

2.5.5 M7500 Insertion

When you have checked supply voltages and configured the M7500 module, you may insert the module in the selected Q-bus slot. Make sure that system power is off while inserting the module.

After insertion of the module, power up and check that the supply voltages have stayed within acceptable limits.

Perform the following quick test on the module:

1. Deposit 0 into the base address
2. Examine the base address; it should be 0
3. Deposit 44000_8 into the base address
4. Examine the base address; it should be 4000_8.

If the above test does not give the expected result, the installation must not be continued, the M7500 module must be either replaced or repaired.

2.6 MODEM CABLE ASSEMBLY INSTALLATION.

At this step the connector assemblies should be installed.

2.6.1 BC55H/BC55U/BC55P Considerations

In order to install modem cable assemblies correctly, the H349 bulkhead connector panel with free slots in J12, J13, J14, or J15 should be available. Otherwise the cable assembly may be screwed directly to the vertical cabinet mounting rails, selecting a proper location where the EIA spaced holes of the mounting rail match the holes of the connector assembly.

Before installing the BC55H, BC55U, or BC55P, verify and configure the appropriate modem line jumpers.

Refer to Table 2-5 for the configuration of the BC55H, BC55U, or BC55P.

Table 2-5 BC55H, BC55U, and BC55P Jumper Settings

J2 PIN	JUMPER	RS-232-C	BELL 103J	BELL 208B	BELL 209	DATEL 200	DATEL 600	DATEL 1400	DATEL 4800	CCITT V.21	CCITT V.23	CCITT V.26B	CCITT V.27T	ISO2110-1972	ISO2110-2	EIA RS-232-C	EIA RS-449	CCITT V.24
																FUTURE D		
																X 21BIS		
																X 20BIS		
23	W1	IN				IN	IN	IN		IN	IN	IN	IN	IN		CH	SR	111
21	W2	IN		IN												CG	SQ	110
11	W3				IN				IN				IN				SF	126
23	W4															CI	SF	112
16	W5	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SBB	SRD	119
14	W6	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SBA	SSD	118
12	W7	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SCF	SRR	122
21	W8								IN					IN	IN		RL	140
4	W9	IN		IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	CA	RS	105
15	W10	IN		IN	IN		IN	IN		IN	IN	IN	IN	IN		DB	ST	114
17	W11	IN		IN	IN		IN	IN		IN	IN	IN	IN	IN		DD	RT	115
18	W12								IN					IN	IN		LL	141
19	W13	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SCA	SRS	121
	W14	NOT NORMALLY INSTALLED																
25	W15								IN					IN	IN		TM	142
24	W16	IN		IN	IN			IN			IN	IN		IN	IN	DA	TT	113
25	W17						IN										SB	117
24	W18						IN										SS	116
13	W19	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SCB	SCS	121
25	W20															MAKE BUSY		
7	W21	IN	IN	IN	IN	IN	IN	IN					IN			AA		101
2																BA	SD	103
3																BB	RD	104
5																CB	CS	106
6																CC	DM	107
7																AB	SG	102
8																CF	RR	109
20																CD	TR	108
22																CE	IC	125

MK-2725

2.6.2 BC55H, BC55U, and BC55P Installation on the H349 Panel

When the connector panel is configured, it may be mounted onto the H349 bulkhead panel into any available slot from J13 to J15. Refer to Figure 2-6 for the correct panel mounting.

Connect the BC08-S flat cable between the connector panel and the M7500 module, providing a point-to-point connection. To do this, one connector end should have the ribbed side up, the other end the smooth side up. Complete the physical installation by neatly dressing and attaching the cable to the H349.

Refer to Paragraph 2.7 for the KMV11 checkout.

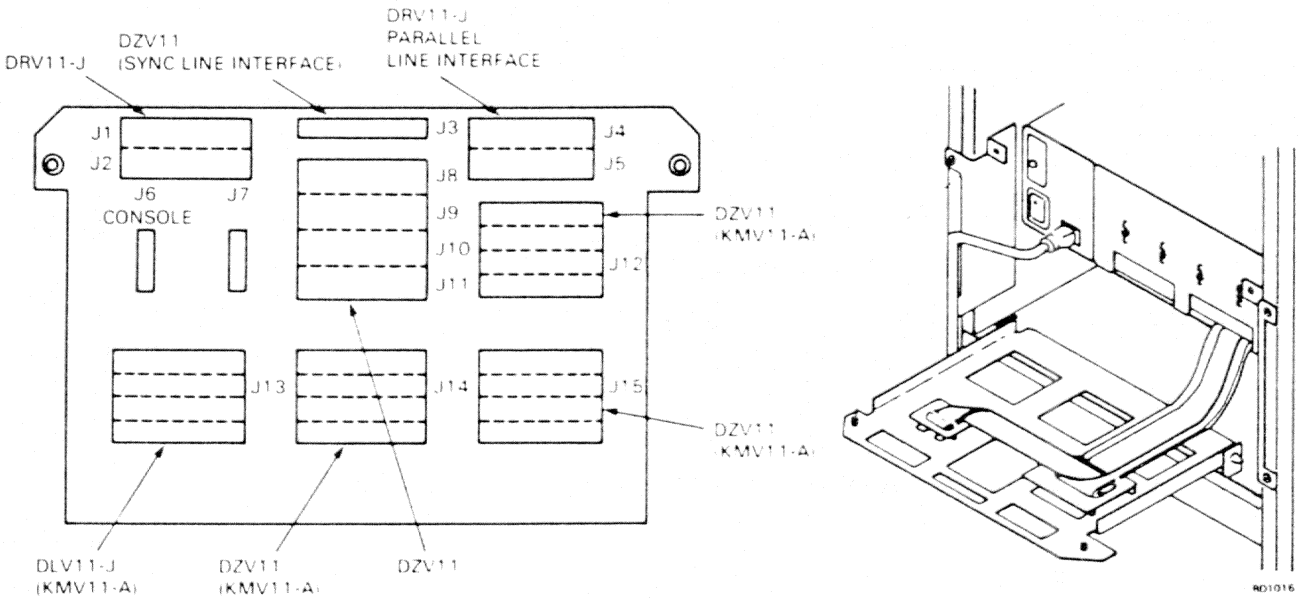


Figure 2-6 Connector Panel Installation

2.6.3 BC55H, BC55U, and BC55P Installation Without H349 Panel

When you have selected the appropriate mounting space and checked the jumper configuration, you may mount the connector panel to the cabinet frame, tightening the screws hard to provide a good shield to ground continuity.

Then connect the BC08-S flat cable between the connector panel and the M7500 module, providing a point-to-point connection.

2.7 KMV11 SYSTEM TESTING

When the physical installation of the KMV11 has been completed, it should be tested by means of the diagnostic programs.

2.7.1 Functional Diagnostic Testing.

The functional diagnostic VKMC exercises the KMV11 in a standalone mode. Make sure, before starting the diagnostic, that either the H3251 or H325 cable test connector is fitted to the cinch connector at the cable assembly panel, or the H3255 module test connector is fitted on the M7500 module.

Allow the diagnostic to run for at least five error-free passes.

If errors occur, refer to Chapter 5 to perform corrective maintenance.

2.7.2 DEC-X11 System Exerciser

The DEC-X11 system exerciser, CXKMD, will run the host, peripherals, and KMV11 in a worst-case environment similar to a user's operating system. Any error message calls for corrective maintenance to be performed. Refer to Chapter 5 for corrective maintenance.

2.7.3 Final Cable Connections

After the successful completion of diagnostic testing, remove all test connectors and install the modem or null modem cables as needed by the application.

Standard modem cables:

RS-232-C	BC05D-25	7.5 m (25 ft) Connects the modem to a 25-pin cinch connector on a BC55H cable assembly
RS-423-A	BC55D-33	10 m (33 ft) Connects the modem to a 37-pin cinch connector on a BC55P cable assembly
RS-422-A	BC55D-33	10 m (33 ft) Connects the modem to a 37-pin cinch connector on a BC55U cable assembly

2.8 KMV11 INSTALLATION CHECKOFF LIST

Date Completed

PHASE I PREINSTALLATION

1. Mounting space (2.4.1)
2. Power requirements (2.4.2)
3. Modem cable requirements (2.4.3)

PHASE II M7500 INSTALLATION

1. Unpack, check for full shipment (2.2)
2. Backplane voltages (2.5.1)
3. Switches configured (2.5.2)
   (2.5.4)
4. Jumpers configured (2.5.3)
   (2.5.4)
5. M7500 installed (2.5.5)
6. Backplane voltages (2.5.1)
7. M7500 quick check (2.5.5)

PHASE III MODEM CABLE ASSEMBLY INSTALLATION

1. H349 or mounting space on cabinet frame available for BC55H/U/P (2.6.1)
2. BC55H/U/P configured (2.6.1)
3. BC55H/U/P installed (2.6.2)
   (2.6.3)
4. BC08-S installed and connected (2.6.2)
   (2.6.3)

PHASE IV KMV11-A SYSTEM TESTING

1. Test connectors fitted (2.7.1)
2. Functional diagnostics (2.7.1)
3. DECX-11 exerciser (2.7.2)
4. Test connectors removed, modem cables installed (2.7.3)

CHAPTER 3
PROGRAMMING

3.1 SCOPE

This chapter is intended to give an overview of programming the KMV11.

Details and reference material to allow actual programming are available in the KMV11 User's Guide.

3.2 INTRODUCTION

As well as the maintenance modes, used by diagnostics, an application mode is available with the KMV11.

The mode selection is programmable at initialization of the KMV11.

Application mode has the following characteristics:

- Firmware to be loaded into RAM
- Eight Control and Status Register (CSR) words available
- One byte of CSR predefined
- Two bytes may generate a DCT11 interrupt when written to by the host
- 32K bytes of RAM for program and buffer storage
- Programmable real-time and line clock
- Programmable Universal Synchronous/Asynchronous Receiver/Transmitter (PUSART)
- Programmable modem control signals

To make full use of the application mode an RSX driver and firmware code package is available. The firmware code supports basic HDLC framing with full modem control. This firmware package is also used by the functional diagnostic program and has the following characteristics:

- Four Control and Status Registers (CSRs) used
- Four CSRs defined
- HDLC physical layer protocol
- Modem handshaking for full-duplex operation

3.3 CONTROL AND STATUS REGISTER DESCRIPTION

Communication of control and status information between the host and the KMV11 uses 8 words (16 bytes) of Control and Status Registers (CSRs). These have the addresses from 76xx00 to 76xx17. These device addresses are subsequently referred to as 'byte select 0 to 17' (BSEL0 to BSEL17) for indicating individual bytes, and as 'select 0 to 16' (SEL0 to SEL16) for indicating individual words.

BSEL1 is defined by the KMV11's root firmware routines for the following functions:

- Diagnostic firmware self-test execution
- Application mode control
- Special maintenance functions

The root firmware always takes control after power-up, restart or master clear (MCLR). The contents of the RAM memory is only preserved after an MCLR. In addition, the execution of an HLT instruction in the application firmware will transfer control to the restart entry point in the root firmware. In application mode function bits are defined to load, unload, and run application firmware.

Before the KMV11 is able to execute the application firmware, firmware code must be loaded into the RAM of the KMV11.

In order to recover the contents of the RAM for system analysis or diagnostic purposes, an unload function is supported by the root firmware.

To start the execution of the application firmware, the host passes the start address of the application firmware to the KMV11 root firmware.

3.4 CONTROL AND STATUS REGISTER LAYOUT

Figure 3-1 indicates the layout of the CSRs in the host processor I/O page.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL1								BSEL0								SEL0
BSEL3								BSEL2								SEL2
BSEL5								BSEL4								SEL4
BSEL7								BSEL6								SEL6
BSEL11								BSEL10								SEL10
BSEL13								BSEL12								SEL12
BSEL15								BSEL14								SEL14
BSEL17								BSEL16								SEL16

RD1066

Figure 3-1 CSR Definitions

3.5 CONTROL AND STATUS REGISTER BYTE 1 LAYOUT

Register BSEL1 is hardware defined. Figure 3-2 shows the bit layout of BSEL1.

15	14	13	12	11	10	9	8	CSR BIT
RUN	MCLR	WRITE	MODE		READ		ERROR	

RD1067

Figure 3-2 BSEL1 Definitions

Bit	Name	Function
8	Error	This bit will be set when reading or writing to an illegal address in the KMV11 RAM memory or when the address supplied with the RUN command is illegal.
10	Read	When set, this bit directs the root firmware to the memory read routine. The contents of word SEL4 will be used as the memory address. The contents of the memory location will be returned in word SEL6.
11 & 12	Mode	These two bits define the KMV11 mode of operation. 0 – Application mode. The root firmware performs the function defined with the run (without MCLR), read, or write bit. 1 – Reserved. 2 – Maintenance mode 1. Test routines in the root firmware are executed. 3 – Maintenance mode 2. The root firmware clears master clear and puts itself in a continuous loop. For normal operation, these bits will always be cleared on power-up or MCLR to enable the application mode.
13	Write	Used in application mode. When set this bit requests the loading of the contents of SEL6 into the KMV11 at the address specified in SEL4.
14	MCLR (Master Clear)	When this bit is set a power-up initialization is performed. This clears the hardware and restarts the root firmware in the mode defined by the mode bit. The bit is cleared by the KMV11 on completion of initialization.
15	Run	When set, after MCLR, in the application mode configuration, program control is transferred from the root firmware to the application firmware starting at the address contained in SEL4. When set, together with MCLR, the self-test is run before starting operation.

NOTE

When a HALT instruction is executed, program control will be transferred to the root firmware.

3.6 INITIALIZATION AND MODE SELECTION

Before any other operation, after power up, the KMV11 must be initialized. Change of mode is only possible at initialization time. As part of the initialization a one-pass self-test may be performed, depending on the state of switch E29-10 and BSEL1.RUN (BSEL1.7). Initialization is carried out by loading the mode into BSEL1.MODE, and setting BSEL1.MCLR (BSEL1.6) together with BSEL1.RUN if self-test is wanted and not prevented by switch E29-10 being ON.

Initialization, mode selection, and self-test execution is acknowledged by the KMV11 when the MCLR bit (BSEL1.MCLR) is cleared. If at this time the run bit (BSEL1.RUN) remains set, an error has occurred during self-test execution. In this case BSEL0.0-5 contains the number of the test which has failed.

The following flowchart, Figure 3-3, illustrates this sequence.

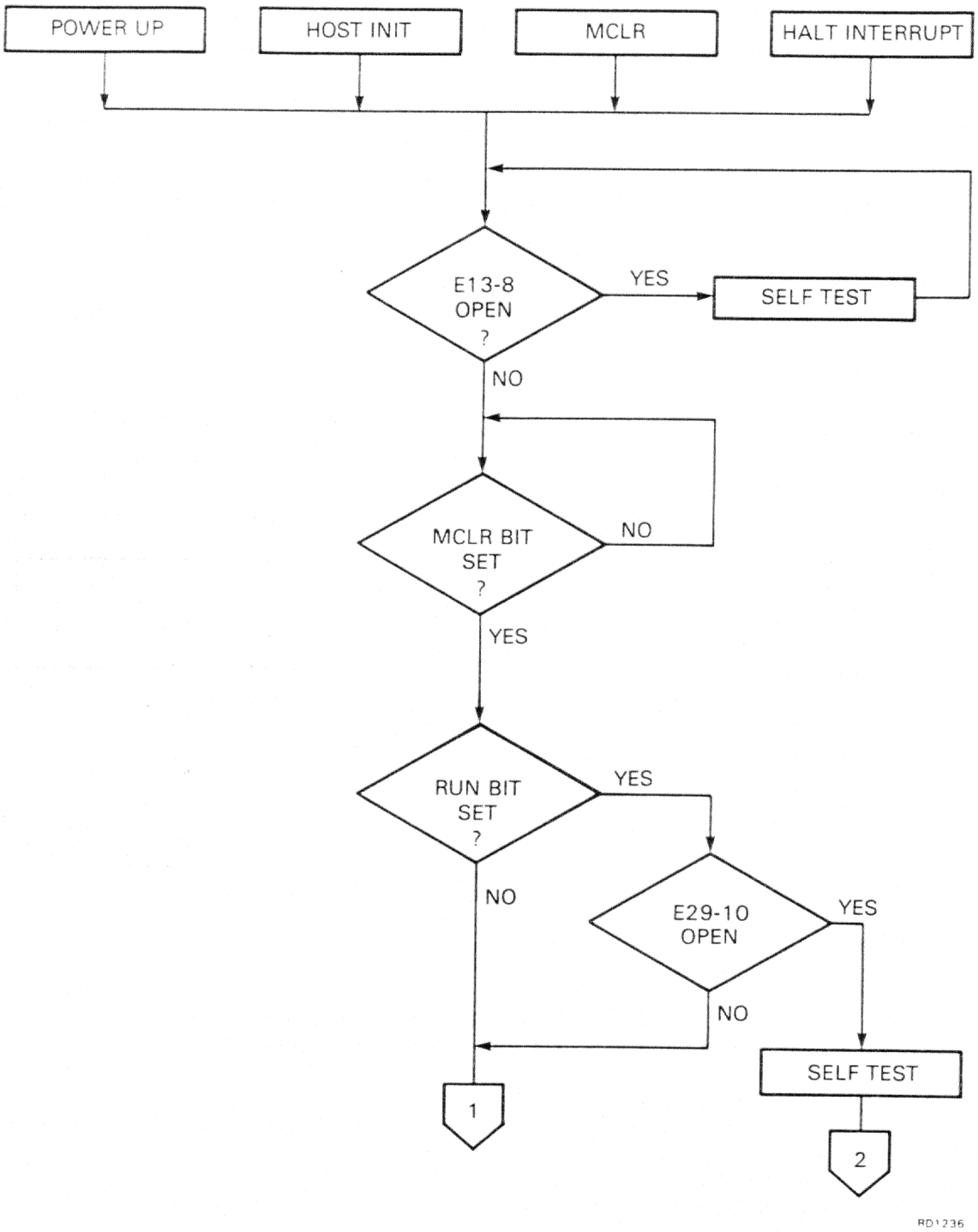


Figure 3-3 Initialization and Mode Setting Flowchart

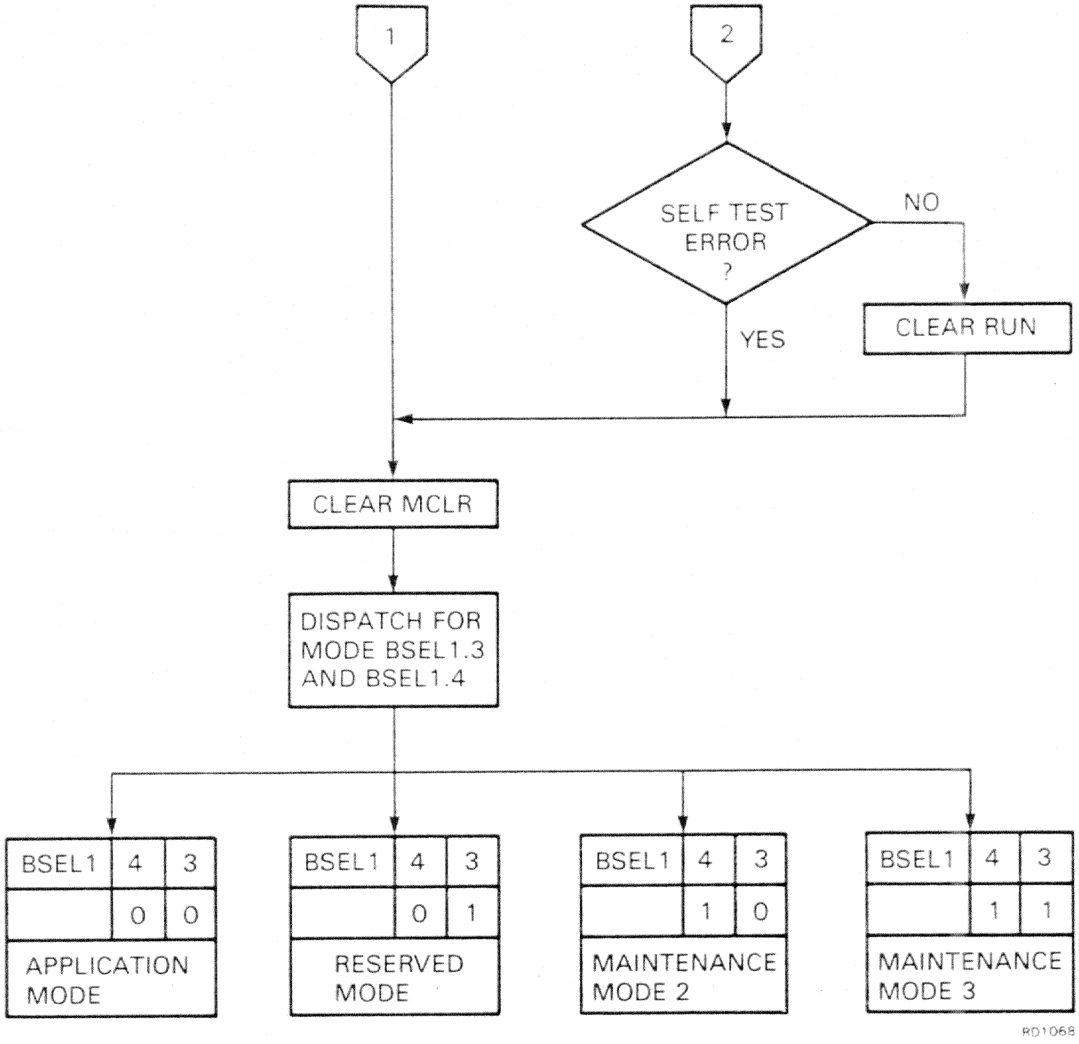


Figure 3-3 Initialization and Mode Setting Flowchart (Cont)

3.7 APPLICATION MODE PROGRAMMING.

Once the application mode is selected, further bit toggling in BSEL1 allows loading, unloading, and starting of the application firmware. These functions are carried out by root firmware resident in ROM.

When the application firmware has been started, instruction execution by the DCT11 is under the control of the application firmware.

However, when a HALT instruction is found during application firmware execution, control is automatically transferred to the root firmware at the restart entry point.

Although the remaining 15 bytes of CSRs are available for implementing any handshake protocol, it must be noted that BSEL0 and BSEL2 cause interrupts to the DCT-11. This means that, if the feature has been enabled, a write access from the host to either one of the register bytes will trigger an interrupt on two vectors within the KMV11 front-end microprocessor.

3.7.1 Application Firmware Loading.

Application firmware is loaded word by word via the CSRs.

- The address has to be written into SEL4
- The date has to be written into SEL4
- The write into KMV11 memory is requested by setting the write bit (BSEL1.5)
- The KMV11-A root firmware clears the write bit to acknowledge the operation; it sets the error bit (BSEL1.0) when the address in SEL4 is considered illegal (either odd address or address not located within the KMV11-A RAM space).

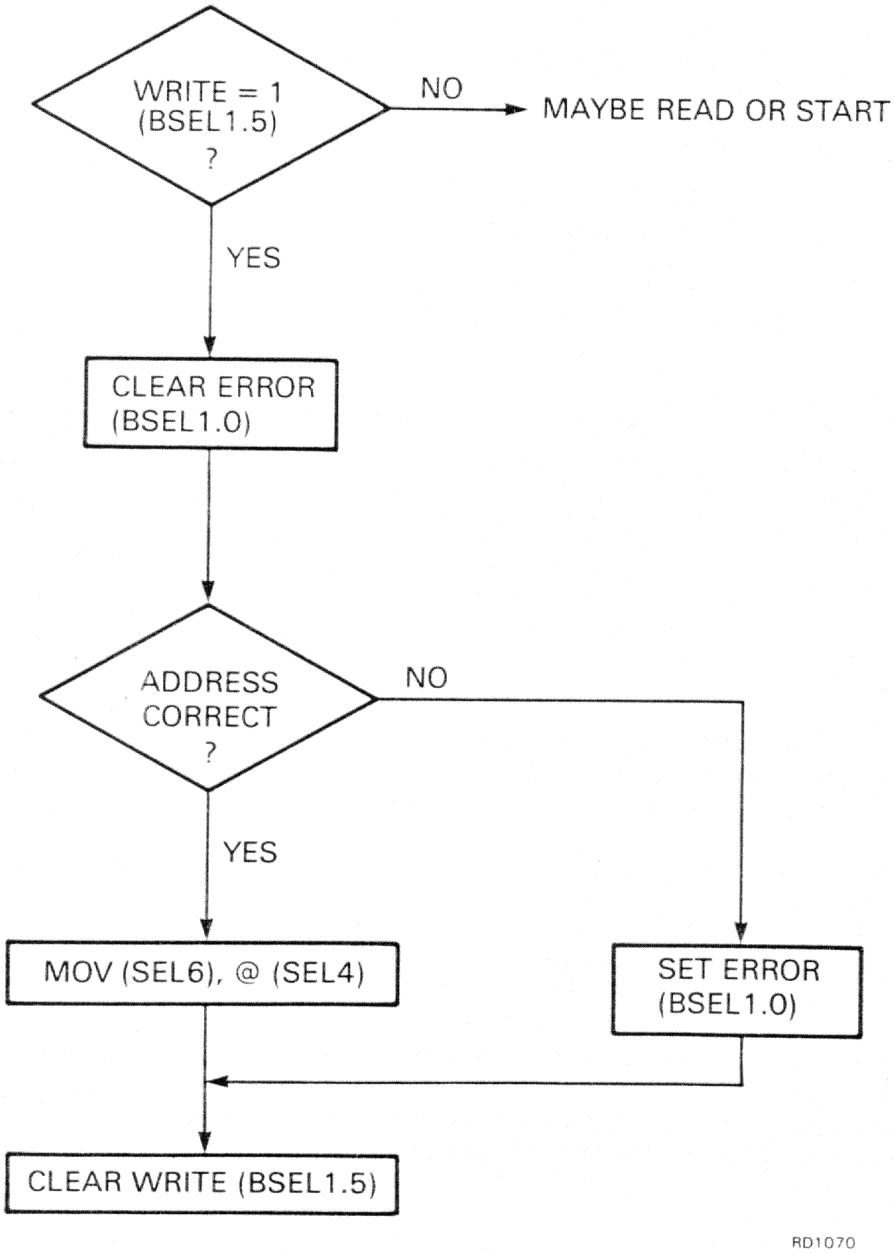


Figure 3-4 Write into RAM Flowchart

3.7.2 Application Firmware Unloading

Application firmware may be unloaded (read) word by word via the CSRs. This may be useful for verifying a previous write.

- The address has to be written in SEL4
- When the read bit (BSEL1.2) is set, the contents of the address in SEL4 will be returned in SEL6 and the read bit cleared by the root firmware.

  If the error bit (BSEL1.0) is set, the address was considered to be illegal (odd address, or not within RAM or ROM space).

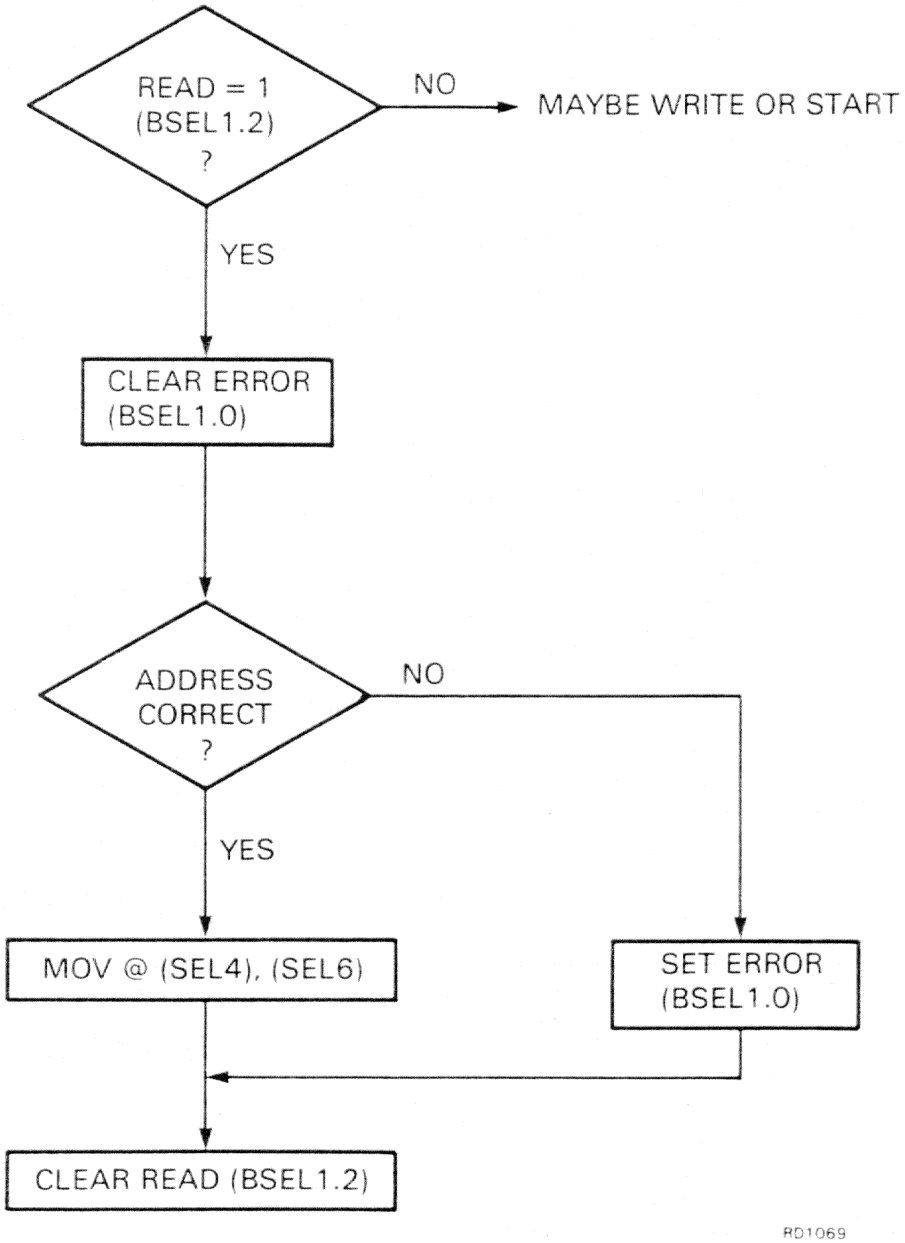


Figure 3-5 Read from RAM or ROM Flowchart

3.7.3 Application Firmware Starting

The previously loaded firmware may be started via the run bit (BSEL1.7).

When this bit is set, the instruction execution is transferred to the address contained in SEL4, unless the address was considered to be illegal (odd address, or not within KMV11 RAM or ROM space). It will be cleared by the root firmware.

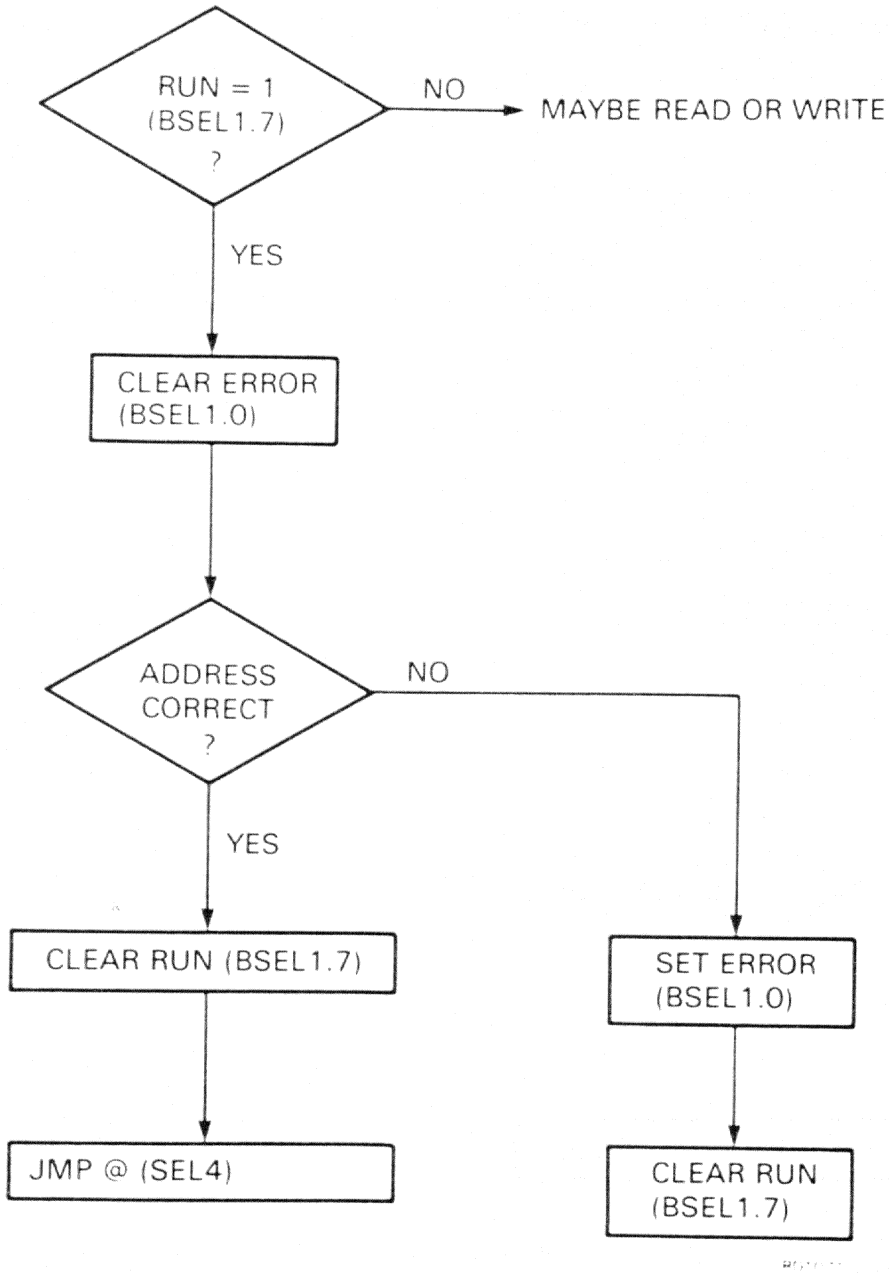


Figure 3-6 Run Flowchart

CHAPTER 4
FUNCTIONAL DESCRIPTION

4.1 SCOPE

This chapter describes the architecture, and the hardware and firmware elements of the KMV11. Together with the drawing set (MP01173) it allows the reader to understand the function of the KMV11.

Prerequisites:

- Understanding of Q-Bus
- Knowledge of the DCT11 microprocessor

4.2 ARCHITECTURE

As shown in Figure 4-1, the KMV11 connects two data paths:

- The Q-Bus (LSI Bus)
- The serial line

The Q-Bus is the route for all data transactions between the host processor and its memories and peripheral controllers.

The KMV11 is one of these peripheral controllers.

The KMV11 is microprocessor controlled. Its functional elements are connected by the DCT11 Bus.

The DCT11 Bus and Q-Bus communicate for:

- CSR transactions (control and status information)
- DMA transactions (data).

4.3 HARDWARE COMPONENTS

The hardware of the KMV11-A is organized into the following functional groups:

- Q-Bus transceivers and address decoders
- Q-Bus protocol logic
- Q-Bus to DCT11 bus data port (CSR RAM)
- DCT11 microprocessor
- RAM memory
- EPROM memory
- DCT11 I/O and interrupt logic
- Line controller (PUSART)
- Line and real-time clock
- Line drivers and receivers

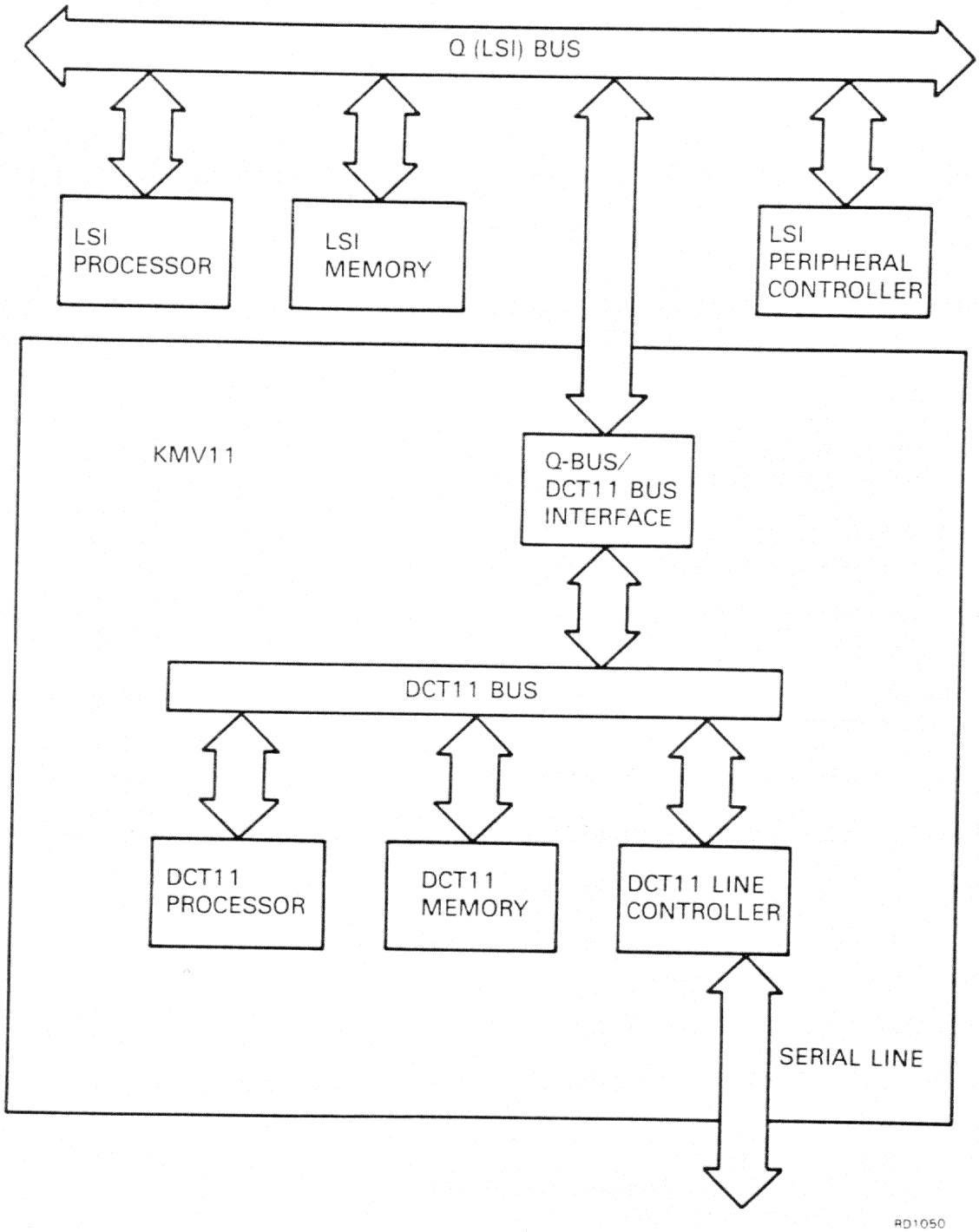


Figure 4-1 KMV11 Architecture

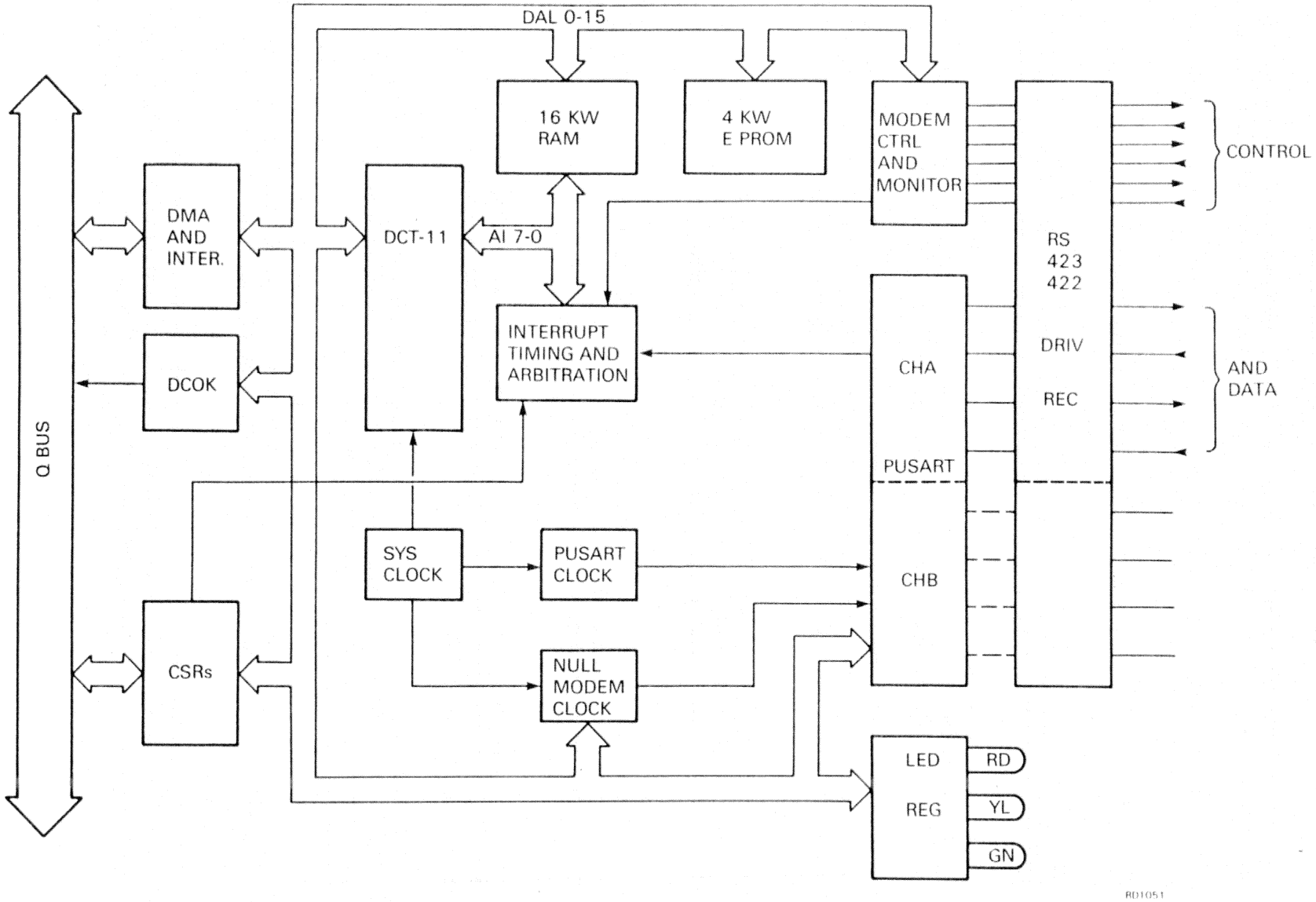


Figure 4-2 Block Diagram of the KMV11

4.3.1 Q-Bus Transceivers and Address Decoders

The DC005 transceiver transfers all information to and from the Q-Bus.

The direction of transfer is determined by QRX H and QTX H. QRX H asserted means that the data flow direction is from the Q-Bus to the DCT11 Bus. QTX H asserted transfers in the opposite direction.

The DC005 transceivers also contain address comparators. MATCH H is asserted when the address on the Q-Bus matches the setting of the address switches.

When VECTOR ENABLE H is asserted during a Q-Bus interrupt transaction, the vector configured by the switches is gated onto the Q-Bus. Vector bit 2 depends on the state of VECTOR 2 H.

The extended address drivers are enabled during the DMA transaction address phase (ADREN). The same holds true for the BBS7 signal, which, when asserted, routes the address into the Q-Bus I/O page.

4.3.2 Q-Bus Protocol Logic

The DC004 decodes the CSR address used in the transactions that follow. The type of transaction (DATI, DATO, DATOB) is determined by the state of OUTHB L, OUTLB L, and IN WORD L.

To decode any CSR address, the CSR logic requests use of the DCT11 bus. When the access has been granted by the DCT11 which is indicated by asserting TDMG H, the transaction (described in the following chapter) takes place and RPLYO H is transmitted to the host, to indicate the end of the CSR transaction.

The DC003 chip controls interrupts on the Q-Bus. These are triggered by a DCT11 write access to the pseudo-register 'Q-CTRL' generating REQ STB H. Interrupts are requested on the BIRQ line, and granted on the BIAKI line. The signal VECTOR H generates the appropriate vector address together with RPLY0 H.

DMA transfers are started by the DCT11 asserting QDMARQ H at the input of the DC010 chip. This occurs on any write access to either the 'extended address out' or 'extended address in' register. At the same time TRANS DIR is latched to indicate the type of transaction to follow (TRANS DIR H asserted = DATO).

The DC010 requests Q-Bus mastership on the BDMR line. Once the DMA is granted by assertion of BDMGI, the DC010 internal timing and logic take over to cause the correct DATO or DATI sequence, depending on the state of TRANS DIR H.

During a DMA transaction the counter 74 LS 390 checks for timeout. A maximum time of 9 microseconds is allowed for a DMA (eight 864 kHz periods). If the period is exceeded (by a nonexistent address) the current DMA transaction is aborted and the timeout indicator is set.

The QINIT flip-flop will be set either by writing a 1 into CSR 0, bit 14 (BSEL1.6) or by the Q-Bus initialize signal. The change from 0 to 1 of QINIT causes the microprocessor to trap to the RESTART address (172 004 – addresses are in octal). QINIT also clears Q-Bus-connected logic.

4.3.3 CSR RAM

Four high-speed RAM memories are referred to as the CSR RAM. Only eight words of the 16-word memory are used for the CSR data port. Six additional words are used for the two DMA channels, the remaining two words are scratch pad locations for use by the root firmware.

The memory can be selected from three sources:

- The DCT11 microprocessor, via the signal 100K RAS L
- The CSR logic, via the signal MEM AD L
- The DMA logic, via the signal MASTER H

The same holds true for the high-order and low-order byte write controls:

- DCT11 write, via the signals WHB PI L or WLB PI L
- CSR write, via the signals OUT SEL HB L or OUT SEL LB L
- DMA write, via the signal MASTER DIN O L

The memory is addressed by the DCT11 latched address lines TALL 1 H to TALL 4 H. These lines are normally controlled by the DCT11 microprocessor during its read/write accesses. However, for CSR and DMA transactions these lines are tristated by the microprocessor: for a CSR access the address will be carried on TALL 1 to TALL 3. During DMA transactions, depending on the direction and the phase of the transaction, the appropriate DMA register address will be forced on these lines.

The 74 LS 245 transceiver provides the gateway between the QDAL lines (Q-Bus) and the TDAL lines (T11 bus).

The 74 S 241 drives the TALL lines during DMA transactions. The 74 S 374 latches the CSR address and drives the TALL lines during CSR transactions.

Sequence of CSR transaction:

1. The DC005 transceivers decode the KMV11 device address at SYNC time and generate MATCH H. SYNC latches the CSR address bits 0 to 2 within the DC004 chip, and bit 3 within 74 LS 74 at the same time as bits 1 to 4 in 74 LS 374.

2. Decoding of any CSR address asserts CSR SEL, which in turn asserts TDMA RQ. TDMA RQ is synchronized with the DCT11 timing, and sampled during PI time.

3. When the DCT11 has granted the DMA via TDMG, 74 LS 374 is enabled to provide the proper CSR address via MEM AD. Assertion of MEM AD also provides the chip select for the CSR RAM chips, as well as the read/write enables OUT SEL HB, OUT SEL LB, and IN WORD SEL.

4. The connection between the Q-Bus lines and TDAL lines is established via TDMG assertion. While the read or write is performed, TDMG causes BRPLY to be generated to acknowledge the transaction to the host.

5. The host responds by negating SYNC, which causes negation of CSR SEL, followed by the drop of the TDMARQ which will be sampled inactive on the following PI strobe.

Sequence of DMA transaction:

1. Any DCT11 write access to either the 'DMA extended address out' register (100 036) or the 'DMA extended address in' register (100 034) triggers the DMA logic, generating QDMA H.

2. The direction flip-flop is clocked to define the direction of the transfer. At the same time QDMA H is asserted and loads the extended address into the QXAD buffer register and sets the request flip-flop which in turn asserts TDMARQ.

3. TDMARQ is clocked at CAS time and sampled during PI time.

4. Once the DCT11 has granted the DMA via T DMG, Q-Bus mastership is requested via QDMARQ on the DC010 chip.

5. MASTER asserted indicates the start of the DMA cycle.

6. MASTER enables the selection of the CSR RAM for use by the DMA logic.

7. The DC010 asserts ADREN to indicate the address phase of the transfer.

8. If the transfer is to be made within the I/O page, ADREN enables the extended address bus drivers and the BBS7 driver. ADREN also forces either the 'DMA address in' register (100 024) or 'DMA address out' register (100 026) address on the TALL 1 to 4 lines. The respective transfer addresses are read out from the CSR RAM and gated onto the Q-Bus BDAL receivers/transmitters.

9. On completion of the address phase, (when ADREN is negated, the DC010 asserts DATEN L for an 'OUT' transfer or DINO H for an 'IN' transfer. In both states the negation of ADREN causes the TALL 1 to 4 lines to switch to either the 'DMA data in' register (100 020) address or 'DMA data out' register (100 022) address.

10. DINO H and MASTER assert WR MEM HB L and WR MEM LB L for an 'IN' transfer.

11. The direction of transfer through the DC005 transceivers and the 74 LS 245 transceivers is determined by the QTX and QRX signals.

12. When data is available from the slave, or accepted by the slave, as indicated by RPLY, the DC010 negates either DATEN for 'OUT' or DINO for an 'IN' transfer, which ends the Q-Bus DMA cycle.

13. The trailing edge of DMA DATEN clocks the REQUEST flip-flop clear.

14. On the following CAS and PI strobes the DMA request on the DCT11 will be sampled inactive, which completes the DMA IN or OUT transfer.

4.3.4 DCT11 Microprocessor

The DCT11 microprocessor, executing the PDP-11 base-level instruction set, interfaces to the KMV11 logic elements via the following lines:

- TDAL 0–15 — Multiplexed address/data lines
- AI 0–7 — a. Multiplexed row and column addresses; b. Output lines for the dynamic RAM; c. DMA and interrupt request input lines

- R/W LB and R/W HB — Read-write control lines

  Both high means read transaction
  Both low means write word
  R/W LB low means write low-order byte
  R/W HB low means write high-order byte

- SEL0, SEL1 — Select lines
  Indicate the type of transaction. Both high indicates DMA transaction.
  SEL0 low for normal fetch, read, and write transactions.

- RAS — Row Address Strobe
  Leading edge indicates valid address information available on TDAL lines and valid row address information available on AI lines

- CAS — Column Address Strobe
  Leading edge indicates valid column address information available on AI lines

- PI — Priority IN strobe
  Used as write strobe; also samples interrupt, HLT and DMA requests on to the AI lines.

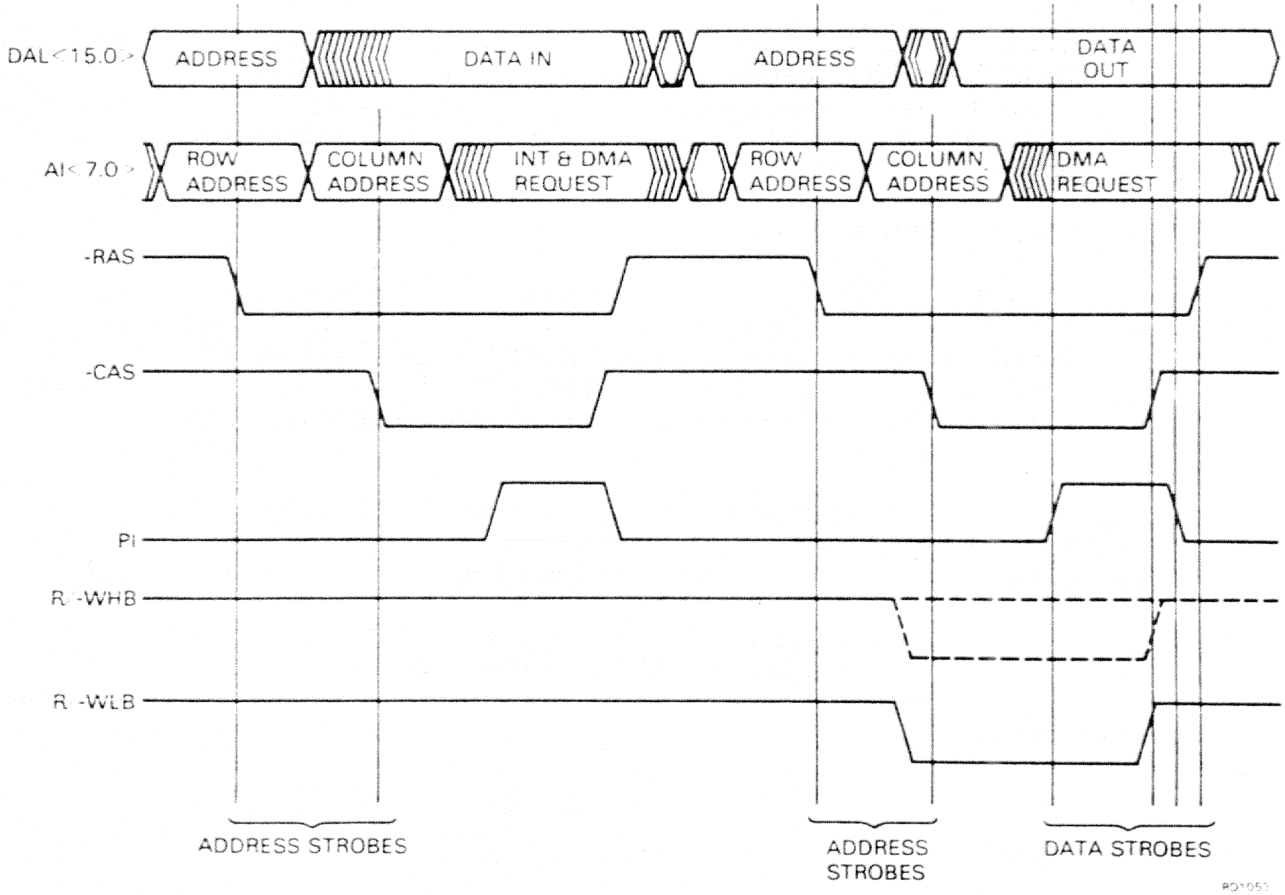


Figure 4-3 Basic DCT11 Timing

Interrupt and DMA requests are sampled within read transactions. DMA requests are sampled within read and write transactions. DMA requests are not serviced during reads before a write to the same address.

Read cycles may follow reads.

Write cycles always follow read, except for stack operations.

Transparent refresh cycles are inserted at a preset rate between normal read-write DMA transactions to ensure correct dynamic memory refreshing.

4.3.5 DCT11 Microprocessor Interrupt System

All external events use the AI lines to cause interrupts, and DMA and HALT requests. In order to synchronize the requests with DCT11 timing, they are latched with the leading edge of the CAS strobe and sampled with the PI strobe.

- Halt interrupt (may also be caused by executing the HALT (0) instruction)

  The halt is caused by a Q-Bus INIT, or by the host setting the MCLR bit (CSR0, bit 14). The halt request is latched in 74 LS 74 at CAS time and gated on to TAI 7 during PI time. The result is an unconditional trap to the restart location 172 004. Note that this interrupt is caused by the change in level of the halt signal. Halt must be reset before another halt interrupt can be detected and serviced.

- DMA request

  The DMA request is caused either by a host to CSR access, or by a KMV11 to host DMA transfer (DATO or DATI). In both conditions the purpose of the DCT11 DMA state is to release the TALL and TDAL lines for use by the CSR and DMA logic, when accessing the CSR RAM. The request is latched in 74 LS 74 at CAS time and gated on to TAI 0 during PI time.

- Coded priority interrupts

  The remaining TAI lines are used in a 'coded priority interrupt' system. The configuration of the CP0 to CP3 lines, gated onto the TAI 4 to TAI 1 lines with the PI strobe, are interpreted by the DCT11 as interrupt requests on four different priority levels. These point to a range of vectors determined by an internal decoding table. Table 4-1 shows the relation between the eight possible interrupt sources and their assigned priorities and vectors.

Table 4-1 Vector Assignment and Priority

Requesting Device	C.P. Encoding				Priority	Vector	ACK
	-CP3 (AI1)	-CP2 (AI2)	-CP1 (AI3)	-CP0 (AI4)			
RX Data channel A	L	L	L	L	7	140	Note
RX Data channel B	L	L	H	L	7	150	Note
TX Data channel A	L	H	L	L	6	100	Note
TX Data channel B	L	H	H	L	6	110	Note

Table 4-1 Vector Assignment and Priority (Cont)

Requesting Device	C.P. Encoding				Priority	Vector	ACK
	-CP3 (AI1)	-CP2 (AI2)	-CP1 (AI3)	-CP0 (AI4)			
PUSART Special Cond.	H	L	L	L	5	120	Note
Timer	H	L	H	L	5	130	Note
CSR 0 transaction	H	H	L	L	4	60	Note
CSR 2 transaction	H	H	H	L	4	70	Note

NOTE

These interrupts are not self-clearing. A request continues as long as the interrupting condition has not been serviced.

4.3.6 Microprocessor Implementation

The 'processor' page of the drawing set MP01173 shows how the DCT11 microprocessor is implemented within the KMV11-A. The 6912 kHz clock comes from a 13824 kHz crystal oscillator and a divider chain, that provides all timing references for the KMV11. AI-1 to AI-7 lines are buffered to provide the necessary drive capabilities for the 16 dynamic RAM chips. The multiplexed data/address lines TDAL 1 to TDAL 15 are latched to provide stable addressing information on TALL 1 to TALL 15 H. TALL 15H divides the available 32K word addressing space between 16K word RAM space and 16K word I/O and PROM space.

The decoder divides the I/O space into eight chip select signals.

4.3.7 Front-End Processor Address Space

The DCT11 microprocessor address space is divided into three sections: a read/write memory section of 16K words, a read only memory section of 4K words, and an I/O address space of 12K words.

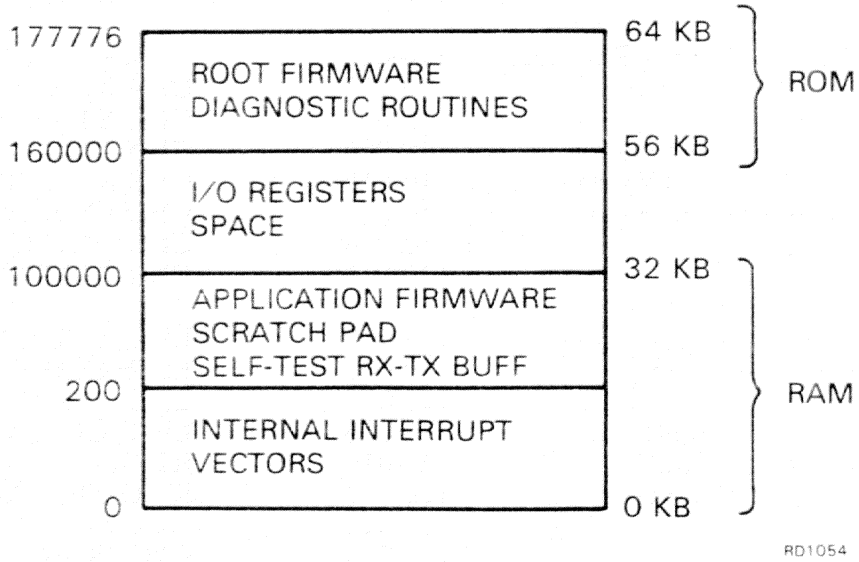


Figure 4-4 KMV11 Memory Map

4.3.8 I/O Register Assignment

The I/O register space, from 100 000 to 160 000, is divided into five logical areas each allocated to one of the functional components. Each component has an address space of 10000_8 bytes.

The functional component address spaces are:

1. CSR and DMA registers, 100 000 to 107 777
2. Line controller chip, 110 000 to 117 777
3. Clock chip, 120 000 to 127 777
4. Peripheral port chip, 130 000 to 137 777
5. Q-bus control, 140 000 to 147 777

Table 4-2 I/O Register Assignments

Address Range	Destination	Address	Registers	
100 000 107 777	CSR RAM	100 000	CSR 0	R/W
		100 002	CSR 2	R/W
		100 004	CSR 4	R/W
		100 006	CSR 6	R/W
		100 010	CSR 10	R/W
		100 012	CSR 12	R/W
		100 014	CSR 14	R/W
		100 016	CSR 16	R/W
		100 020	DMA DATA IN	R/W
		100 022	DMA DATA OUT	R/W
		100 024	DMA ADDRESS IN	R/W
		100 026	DMA ADDRESS OUT	R/W
		100 030	ROOT FW SCRATCH	R/W
		100 032	ROOT FW SCRATCH	R/W
		100 034	EXTENDED ADDR IN	R/W
		100 036	EXTENDED ADDR OUT	R/W
110 000 117 777	7201 PUSART	110 000	CHA RX BUF	RO
		110 002	CHA TX BUF	WO
		110 004	CHA STATUS	RO
	(only low-	110 006	CHA COMMAND	WO
	order bytes	110 010	CHB RX BUF	RO
	are used)	110 012	CHB TX BUF	WO
		110 014	CHB STATUS	RO
		110 016	CHB COMMAND	WO
120 000 127 777	8254 Timer	120 000	LINE CLOCK 1 RD	RO
		120 002	LINE CLOCK 1 WR	WO
		120,004	LINE CLOCK 2 RD	RO
	(only low-	120 006	LINE CLOCK 2 WR	WO
	order bytes	120 010	RT CLOCK RD	RO
	are used)	120 012	RT CLOCK WR	WO
		120 014	not used	–
		120 016	CLOCK CONTROL WR	WO

Table 4-2 I/O Register Assignments (Cont)

Address Range	Destination	Address	Registers	
130 000	8255 I/O	130 000	A PORT READ	RO
137 777		130 002	not used	–
		130 004	not used	–
	(only low-	130 006	C PORT WRITE	WO
	order bytes	130 010	not used	–
	are used)	130 012	B PORT WRITE	WO
		130 014	not used	–
		130 016	8255 CONTROL WR	WO
140 000	Q-bus Control	140 000	QIRQ, QDCOK	WO
147 777				
150 000		RESERVED		
157 777				

RO = Read-Only register
WO = Write-Only register
R/W= Read-Write register

NOTE

Only MOV or MOVB instructions may be used to operate on RO and WO registers. Instructions which first read, then perform operations in internal processor registers and write the results back like INC, BICB, BISB, ADC and so on may only be used with R/W registers.

The tristate drivers connected to TDAL 9 and TDAL 11 define mode parameters for the DCT11 at power-up.

MEM READ is generated during RAM and PROM read transactions. It is used to gate the memory read bus, which is shared by the PROM and RAM, to the TDAL lines. The memory read bus is needed because of the RAM chip timing characteristics.

4.3.9 Line Controller and Clock

The line controller is the 7201 PUSART (or equivalent) chip (E46). It basically serializes information to be transmitted and deserializes received information. This is done for:

- Asynchronous protocols
- Character synchronous protocols (monosync, bisync)
- Bit synchronous protocols (SDLC, HDLC).

It features some fundamental protocol functions such as:

- Parity generation and checking
- CRC generation and checking
- Flag/sync transmission and synchronization
- Break/abort/framing error detection
- Bit stuffing and stripping for HDLC/SDLC.

In addition it is used to monitor four modem status leads and generate one modem control signal.

Operation of the chip is controlled through a set of internal registers. They are accessible by the microcode as well as five interrupt-generating control leads.

A more detailed description of this chip is beyond the scope of this manual, but may be found in the KMV11 User's Guide.

The chip is selected when 110K RAS L is asserted. The TALL 2 and TALL 3 lines select one of the internal registers. TALL 1 selects between read and write addresses. This selection system holds true for all the 8255 and 8254 type chips. The TDAL 0 to 7 lines carry information to and from control registers and data buffers within the chip.

RXDRQA is asserted high when the transmit buffer is empty. It causes an interrupt request to vector 140.

TXDRQA is asserted high when the transmit buffer is empty. It causes an interrupt request to vector 100.

RXDRQB is asserted high when the transmit buffer is empty. It causes an interrupt request to vector 150.

TXDRQB is asserted high when the transmit buffer is empty. It causes an interrupt request to vector 110.

RXDRQB and TXDRQB are channel B interrupt request lines, not used in the KMV11-A.

INT L is asserted for special receive conditions and external events, requesting an interrupt to vector 120.

The change in state of the following modem lines:

- CCITT 109 (Carrier Detect)
- CCITT 106 (Clear to Send)
- CCITT 107 (Data Set Ready)
- CCITT 125 (Ring Indicator)

is monitored within the chip and causes an interrupt if the feature has been enabled by the microcode.

Transmit and receive clocks come from two sources:

- External clock (DCE clock)
- Internal clock

Selection between the two clock sources is made within a multiplexer. SCM asserted high, gives the internal clock source. A programmable counter chip provides the internal clock sources (LCLK1, LCLK2) as well as the DTE terminal clock modem signal (CCITT 113).

The external transmit clock is modem line CCITT 114.

The external receive clock is modem line CCITT 115.

For synchronous operation the following standard clock rates are programmable:

64 Kbytes/s
56 Kbytes/s
48 Kbytes/s
19.2 Kbytes/s
9.6 Kbytes/s
9.8 Kbytes/s
4.8 Kbytes/s
1.2 Kbytes/s and below

For asynchronous operation the bit rates are as follows:

19.2 Kbytes/s
9.6 Kbytes/s
4.8 Kbytes/s
2.4 Kbytes/s
1.2 Kbytes/s and below

A second multiplexer provides an internal loopback capability for diagnostic purposes. When SLP is asserted high, the transmit outputs of both channels are connected to their receive inputs. At the same time modem line CCITT 103 (Transmit Data) is held in the MARK state.

The third programmable counter is used to implement a software timer. Output RTCL H can be programmed to interrupt once at terminal count or at repeating intervals.

Details of the operation and programming of the 8254 connector timer chip may be found in the KMV11 User's Guide.

4.3.10 Multiport Chip and Q-Control

The multiport chip (8255) implements two 1-byte-wide firmware-writable OUT registers and one 1-byte-wide firmware readable IN register.

The following signals are generated by this chip:

B Port

Bit 7:	TTL 108 A	–	Modem signal: CCITT 108 (Data Terminal Ready)
Bit 6:	reserved		
Bit 5:	Q DMA EN	–	When asserted high, allows DMA transactions
Bit 4:	TER IN SER	–	Modem signal: Terminal In Service
Bit 3:	I/O page	–	When asserted high, asserts BBS7 on the Q-Bus during DMA transactions
Bit 2:	TTL 141 AH	–	Modem signal: CCITT 141 (Local Loopback)
Bit 1:	TTL 140 AH	–	Modem signal: CCITT 140 (Remote Loopback)
Bit 0:	TTL 111 AH	–	Modem signal: CCITT 111 (Select Frequency)

C Port

Bit 7:	EN CSRI 2H	–	Enable interrupt when host accesses CSR2 low-order byte
Bit 6:	EN CSRI 0H	–	Enable interrupt when host accesses CSR0 low-order byte
Bit 5:	SCM H	–	When asserted, selects internal clock mode
Bit 4:	SLP H	–	When asserted, selects internal loop mode
Bit 3:	RDLD H	–	Red LED
Bit 2:	YLLD H	–	Yellow LED
Bit 1:	GNLD H	–	Green LED
Bit 0:	ENRTC H	–	When asserted, allows timer interrupts

The following signals are monitored through the multiport chip:

A Port

Bit 7:	latch timeout	–	Cleared when DMA is triggered, set if DMA timeout occurred
Bit 6:	TTL 142 AH	–	State of modem line CCITT 142 (Maintenance Mode)
Bit 5:	TTL 112 AH	–	State of modem line CCITT 112 (Rate Indicator)
Bit 4:	SW1 H	–	Asserted, when switch E29-10 is OFF
Bit 3:	reserved		
Bit 2:	SW2 H	–	Asserted, when switch E13-8 is OFF
Bit 1:	KMV11-AH	–	Asserted for KMV11-A
Bit 0:	reserved		

A flip-flop allows programmable negation of DCOK on the Q-Bus to reboot the host system for down-line loading applications. REQ STB generated by a write access to the low-order byte of address 140 000 also clocks the Q-Bus interrupt request within the DC003 chip.

4.3.11 Line Receivers and Drivers

The sheet entitled 'Line Receivers' of drawing set MP01173 shows the modem line receivers. The receiver chips are 26 LS 32 (or equivalent) differential line receivers, they convert from EIA RS-422, RS-423, and RS-232-C electrical levels to TTL levels.

The 4.7 kiloohm resistors tied to one pin of each receiver input provide a common reference for RS-423 and RS-232 unipolar operation. The 24 kiloohm resistors provide a negative bias to the receiver inputs to keep them in 'failsafe condition'. The 'failsafe condition' needs open data lines to be interpreted as in the MARK state (TTL +3 V) and control lines as in the OFF state (TTL 0 V).

The charge pump supplies –12 V to the failsafe resistors and to the line driver supply.

Switches E85-9 and E85-10 disconnect pins U and X from the modem cable assembly. They should only be OFF when the connection of the modem causes a conflict on these pins.

Wire link W15 allows CCITT 109 (Carrier Detect) to be permanently asserted. It is normally out.

Changes from the normal configuration (E85-9 and E85-10 ON, W15 not installed) will cause errors in the modem line loopback tests.

The line drivers may be found on sheet 'line drivers' of print set MP01173.

The 26 LS 31 or equivalent chip is the 4-line driver for the RS-422 (V.11) category I (differential) circuits.

The 26 LS 29 or equivalent chip is the quad driver for the RS-423 (V.10) category I (unipolar) circuits.

Selection between RS-422 and RS-423 is done by positioning DIP switches E85 1 to 8:

- E85 1 to 4 ON, E85 5 to 8 OFF provides RS-422 operation
- E85 1 to 4 OFF, E85 5 to 8 ON provides RS-423 operation.

Other combinations are illegal.

Category II circuits for both RS-422 (V.11) and RS-423 (V.10) are driven by a second 26 LS 29 or equivalent chip.

Terminal in Service (connector Pin C) is not a commonly used modem line but is needed for loopback testing. It should therefore only be disconnected by removing wire link W14 when the connection causes a conflict with the modem in use.

4.4 FIRMWARE COMPONENTS

The following functions are provided by the root firmware permanently resident in the KMV11 PROM set.

- Power-up initialization
- Mode control
- Diagnostics

4.4.1 Power-up Initialization

When power is applied to the KMV11 the following actions take place:

1. BCLR is asserted for about 15 microseconds. While BCLR is asserted, the MODE bits are read on the TDAL lines
2. After negation of BCLR, 10 refresh transactions are performed on the dynamic RAM
3. Instruction execution is started at the power-up entry point ($172\ 000_8$)
4. The firmware will set the mode of the peripheral chip (8255) and the PUSART chip (7201), and set up the stack pointer
5. Depending on the configuration of the self-test switches, the firmware will either:
   - Omit the self-test (E13-8 ON, E29-10 ON)
   - Do one pass of self-test (E13-8 ON, E29-10 OFF)
   - Loop in self-test continuously (E13-8 OFF)
6. In any of these states, MCLR (BSEL1.6) will force the firmware to the mode controller.

4.4.2 Mode Control

When the MCLR bit is asserted, the firmware will check BSEL1.3–4 to enter one of the modes of operation defined as follows.

BSEL1		Mode
Bit 4	Bit 3	
0	0	Application mode
0	1	Reserved mode
1	0	Maintenance mode 2
1	1	Maintenance mode 3

In application mode, if the run bit (BSEL1.7) is asserted, together with the MCLR bit, one pass of the self-test will be performed, before starting execution in the application mode, providing switch E29-10 is OFF to allow self-test.

On successful completion the run bit and the MCLR bit will be cleared and the firmware will be ready for the first application mode command.

If an error occurred in the self-test, only the MCLR bit will be cleared, the run bit will stay set and the firmware will loop, waiting for a new master clear. BSEL0 contains the number of the failing test routine in bits 0 to 5. (See Table 5-3.)

Regardless of self-test execution, the MCLR bit will always be cleared by the firmware to acknowledge mode selection.

4.4.3 Diagnostic Firmware

Diagnostic firmware is a set of test routines and two monitors.

One of the monitors is started by initializing mode 2. It executes the test requested in BSEL0 and uses BSEL2 to BSEL17 for parameter transfer. On successful completion of the test, the test number in BSEL0 will be cleared: otherwise the setting of bit 7 or bit 6 will indicate an error, with error information in BSEL2 to BSEL17. The main use of this monitor is by host-resident diagnostic programs.

The other monitor is the self-test monitor. It is selected at power-up, or by setting the run bit together with the MCLR bit in BSEL1. It chains the test routines and provides the appropriate parameters in BSEL2 to BSEL17.

When the self-test is running in the continuous loop mode (E13-8 OFF) it uses either the:

- Normal test table (E29-10 OFF)
- Extended test table (E29-10 ON).

The normal test table omits tests that need an external loopback connector. It also omits the memory address interaction test, which takes about one hour to complete.

Maintenance mode 2 is only a NOP loop, allowing a host-resident diagnostic to perform data dependability tests on the CSRs without microprocessor intervention.

CHAPTER 5
SERVICE

5.1 SCOPE

This chapter contains information for servicing the KMV11-A. It includes the maintenance philosophy, maintenance functions, preventive maintenance, and corrective maintenance. The section on corrective maintenance contains a short description of the diagnostics for the KMV11-A.

5.2 MAINTENANCE PHILOSOPHY

The field replaceable unit (FRU) for the KMV11 is either a defective module or cable. The training of Field Service personnel concentrates on the use of diagnostics to isolate the FRU. Spare parts for module repair are not available in the field. Typical applications of the KMV11 do not permit long troubleshooting sessions. Component troubleshooting and repair needs at least a 16-channel logic analyzer.

CAUTION

When inserting or removing the KMV11 module, be sure not to move any components mounted on sockets (for example, PROMs or the microprocessor).

5.3 MAINTENANCE TOOLS AND FEATURES

The following features are provided with the KMV11 to help fault isolation and status checking:

- LED indicators
- On-board diagnostics
- Line clock and loopback connectors.

5.3.1 LED Indicators

Five small red LED indicators show the status of the following modem signals (at TTL level):

CCITT 103	Transmit Data	(inverted, MARK = LED OFF)
CCITT 104	Receive Data	(true, MARK = LED ON)
CCITT 107	Data Set Ready	(true, ON = LED ON)
CCITT 106	Clear to Send	(true, ON = LED ON)
CCITT 109	Carrier Detect	(true, ON = LED ON)

Three large colored LEDs are operated by the microcode.

The physical location of the LEDs is shown in Figure 5-1.

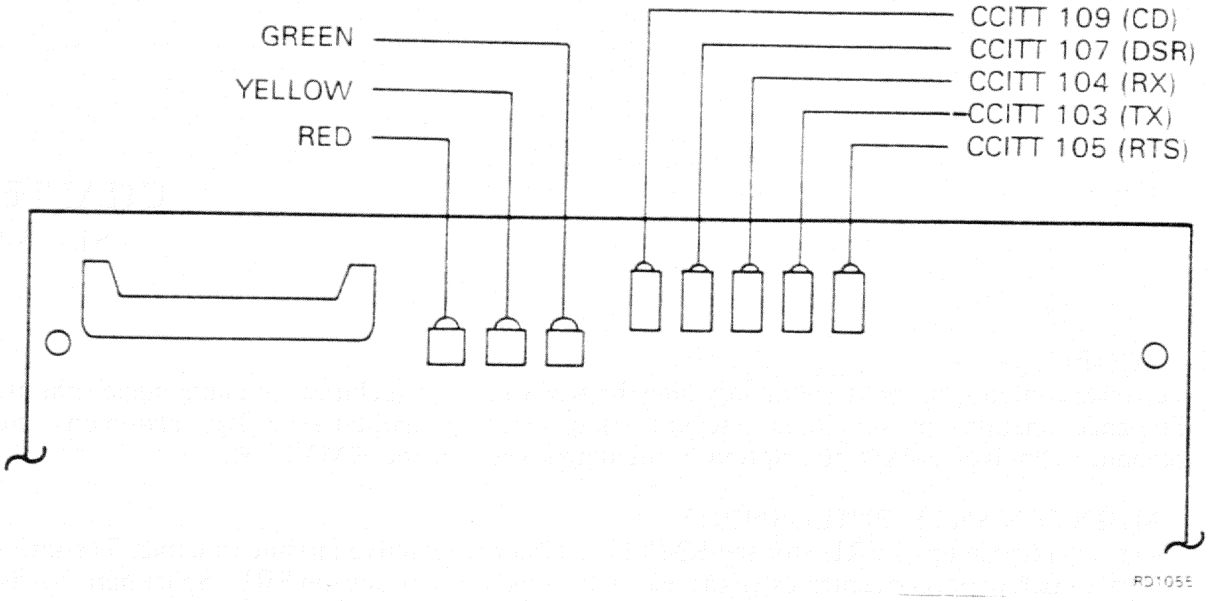


Figure 5-1 LED Indicator Location

Table 5-1 shows the meaning of the microcode-operated LED display.

NOTE

This table is only true for the PROM-resident firmware. Application firmware may drive the LEDs in other ways.

Table 5-1 LED Meaning

LED Status			State	Comment
Red	Yellow	Green		
OFF	ON	OFF	KMV power on self-test disabled self-test started	Steady state if self-test is disabled, 10 seconds, at self-test start
OFF	ON	ON	Self-test execution for 1 pass	10 seconds duration
OFF	OFF	ON	Self-test successful completion	Steady state
ON	OFF	OFF	Self-test error	Steady state on first error
OFF	ON	ON/ OFF	Normal self-test running in continuous loop	10-second period between green ON/OFF states

Table 5-1 LED Meaning (Cont)

LED Status Red	Yellow	Green	State	Comment
OFF	ON	ON/ OFF	Extended self-test running in continuous loop	½-second period between green ON/OFF states
OFF	ON	ON/ OFF	Logic or line controller diagnostic running without errors	Random periods between green ON/OFF states
OFF/ ON	ON	ON/ OFF	Logic or line controller diagnostic running with errors	Random periods between green and red ON/OFF states depending on number of errors and diagnostic

5.3.2 Self-Test

The major part of the PROM-resident firmware is for on-board diagnostic facilities. Routines may be used by the host-resident diagnostic or in a chained mode by the self-test.

The self-test will run in one of the following modes. The modes are selected by on-board dip switches:

a. Single pass on power-up or when requested by the host software's setting the run and MCLR bits together

b. Continuous loop on power-up

c. Continuous loop on power-up with extended diagnostic routines.

Refer to Figure 5-2 for the self-test switch locations and Table 5-2 for the switch configuration.

Table 5-2 Self-Test Switch Configuration

State E13–8	E29–10	Action
ON	ON	Self-test disabled
ON	OFF	Self-test runs for one pass at power-up or when run bit asserted together with MCLR bit
OFF	OFF	Self-test starts to run in endless loop at power-up: normal mode
OFF	ON	Self-test starts to run in continuous loop at power-up: extended mode

Note that the loop time for normal mode is approximately 30 seconds, while for extended mode it can be as long as 1 hour! Correct execution of the extended self-test needs either the module loopback connector (H3255) or the RS-422/RS-423 modem cable assembly with loopback connector (H3251).

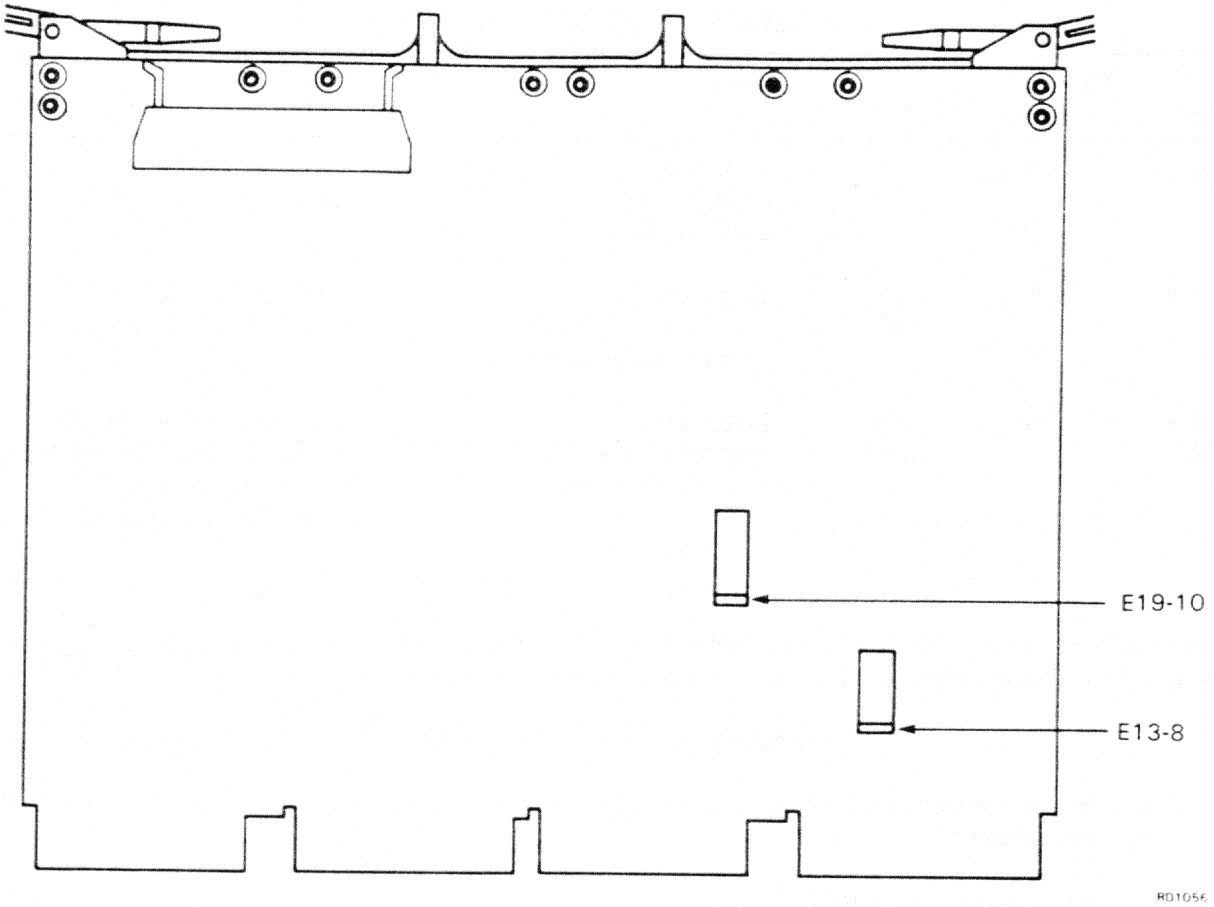


Figure 5-2 Self-Test Switch Locations

On detection of any error condition, testing will be aborted and the red LED will be ON (green and yellow OFF). In addition the low-order byte of CSR0 will contain 1xx or 2xx, where xx is the test number in error according to the test number table (Table 5-3).

Table 5-3 Self-Test List

Test	Description (Addresses and Patterns in Octal)	Comment
0	Stack push-pull test (RAM locations 77774, 77776)	S
1	CSR and DMA registers word access test (pattern 52525)	
2	CSR and DMA registers word access test (pattern 125252)	
3	CSR and DMA registers byte access test (pattern 252)	
4	CSR and DMA registers byte access test (pattern 125)	
5	Dynamic RAM data test (pattern 52525)	
6	Dynamic RAM data test (pattern 125252)	
7	Dynamic RAM address test (pattern = address)	
10	Dynamic RAM address test (pattern = address inverse)	
11	Real-time clock test (8254 clock/counter chip)	
12	Baud rate generator test, channel A (8254 clock/counter chip)	
13	Baud rate generator test, channel B (8254 clock/counter chip)	B

Table 5-3 Self-Test List (Cont)

Test	Description (Addresses and Patterns in Octal)	Comment
14	Dynamic RAM address interaction test (pattern 177777)	E
15	PROM checksum verification test	
16	KMV11-B modem signal loopback test, channel A	B,E
17	KMV11-B modem signal loopback test, channel B	B,E
20	RX-TX, channel A, internal loopback, interrupt disabled	
21	RX-TX, channel B, internal loopback, interrupt disabled	B
22	RX-TX, channel A, internal loopback, low-speed, interrupts enabled	
23	RX-TX, channel B, internal loopback, low-speed, interrupts enabled	B
24	RX-TX, channel A, internal loopback, high-speed,interrupts enabled	
25	RX-TX, channel B, internal loopback, high-speed, interrupts enabled	B
26	RX-TX, channel A, external loopback, high-speed, interrupts enabled	E
27	RX-TX, channel B, external loopback, high-speed, interrupts enabled	B,E
30	KMV11-A modem signal loopback test	A,E

COMMENTS
S: This test is always executed at power-up
A: Runs on the KMV11-A only
B: Runs on the KMV11-B only
E: Runs only in extended self-test mode

5.3.3 Line Clock and Loopback Connectors

A programmable line clock is available for transmission and reception without a modem or other external clock source.

5.3.3.1 Line Clock – Two counters provide local transmit/receive clocks for null modem connections or test purposes. The A and B line clocks are identical, but the B line clock is only useful with the KMV11-B.

Both counters are fed with a 6912 kHz clock. The divider ratio or both counters may be programmed from 1 to 32768_{10} in binary mode, or from 1 to 10000_{10} in BCD mode.

For maintenance or special applications the output of the A line clock may be applied to the TRANSMIT CLOCK A, RECEIVE CLOCK A, and the output of the B line clock to the respective channel B clock inputs of the MPSC chip.

The line clocks are always available on the CCITT 113 modem line. (Channel A and channel B for KMV11-B).

NOTE

When PTT requirements specify the CCITT 113 lines to be held in a steady OFF state, no divider ratio should be programmed into the clock chip for the counter(s) concerned.

5.3.3.2 Real-Time Clock – A third counter within the 8254 is available as a real-time clock.

Its output will generate an interrupt to vector 130 on priority level 5 (on-board DCT11 system).

Two modes of operation are available :

- One-shot mode (mode 0)
- Clock mode (mode 2)

In one-shot mode the counter will interrupt after a preset time interval and stop. In clock mode the counter will give a series of interrupts separated by the preset time interval.

Time intervals for both modes may be computed according to the following formula:

$$\text{Time} = 18.5 \text{ microseconds} \times (N + 1)$$

where N is programmable from 1 to 32768_{10} in binary mode, and from 1 to 10000_{10} in BCD mode.

In addition to processor priority level masking, RTC bit 0 of the 8255 port C (address 130 006_8) disables/enables the real-time clock interrupt.

This bit must be reset, after an RTC interrupt has occurred, to acknowledge the interrupt and may then be set again to enable the next clock interrupt.

5.3.3.3 Loopback Connectors/Tests – Three types of loopback are available for use with the KMV11-A:

1. Module – provided by H3255 for use on the M7500 module connector J1.

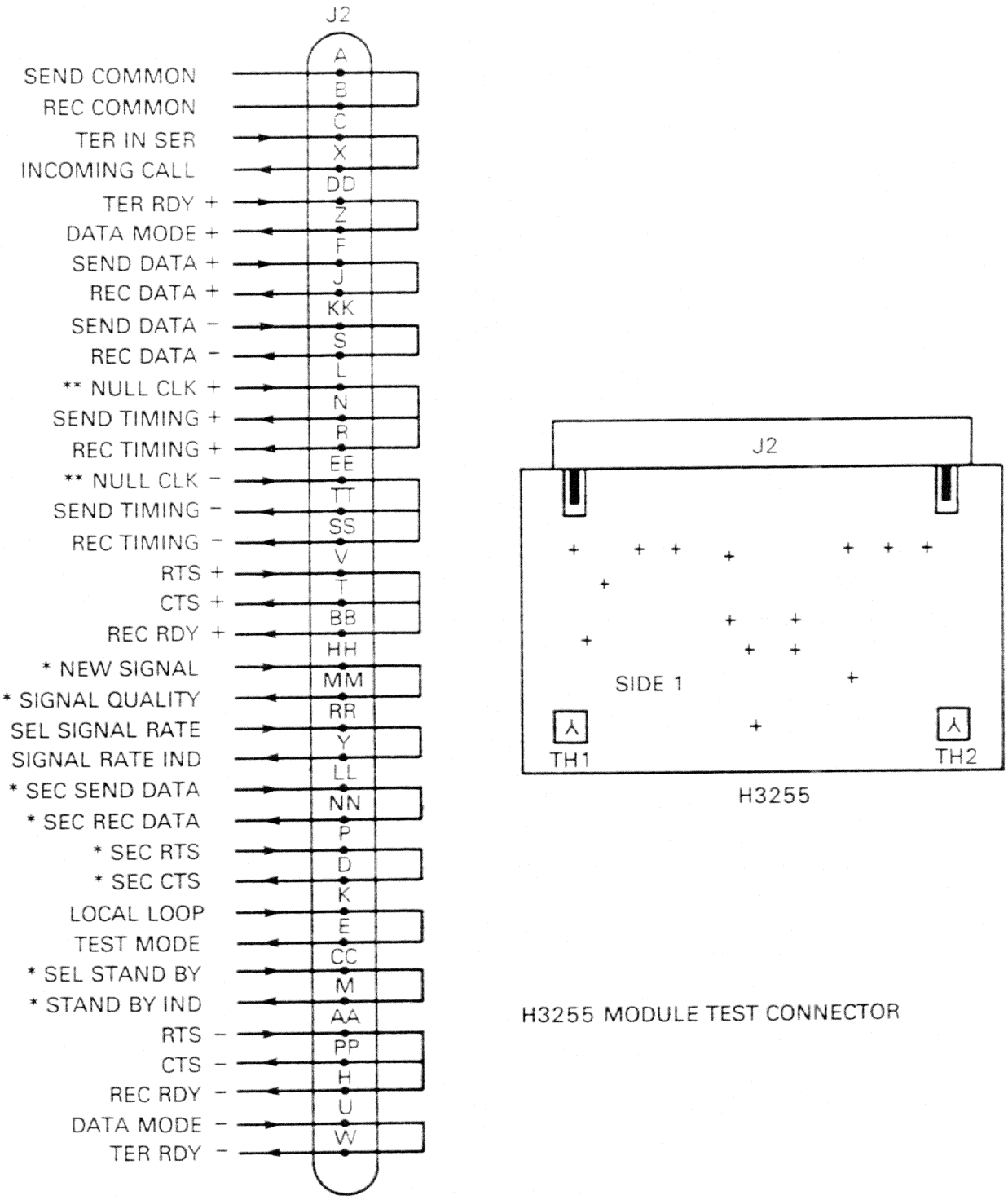
2. Cable – provided by:

   a. H3251 for 37-pin RS-449 cable connectors
   b. H325 for 25-pin RS-232 cable connectors (see note)

NOTE

The RS232 loopback (H325) connector cannot be used for modem signal loopback tests. It does not provide turnaround for all modem signals used by the KMV11.

3. Modem – some types of modem have internal loopback facilities. This feature is used by the functional diagnostic VKMC on the KMV11-A only. Both local and remote modems may provide the loopback.



H3255 MODULE TEST CONNECTOR

* NOT REQUIRED FOR KMV11
** RS-499 SIGNAL = TERMINAL TIMING

RD1057

Figure 5-3 KMV11 Loopback Connector H3255

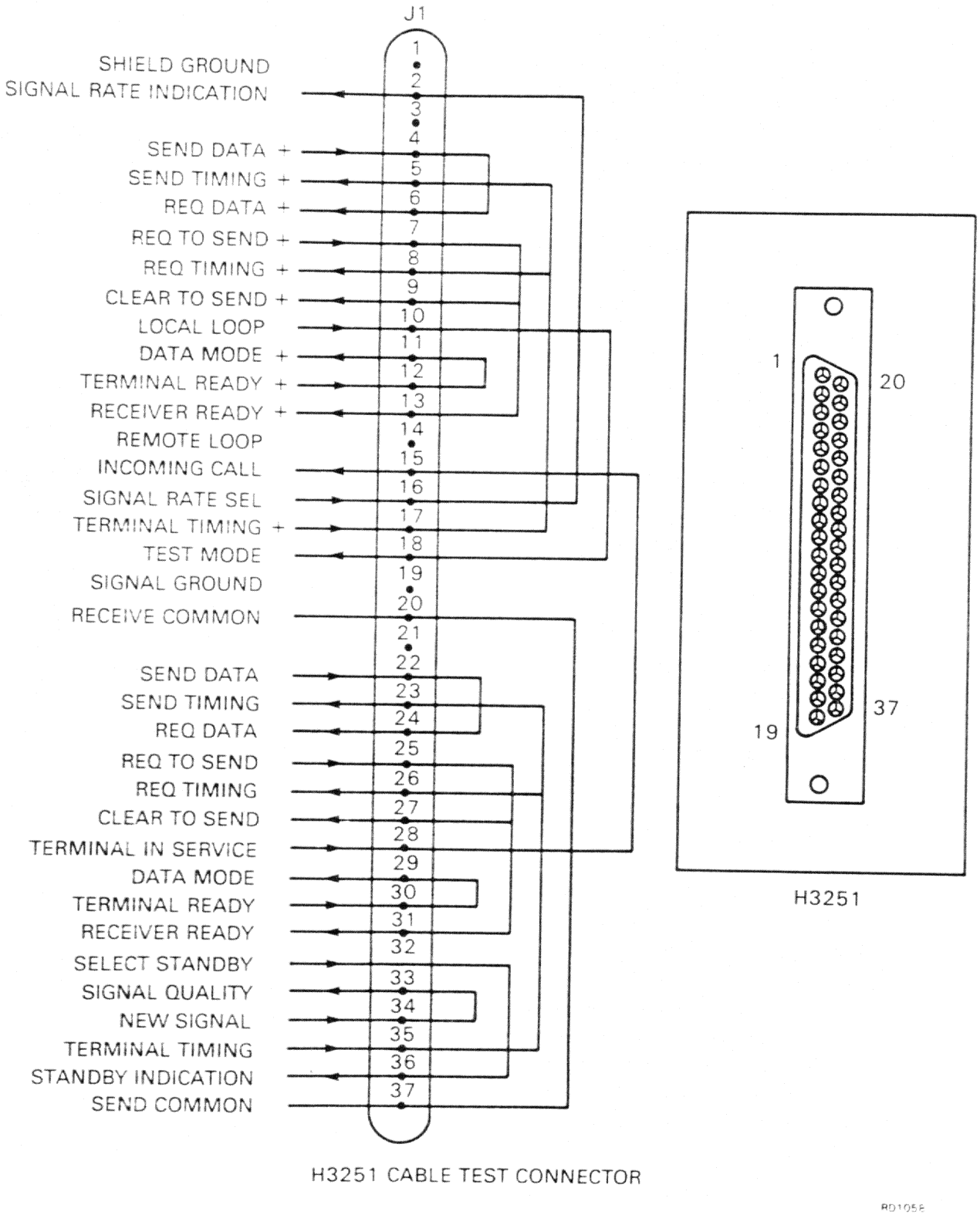


Figure 5-4 KMV11 Loopback Connector H3251

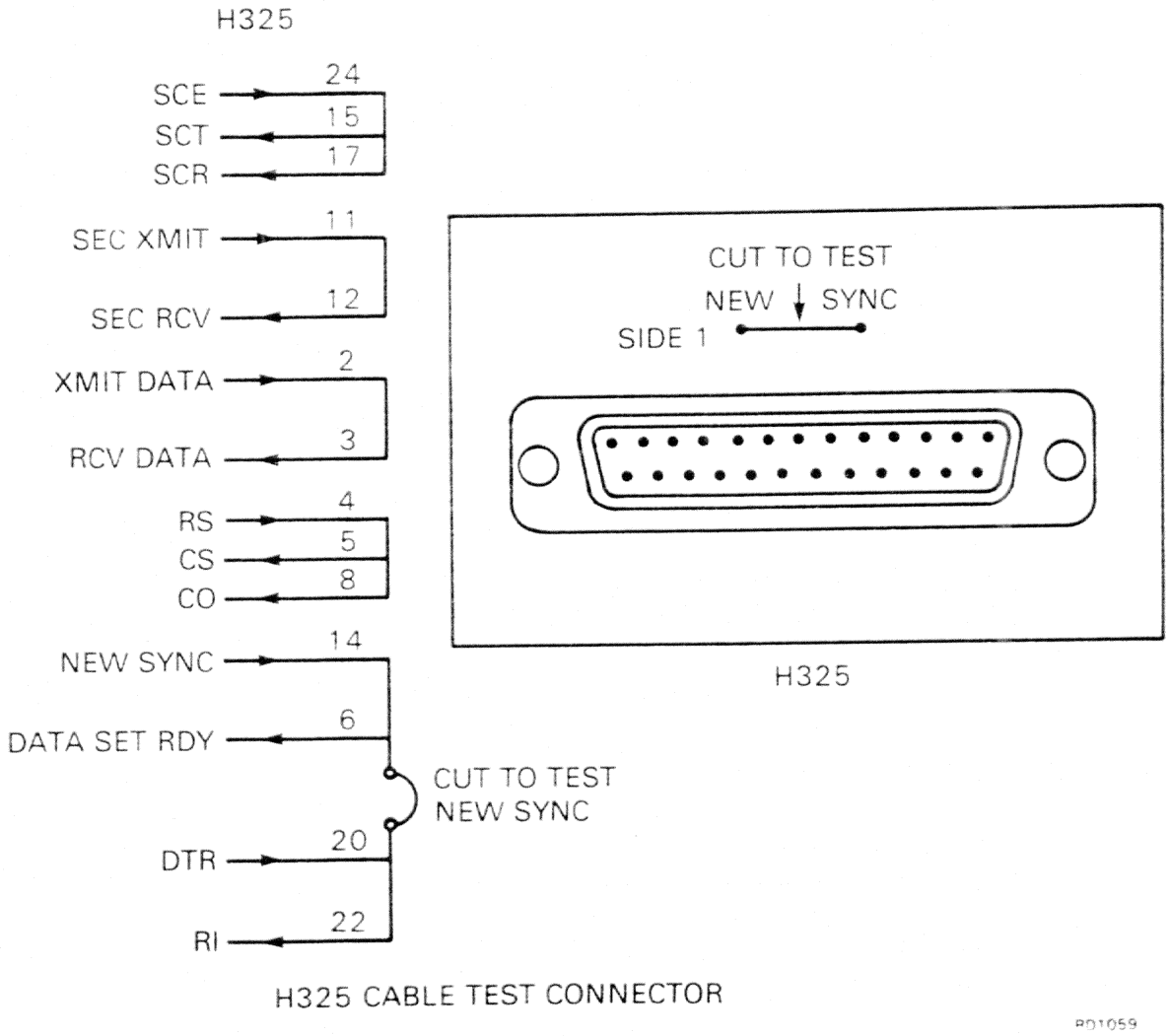


Figure 5-5 KMV11 Turnaround Connector H325

5.4 DIAGNOSTICS

As well as the on-board self-test, four diagnostic programs are provided with the KMV11-A:

1. VKMA logic diagnostic
2. VKMB line controller diagnostic
3. VKMC functional diagnostic
4. XKMD DECX-11 exerciser module

The first three programs are run under the standalone diagnostic supervisor. They must be overlaid with the diagnostic supervisor, or be previously combined with it and loaded as a single file. In both methods, the programs will not exceed 16K of memory with the exception of the VKMCA functional diagnostic.

5.4.1 VKMA Logic Diagnostic

This diagnostic does not need any cable or loopback connector. The execution time for one error-free pass is five minutes.

Test description:

Test 1: checks accessibility of KMV CSR addresses
Test 2: clears and checks KMV CSR registers
Test 3: data integrity test (CSR 2 to 16)
Test 4: data integrity test (CSR 0)
Test 5: CSR byte access test

Test 6: CSR 2 data transfer test
Test 7: CSR 4 data transfer test
Test 8: CSR 6 data transfer test
Test 9: CSR 10 data transfer test
Test 10: CSR 12 data transfer test

Test 11: CSR 14 data transfer test
Test 12: CSR 16 data transfer test
Test 13: combined CSR data test
Test 14: dynamic RAM pattern test
Test 15: dynamic RAM address test

Test 16: dynamic RAM inverted address test
Test 17: PROM revision level check
Test 18: PROM read checksum verify
Test 19: DMA transfer, Q-Bus to KMV11
Test 20: DMA transfer, KMV11 to Q-Bus

Test 21: DMA transfers, both directions, and memory interaction test
Test 22: KMV11 to Q-Bus interrupts
Test 23: Q-Bus to KMV11 interrupts

5.4.2 VKMB Line Controller Diagnostic

This diagnostic may run in either internal or external loopback mode, depending on the operator's answer to the startup question on the presence of an external loopback connector.

Tests 7 and 8 will not be executed in internal mode.

Test description:

Test 1: checks accessibility of KMV CSR addresses

Test 2: PROM revision level check

Test 3: real-time clock interrupt test

Test 4: baud rate generator test

Test 5: transmit-receive various length frames in internal loop mode – no interrupts – low-speed

Test 6: transmit-receive various length frames in internal loop mode – interrupts enabled – low- to high-speed

Test 7: transmit-receive various length frames in external loop mode – interrupts enabled – high-speed

Test 8: modem leads external loopback test

5.4.3 VKMC Functional Diagnostic

This diagnostic loads firmware into the KMV11 and exercises the KMV11 as an HDLC communication controller. It provides X.25 Layer 1 (physical layer) protocol functions, and modem control. A detailed discussion appears in the appendix.

The purpose of this diagnostic is to provide troubleshooting facilities for both DIGITAL Field Service engineers and users' support staff. It is fully supported and will be updated as necessary by DIGITAL's software distribution organization.

When used on the KMV11-A this diagnostic program may be used with all types of loopback; that is module, cable, and local and remote modem (if the modems have these facilities).

NOTE

The host memory must be more than 16K words for this diagnostic

Test description:

Test 1: verifies KMV11 initialization

Test 2: runs self-test

Test 3: application firmware load, unload, and start

Test 4: CSR handshaking without interrupts

Test 5: CSR handshaking with interrupts

Test 6: QIO processing in case of resource error

Test 7: QIO processing for various command sequences

Test 8: transmit/receive buffer processing at 2.4 kbytes/s with modem control

Test 9: transmit/receive buffer processing at 2.4 kbytes/s with modem control

Test 10: transmit/receive buffer processing at 64 kbytes/s with modem control

Test 11: transmit/receive buffer processing at 64 kbytes/s without modem control

Test 12: transmit/receive buffer processing at 48 kbytes/s with modem control and address search enabled

5.4.4 XKMD DECX-11 Exerciser Module

This module is provided to allow the KMV11 to be included in the host system's DECX-11 system exerciser. Error-free operation shows that the KMV11 does not react with other system bus activity in a worst-case environment.

The module exercises the KMV11 using test routine number 14 (combined DMA data in and data out test) checking transmitted data against received data and monitoring the KMV11 status.

NOTE

No data is transmitted or received via the serial line. Only pathways and logic between the host and KMV11 are exercised.

5.5 PREVENTIVE MAINTENANCE

There is no specific KMV11 PM schedule. A general check of voltages and connections should be done when system PM is performed. After moving KMV11 modules or cables, a complete checkout of the devices, by running all diagnostics, is needed.

Special care must be exercised because some chips are installed in sockets and may be moved during removal or replacement of the KMV11 or adjacent modules.

5.6 CORRECTIVE MAINTENANCE

The FRU is either the KMV11 module or a cable. All corrective diagnostics should be applied to isolating the failing FRU. KMV11 diagnostics are designed to help in the isolation process and should be run in the following sequence:

1. VKMA logic diagnostic
2. VKMB line controller diagnostic
3. VKMC functional diagnostic
4. XKMD DECX-11 module included within the appropriate DECX-11 system exerciser.

Before considering a KMV11 module to be defective, check switch settings and the wire link configuration by referring to Chapter 2.

APPENDIX A
BASIC HDLC/SDLC FRAMING FIRMWARE

A.1 GENERAL INTRODUCTION

In order to test the KMV11 option in a true data communication environment, the functional diagnostic uses a firmware program to handle basic HDLC/SDLC framing with full modem control according to DEC STD 052. This appendix contains a description of the firmware program and should be used both as an example of how to develop application firmware and as a reference guide for the firmware used by the functional diagnostic. The functional diagnostic loads the firmware as a normal application mode firmware program and passes control to the start address of the basic HDLC/SDLC firmware. The firmware defines the use of the CSRs other than BSEL1.

A.2 CSR DESCRIPTION

The basic HDLC/SDLC firmware uses the first four CSR words out of the eight CSR words available, to provide communication between the host and the KMV11.

A.2.1 BSEL0 and BSEL2 Definitions

The KMV11 is the controller of the CSRs, and the host computer user program can only read or write into the CSRs when permitted by the KMV11. A protocol must be followed by the user program if it is to issue commands successfully and receive status from the KMV11. In order to specify the type of interaction that will take place between the user program and the KMV11, the user program must set up specific bit configurations in BSEL0 and BSEL2. The exchange of a command or response between the KMV11 and the host is called a (CSR) transaction.

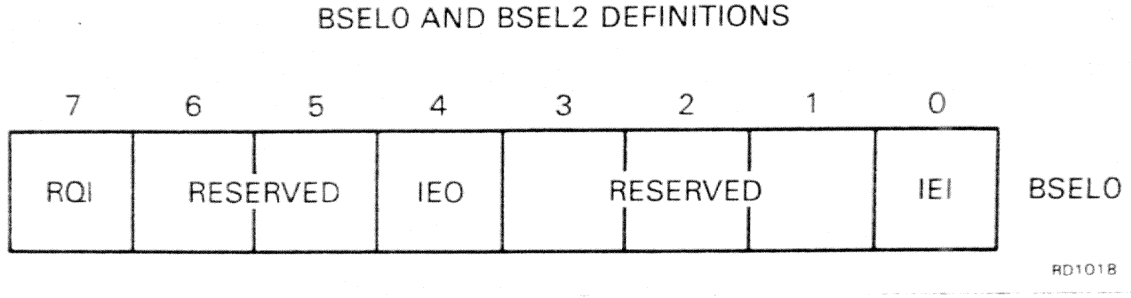


Figure A-1 Control Register BSEL0

Table A-1 BSEL0 Definitions

Bit	Name	Function
0	IEI	Interrupt Enable In – set and reset by the host (PDP-11) to enable/disable interrupts to vector xx0.
1	not used	
2	not used	
3	not used	

Table A-1 BSEL0 Definitions (Cont)

Bit	Name	Function
4	IEO	Interrupt Enable Out – set and reset by the host (PDP-11) to enable/disable interrupts to vector xx4.
5	not used	
6	not used	
7	RQI	Request In – set by the host, to request one or more CSR transactions. Cleared by the host before the end of the last transaction.

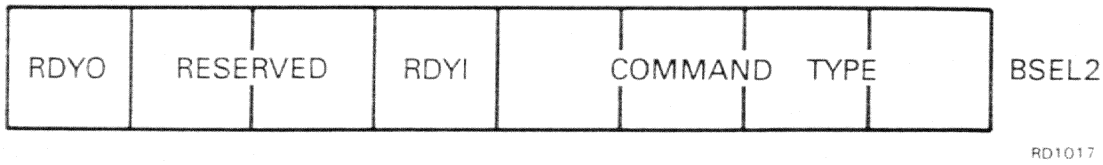


Figure A-2 Control Register BSEL2

Table A-2 BSEL2 Definitions

Bit	Name	Function
0–3	Command/ response	The command/response field determines the type of CSR transactions. See the description of commands and responses for details.
4	RDYI	Set by the KMV11 to indicate granting of a CSR transaction. Causes an interrupt to vector xx0 if IEI is set. Cleared by the host at the end of the transaction.
5	not used	
6	not used	
7	RDYO	Ready Out – set by the KMV11 to flag a KMV11 to host CSR transaction: cleared by the host, when CSR information has been accepted. This bit causes an interrupt to vector xx4 if IEO is set.

A.2.2 Definitions of BSEL3 to BSEL7

The information in BSEL3 to BSEL7 depends on the command or response type specified in BSEL2. It is defined in the following section.

A.3 INPUT COMMANDS

These request that data be transferred from the user program to the KMV11. This can only be done via a specific user program to the KMV11 handshaking subroutine. This user program must first request use of the six data port bytes (BSEL2 to BSEL7) by setting RQI (BSEL0.7).

The KMV11 will then respond by asserting RDYI (BSEL2.4). This then gives the user program control of the data ports to load the command until the user program clears RDYI, thereby giving up control until a future request is issued.

The latency between the user program setting the RQI bit and the KMV11 responding by setting RDYI can range from 50 microseconds to 500 microseconds with an average time of 250 microseconds.

When the user program requests use of the data port bytes by setting RQI it has two choices:

1. Set the IEI (BSEL0.0) bit to enable interrupts. As a result the KMV11 interrupts the main CPU at vector xx0 when it sets the RDYI bit.

   After an interrupt has occurred, the user program can proceed directly to load registers BSEL2 to BSEL7 with the appropriate data, and to clear RDYI.

2. Leave the IEI bit cleared and check the state of the RDYI bit every 100 microseconds. The form of the bit test sequence based on a timer is:

```
C: BITB  RDYI,BSEL2
   BNE   A              ;  RDYI set, load command,
   BR    B              ;  resume previous task at B. When
A:                      ;  timer goes off return to C.
```

   After a command is issued, an output status will be returned by the KMV11 when appropriate, depending on the command and the function to be performed. At this point the user program can request use of the six data port bytes by again setting RQI (BSEL0.7).

   Care must be taken not to overwrite BSEL2 to BSEL7 (they may be still in use by the KMV11) until the KMV11 again asserts RDYI (BSEL2.4).

A.4 OUTPUT RESPONSES

Output status interactions can be started by the KMV11 at any time. The KMV11 indicates to the user program that it has status available by setting RDY0 (BSEL2.7). If the user program has previously set IEO (BSEL0.4), then an interrupt vector at xx4 will take place. If IEO has not been set, the user program must periodically test RDYO but not more often than every 100 microseconds. After the user program has serviced the status indications provided by the KMV11, the user must then clear RDY0, to indicate completion.

When there is contention between RQI from the user program and RDYO from the KMV11, the conflict is solved in favor of RDYO.

A.5 EXAMPLES OF CSR HANDSHAKING

The following are four possible sequences for CSR handshaking:

1. Input command without interrupt
2. Two input commands with interrupt
3. Output response without interrupt
4. Two input commands and one response with interrupt

Example 1: Input Command Without Interrupt

User Program	KMV11
Set RQI	
Wait for RDYI set	Set RDYI
Recognize RDYI Load info. in BSEL2 to BSEL7 Clear RQI Clear RDYI in BSEL2	
	Handle the command

Example 2: Two Input Commands With Interrupt

User Program	KMV11
Set IEI Set RQI	
	Set RDYI Generate interrupt xx0
Interrupt occurs Load info. in BSEL2 to BSEL7 Clear RDYI in BSEL2	
	Handle the command . . . Because RQI remains set, set RDYI Generate interrupt xx0
Interrupt occurs Load information in BSEL2 to BSEL7 Clear RQI Clear RDYI in BSEL2	
	Handle the command

Example 3: Output Response Without Interrupt

User Program	KMV11
Wait RDYO	Load BSEL2 to BSEL7 with information Set RDYO
Recognize RDYO Handle response Clear RDYO	

Example 4: Two Commands And One Response With Interrupt
(the response occurs when the first command is being serviced)

User Program	KMV11
Set IEI and IEO Set RQI	
	Set RDYI Generate interrupt xx0
Handle interrupt Load BSEL2 to BSEL7 with info. Clear RDYI in BSEL2	Output response occurs, user program has use of the port bytes.
	Handle the command
	Load BSEL2 to BSEL7 with info. Set RDYO Generate interrupt xx4
Handle interrupt Handle response Clear RDYO	
	Set RDYI because RQI remains set Generate interrupt xx0
Handle interrupt Clear RQI Load BSEL2 to BSEL7 with info. Clear RDYI in BSEL2	
	Handle the command

A.6 BASIC HDLC FRAMING FIRMWARE COMMANDS AND RESPONSES

In this section, the possible commands and status responses specific to this option are given. The general CSR format of the commands is given in Figure A-3. The general CSR format of the status responses is given in Figure A-4. Each command and response CSR format is described in Paragraph A.7.

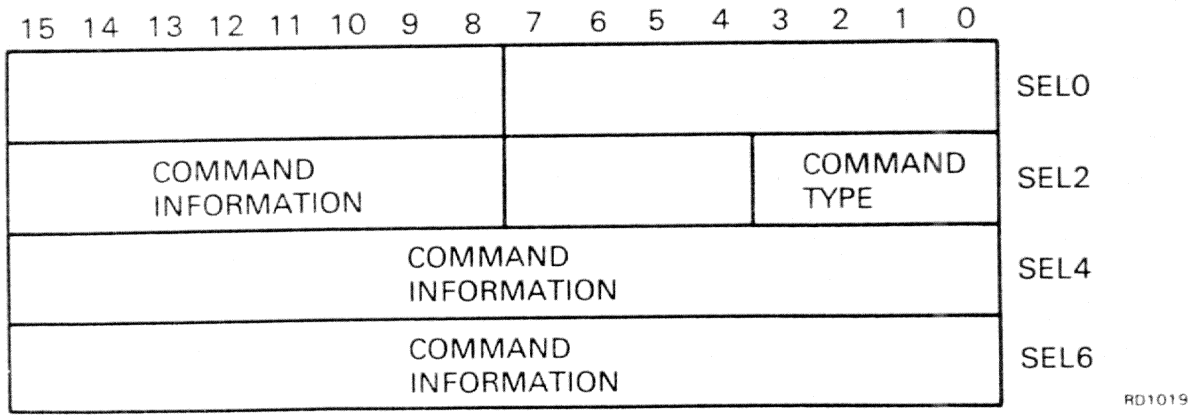


Figure A-3 CSR Command Format

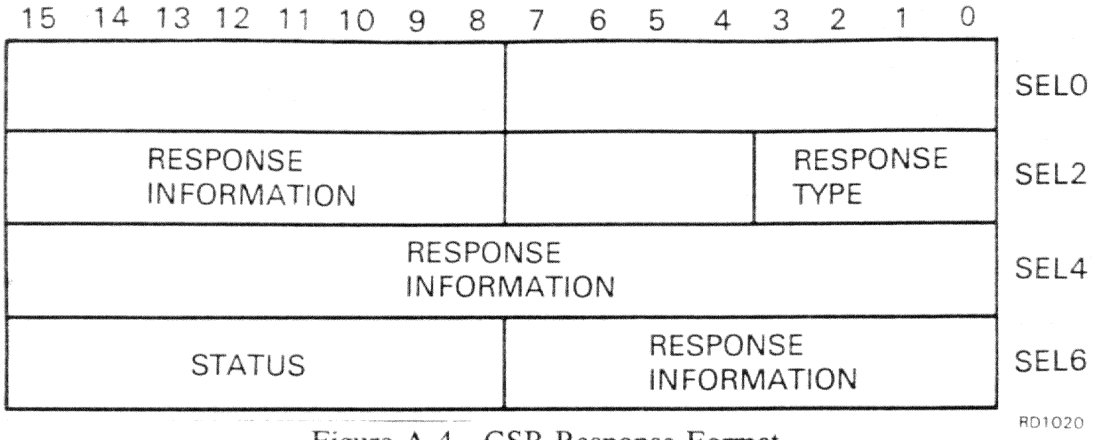


Figure A-4 CSR Response Format

The command and response types appear in SEL2.0–3 and are numbered from 0 to 17_8:

0 : Dummy
1 : Configurate
2 : Deconfigurate
3 : Dummy

4 : Modem change response
5 : Transmit buffer
6 : Receive buffer
7 : Transmit abort

10 : Receive abort
11 : Dummy
12 : Dummy
13 : Dummy

14 : Read modem
15 : Dummy
16 : Enable modem survey
17 : Disable modem survey

Command and response information fields are defined for each command and response. They give complementary data such as: buffer address and buffer length. They are described together with each command and response in the section that follows.

The status returns relating to each response are summarized in Paragraph A.9. Most responses come as an answer to a command, in a synchronous way. However, some response statuses may appear asynchronously (that is, not as an answer to a command) as when a modem lead changes state. A detailed description of commands and responses follows.

A.7 MODEM CONTROL

The basic HDLC/SDLC framing firmware will handle most modem control signals. To report changes in modem leads to the host, the firmware supports asynchronous responses to the host when Data Set Ready, Carrier Detect, Clear to Send, or Ring Indicator changes state, and the host has indicated that it wants to be informed of modem lead changes.

To be able to take the correct modem-controlling actions, the following states are defined in the firmware. The current state may be obtained by the host by means of a read modem command.

- Off-line (S1), master clear or S7B: DTR off, RTS off, TxD mark
- Enabled (S3), configurate or S7A: DTR on and RTS on
- Waiting for start (S5), DSR on: start 30-second timer
- Data exchange (S6), DSR on, CD on and CTS on: stop S5 or S6A timer if active
- Line failure (S6A), CD off: start 2-second timer
- Disconnect (S7A), DSR off or S5 or S6A timeout: DTR off, RTS off, TxD mark start 250-millisecond and 2-second timer; if 250-millisecond timeout and DSR off or 2-second timeout return to S3
- Deconfigure (S7B), deconfigurate: DTR off, RTS off, TxD mark start 250-millisecond and 2-second timer; if 250-millisecond timeout and DSR off or 2-second timeout return to S1.

A.7.1 Modem Control for Full Duplex, Data Leads Only

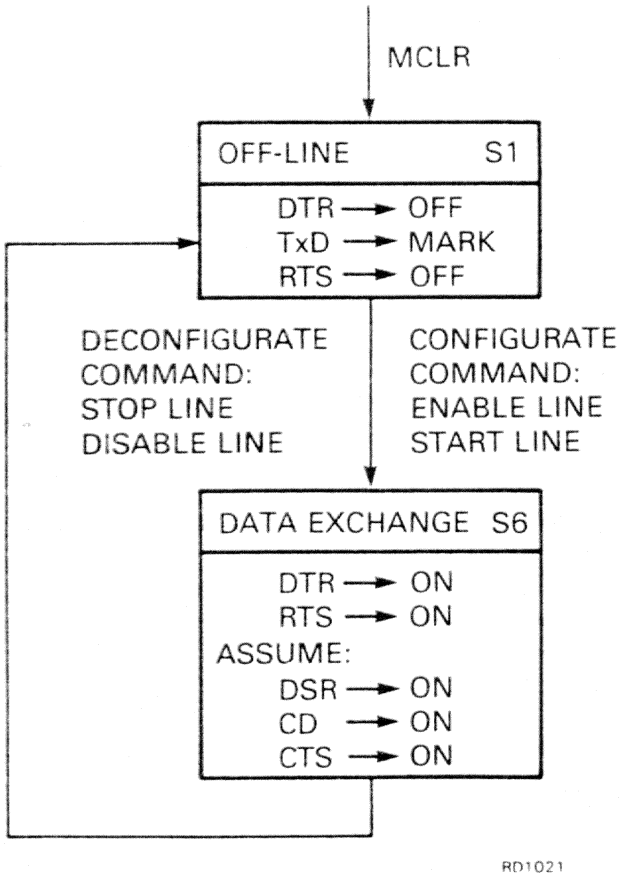


Figure A-5 Modem Control for Full Duplex, Data Leads Only

A.7.2 Modem Control for Full Duplex, Full Modem Control

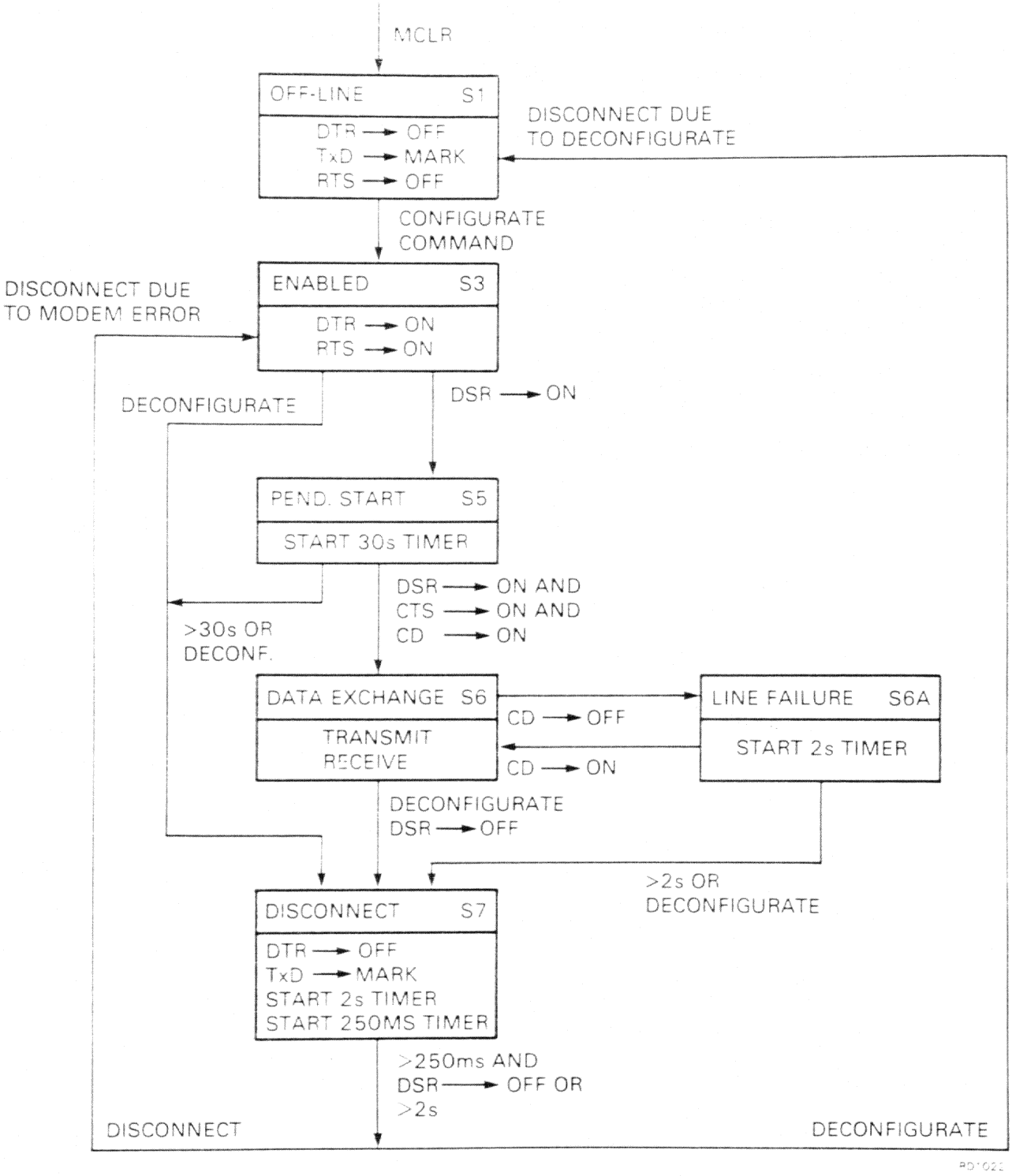


Figure A-6 Modem Control for Full Duplex, Full Modem Control

A.7.3 Configurate

This command is used to configurate the line and is performed once, usually at startup time. It informs the KMV11 of the frame protocol parameters and enables communications on the line.

A.7.3.1 Configurate Command

1. Command number: 1

2. Parameters

   a. BSEL4, BSEL5 and BSEL6 should contain the parameters as described in Figure A-7 and Table A-3.

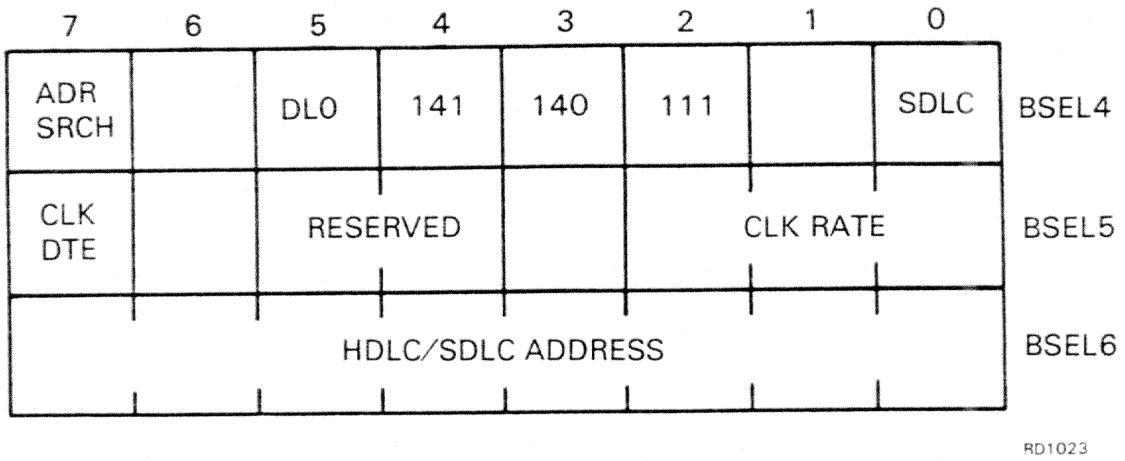


Figure A-7 Configurate Buffer

Table A-3 Configurate Buffer Bit Significance

Bit Name	Value	Function
SDLC	= 0	HDLC
	= 1	SDLC
DLO	= 0	Full modem control
	= 1	Data leads only: CCITT 107 (Data Set Ready), CCITT 109 (Carrier Detect), and CCITT 106 (Clear To Send) assumed to be on
111	= 1	Assert CCITT 111 (Data Signal Rate Selector (DTE))
141	= 1	Assert CCITT 141 (Local Loopback Request)
140	= 1	Assert CCITT 140 (Remote Loopback)
ADR-SRCH	= 0	All frames will be passed on reception
	= 1	Only frames with the indicated or a global address will be passed on reception.
CLK-DTE	= 0	clock source modem
	= 1	clock source internal

Table A-3 Configurate Buffer Bit Significance (Cont)

Bit Name	Value	Function
CLK-RATE		(only if CLK-DTE = 1)
	= 0	1.2 kbits/s
	= 1	2.4 kbits/s
	= 2	4.8 kbits/s
	= 3	9.6 kbits/s
	= 4	19.2 kbits/s
	= 5	48 kbits/s
	= 6	56 kbits/s *
	= 7	64 kbits/s

* 0.5% error

NOTE

72 kbits/s is available for diagnostic purposes only

HDLC/SDLC address = The address against which each received HDLC or SDLC frame address will be compared. If it matches, or the received address is global (377), the received frame will be passed to the host, otherwise the frame will be discarded.

A.7.3.2 Action – The KMV11 initializes all internal tables. It sets up the working mode according to the given parameters: mode and address. Data Terminal Ready (CCITT 108/2) and Request To Send (CCITT 105) will be set. The response will be generated when the line is in the data exchange state (S6) or when the modem does not respond.

A.7.3.3 **Configurate Response –**

1. Response number: 1
2. Possible status responses:
   a. Command correctly performed: 1 – When this response is sent, the line is ready to transfer data (Data Set Ready: CCITT 107, Clear to Send: CCITT 106, and Carrier Detect: CCITT 109 are on)
   b. Out of sequence: 371, if the line is already configured
   c. Modem down: 365, if there is no Carrier Detect within 30 seconds after Data Set Ready is turned on
   d. Double command: 363, if configuration is pending
   e. KMV11 resource error: 357, if there are no internal resources
   f. Deconfigurate pending: 356, if deconfiguration is pending.

A.7.4 Deconfigurate

This command stops the line from being scanned.

A.7.4.1 Deconfigurate Command –

1. Command number: 2

A.7.4.2 Action – All pending transmit and receive requests will be discarded. The modem control routine will force the line into the disconnect state (S7). Data Terminal Ready and Clear To Send will be dropped. If the Data Set Ready lead is turned off after 250 milliseconds, or if a timeout of 2 seconds occurs, the line will be placed in the off-line state (S1).

A.7.4.3 Deconfigurate Response –

1. Response number: 2

2. Possible status responses:

   a. Command correctly performed: 1
   b. Out of sequence: 371, if the line has not been configured
   c. Double command: 365, if deconfigurate is pending
   d. KV11 resource error: 357, if no internal resources are available.

A.7.5 Modem Change Response

A number of the modem leads from the DCE can be monitored for a change by means of the Enable Modem Survey (EMS) command. When a change occurs, the KMV11-A will generates a modem change response to inform the host.

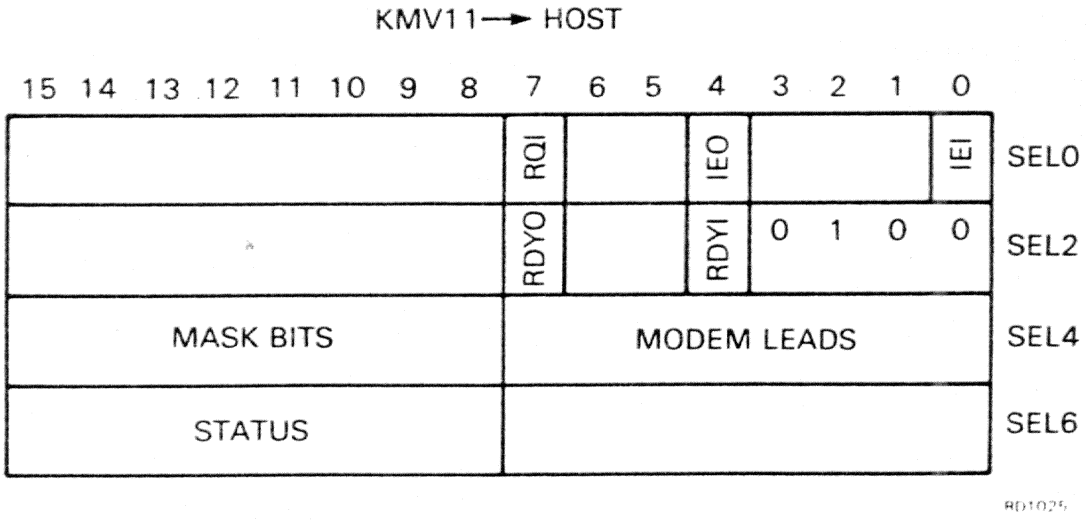


Figure A-8 Modem Change Response

A.7.5.1 Action – Any change in the modem leads defined in the EMS command mask will result in this asynchronous response. This means that each time a modem lead changes state, a response to the host will be generated. BSEL4 will contain the bit setting of the modem leads and BSEL5 a mask indicating which modem lead changed.

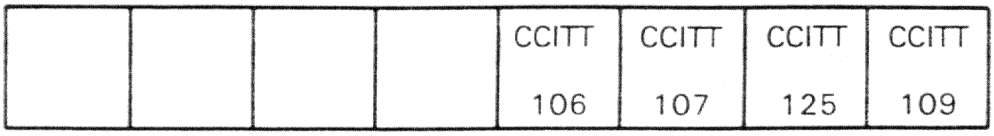


Figure A-9 Modem Change Response Mask Format

CCITT 109 = Carrier Detect
CCITT 125 = Ring Indicator
CCITT 107 = Data Set Ready
CCITT 106 = Clear To Send

A.7.5.2 **Modem Change Response –**

1. Response number: 4

2. Response parameter: (asynchronous only)

3. Possible status responses:

   a. Modem change: 1
   b. KMV11 resource error: 357, if no internal resources are available.

A.7.6 **Transmit Buffer**

This command is used to transmit a frame on the line. Up to two outstanding transmit buffers can be given.

A.7.6.1 **Transmit Buffer Command –**

1. Command number: 5

2. Parameters:

   a. Buffer address. This must be a 22-bit address in the host computer memory. Buffers may start on a byte boundary

   b. Byte count. This is the length of the buffer in bytes. The maximum byte count is 1032 bytes. This will allow a 3-byte HDLC header (extended control field), a 4-byte X.25 packet-level header (modulo 128), and a 1024 byte data field.

A.7.6.2 **Action –** The buffer parameters are stored and the frame will be transmitted according to the selected frame protocol. The buffer contains the information field of the frame to be transmitted. The FCS (Frame Check Sequence) is added by the KMV11. The frames are transmitted in the same order as they have been given by the user program. Do not overwrite the buffer contents before the KMV11 has returned a transmit buffer response.

A.7.6.3 **Transmit Buffer Response –**

1. Response number: 5

2. Possible status responses:

   a. Command correctly performed: 1

b. Nonexistent buffer memory: 374, when there is a failure in the host computer memory or an error in the buffer address. All pending transmit buffers (for the line) are lost. This error is not reported until the KMV11 accesses the buffer for data transmission

c. Frame length error: 372, when the frame is too short. A frame should be at least two bytes long

d Out of sequence: 371, when the line has not been configurated

e. Latency error: 370, when the KMV11 could not fetch the next byte from the buffer in time

f. Modem down: 365, if, during the transmit, Data Set Ready (CCITT 107) is turned off or Carrier Detect (CCITT 109) is off for more than two seconds

g. Too many buffers: 360, when two buffers have already been issued to the line. The last given buffer is not accepted, two being the maximum number of buffers

h. Buffer overflow: 373, if the frame is longer than 1032 bytes

i. KMV11 resource error: 357, if no internal resources are available.

A.7.7 Receive Buffer

This command is used to pass a buffer address to the KMV11 as a storage area for received frames from the other station. Up to two outstanding receive buffers can be given.

A.7.7.1 Receive Buffer Command –

1. Command number: 6

2. Parameters:

   a. Buffer address. This is a 22-bit address in the host computer memory. The buffer may start on a byte boundary.

   b. Byte count. This is the length of the buffer in bytes.

A.7.7.2 Action – The buffer parameters are stored and the buffer will be used as a storage area when a frame is received from the other station. The information field of the received frame will be directly loaded into the buffer. The FCS is removed by the KMV11. The transfer is considered to be completed when the FCS is received correctly. The buffers are loaded with data in the same order as they have been given by the user program.

A.7.7.3 Receive Buffer Response –

1. Response number: 6

2. Response parameter:

   a. Byte count. The byte count is the length of the received frame without the FCS.

3. Possible status responses:

   a. Command correctly performed: 1. This status is returned each time a frame is received correctly. The latency between the user program command and the KMV11 response is undefined, because it depends on the other station and the transmission speed.

   b. Nonexistent memory buffer: 374, when there is a failure in the host computer memory or an error in the buffer address. All the pending receive buffers for the line are lost. This error is not reported until the KMV11 accesses the buffer on data transfer.

   c. Buffer overflow: 373, when the received information field is longer than the buffer size. The data is valid up to the end of the buffer. The FCS at the end of the frame was correct.

   d. Out of sequence: 371, when the line has not been configurated.

   e. Latency error: 370, when the KMV11 could not store the data byte in time in the host memory buffer because of Q-bus delays.

   f. FCS error: 367.

   g. Modem down: 365, if, during the receive, Data Set Ready (CCITT 107) is turned off or Carrier Detect (CCITT 109) is off for more than two seconds.

   h. Abort received: 364, when an abort frame is received.

   i. Too many buffers: 360, when two buffers are already waiting for reception on the line. The last given buffer is not accepted.

   j. KMV11 resource error: 357, if no internal resources are available.

A.7.8 Transmit Abort

Data transmission from the activated transmit buffer is stopped. Transmit buffers waiting for the line are lost.

A.7.8.1 Transmit Abort Command –

1. Command number: 7

A.7.8.2 Action – If a frame is being transmitted it is aborted. Transmit buffers for the line are lost.

A.7.8.3 Transmit Abort Response –

1. Response number: 7

2. Possible status responses:

   a. Command correctly performed: 1. The latency between the user program command and the KMV11 response is less than 500 milliseconds.

   b. Out of sequence: 371, the KMV11 firmware has not been configured

   c. KMV11 resource error: 357, if no internal resources are available.

A.7.9 Receive Abort

Data transfer into the active receive buffer is stopped. Receive buffers for the line are lost.

A.7.9.1 Receive Abort Command –

1. Command number: 10

A.7.9.2 Action – If a frame is being received, data transfer into the buffer is stopped. Receive buffers for the line are lost.

A.7.9.3 Receive Abort Response –

1. Response number: 10
2. Possible status responses:
   a. Command correctly performed: 1. The latency between the user program command and the KMV11 response is less than 500 milliseconds.
   b. Out of sequence: 371, if not configured.
   c. KMV11 resource error: 357, if no internal resources are available.

A.7.10 Read Modem

This command is used to get the status of the DCE-controlled modem leads, and the state of the line.

A.7.10.1 Read Modem Command –

1. Command number: 14

A.7.10.2 Action – The following modem leads will be read and placed in the BSEL4 byte.

		CCITT 142	CCITT 112	CCITT 106	CCITT 107	CCITT 125	CCITT 109

RD1026

Figure A-10 BSEL4 Significance Following Read Modem Command

CCITT 109 = Carrier Detect
CCITT 125 = Ring Indicator
CCITT 107 = Data Set Ready
CCITT 106 = Clear To Send
CCITT 112 = Data Signal Rate Selector (DCE)
CCITT 142 = Test Indicator

The state of the line will be placed in BSEL5:

- Off-line = 0 (S1)
- Line enabled = 1 (S3)
- Pending start = 2 (S5)
- Data exchange = 3 (S6)
- Line fault = 4 (S6A)
- Line disconnect = 5 (S7A)
- Line deconfigurate = 6 (S7B)

A.7.10.3 Read Modem Response –

1. Response number: 14

2. Possible status responses:

   a. Command correctly performed: 1.

   b. Out of sequence: 371, if the KMV11 is not configured and also if configurate is not waiting.

   c. KMV11 resource error: 357, if no internal resources are available.

A.7.11 Enable Modem Survey

A number of modem leads from the DCE can be monitored for a change. The read modem command only gives the status at a specific point in time.

A.7.11.1 Enable Modem Survey Command –

1. Command number: 16

2. Parameters:

   a. BSEL3 must contain a mask for the modem leads to be monitored. Organization of the byte is the same as for the data set change bitmap.

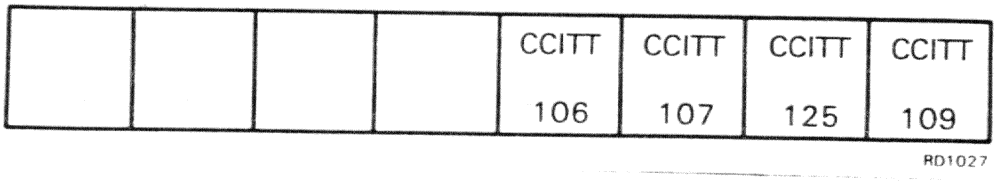


Figure A-11 BSEL3 Modem lead mask

CCITT 109 = Carrier Detect
CCITT 125 = Ring Indicator
CCITT 107 = Data Set Ready
CCITT 106 = Clear To Send

A.7.11.2 Action – After reception of the survey start command, a response is returned to indicate acceptance of the command. The current status of the modem leads is returned in BSEL4, including CCITT 112 and CCITT 142 status as in the read modem response. Any change in the modem leads defined in the enable command mask will result in an asynchronous modem change response (4). This means that each time a modem lead changes state and the KMV11 is configured, a response to the host will be generated.

A.7.11.3 Enable Modem Survey Response –

1. Response number: 16

2. Possible status responses:

   a. Command correctly performed: 1.
   b. Double command: 363, if a modem survey is already enabled.
   c. KMV11 resource error: 357, if no internal resources are available.

A.7.12 Disable Modem Survey
Stop the survey of the modem leads.

A.7.12.1 Disable Modem Survey Command –

1. Command number: 17

A.7.12.2 Action – Stop the survey of the modem leads.

A.7.12.3 Disable Modem Survey Response –

1. Response number: 17

2. Possible status responses:

   a. Command correctly performed: 1.
   b. Double command: 363, if the modem survey is already disabled.
   c. KMV11 resource error: 357, if no internal resources are available.

A.7.13 Dummy Command
These commands are without effect on the KMV11. They are not acknowledged.

A.7.13.1 Dummy Command –

1. Command number (octal): 0, 3, 11, 12, 13, 15

A.7.13.2 Action – None.

A.7.13.3 Dummy Response – No response is given to a dummy command, except that of KMV11 resource error (code: 357, no internal resources available).

A.8 KMV11-A COMMAND AND RESPONSE FORMAT

HOST → KMV11

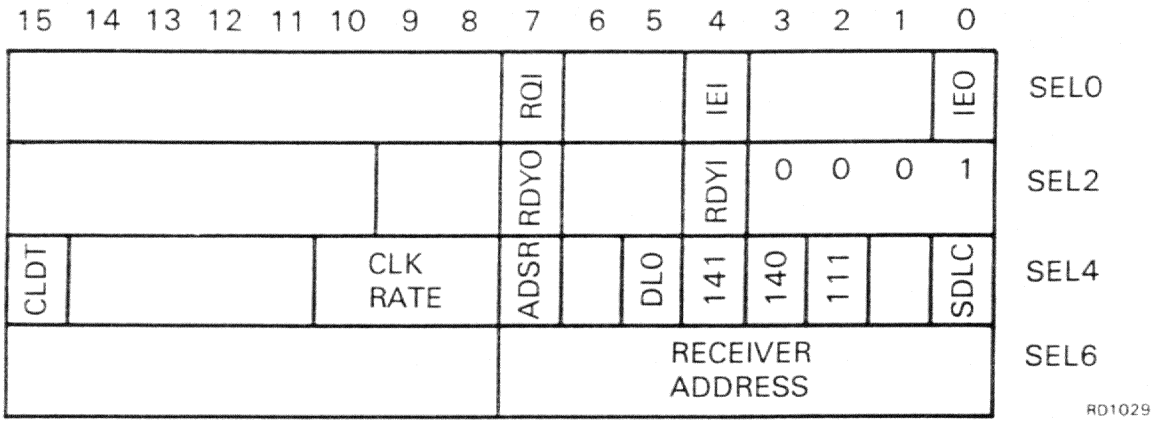


Figure A-12 Configurate Command

KMV11 → HOST

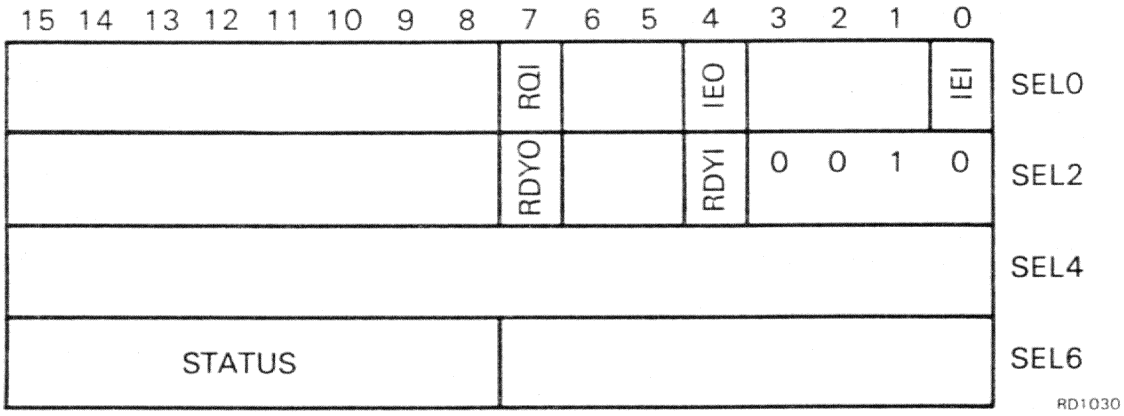


Figure A-13 Configurate Response

HOST → KMV11

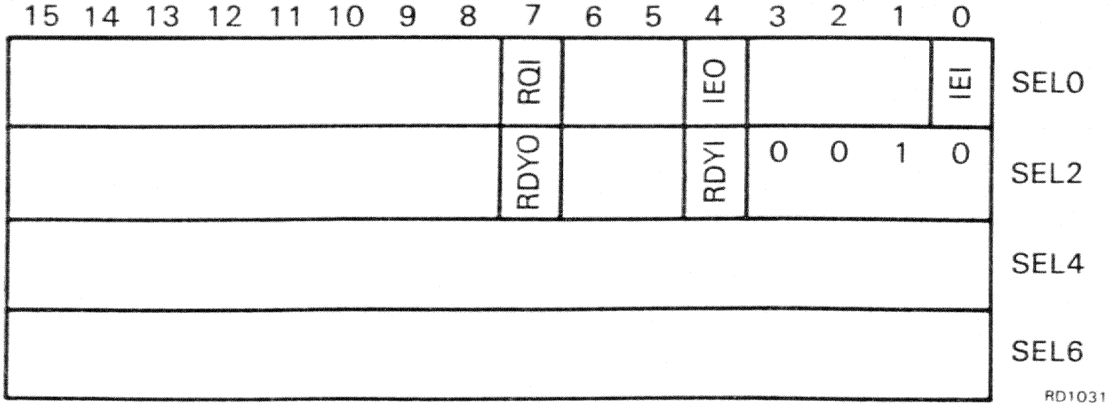


Figure A-14 Deconfigurate Command

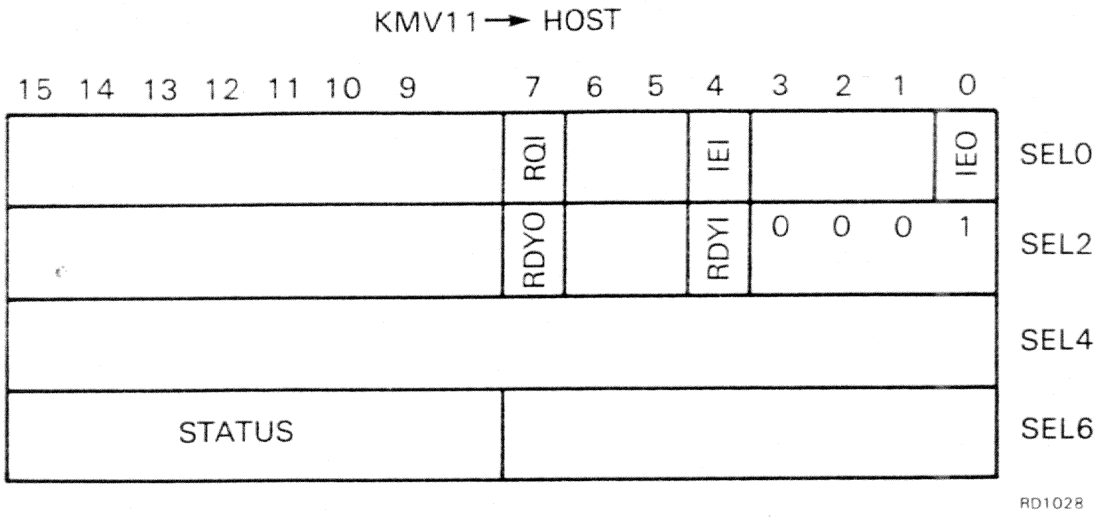


Figure A-15 Deconfigurate Response

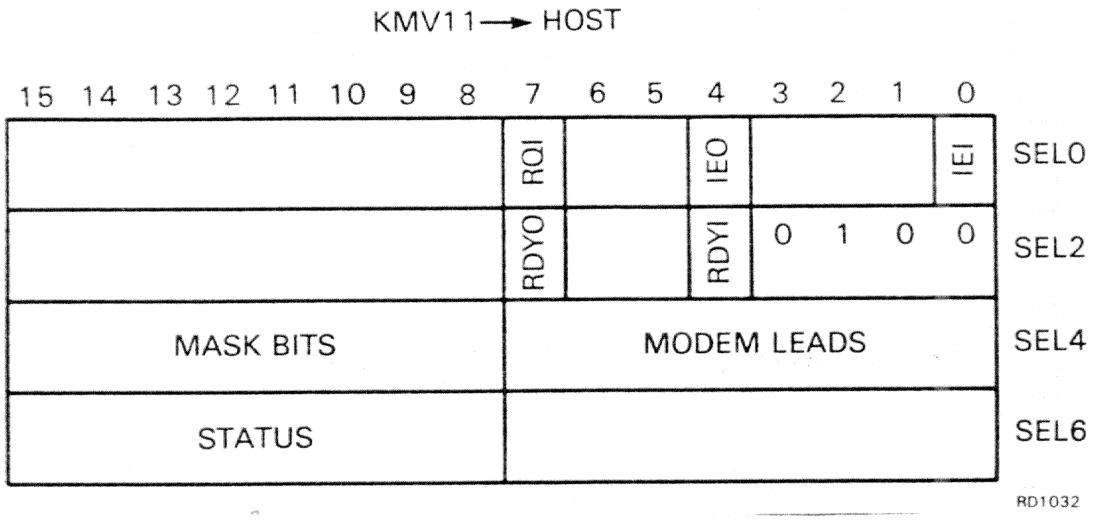


Figure A-16 Modem Change Response

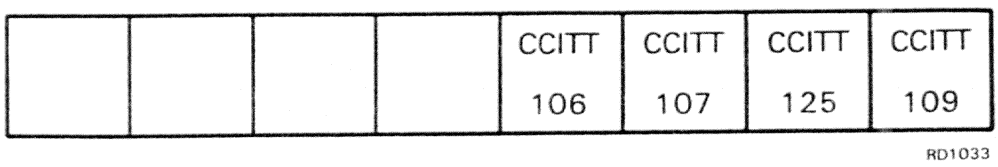


Figure A-17 Modem Change Response Mask Format

CCITT 109 = Carrier Detect
CCITT 125 = Ring Indicator
CCITT 107 = Data Set Ready
CCITT 106 = Clear To Send

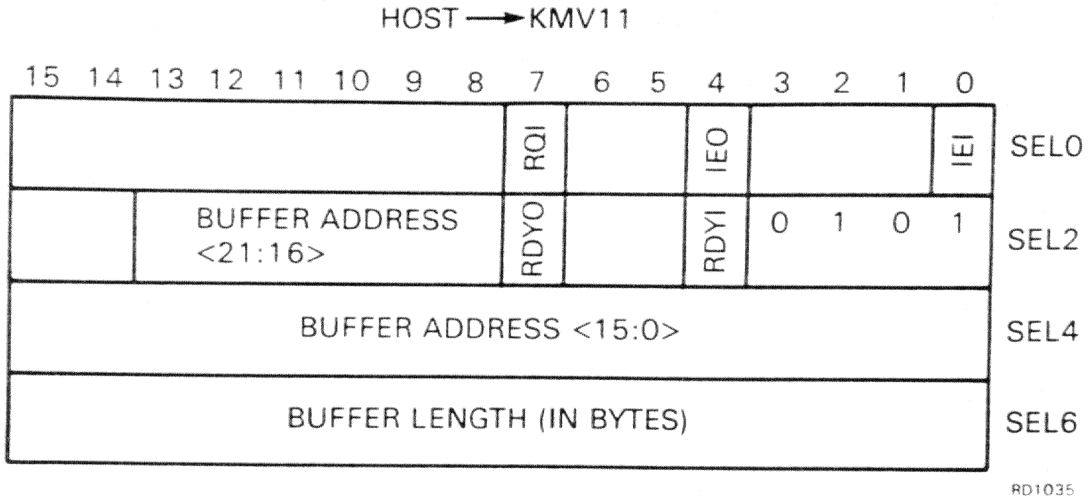


Figure A-18 Transmission Buffer Command

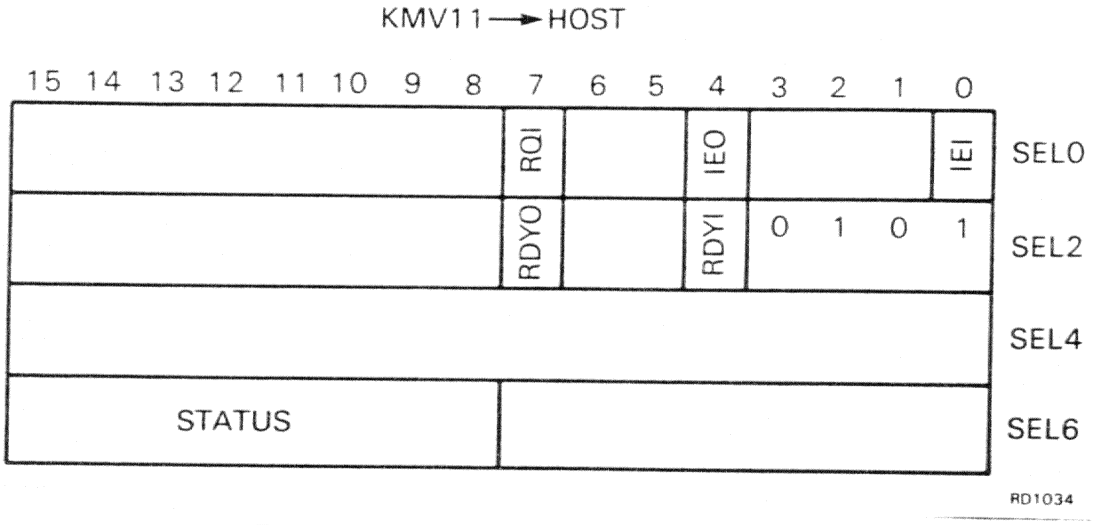


Figure A-19 Transmission Buffer Response

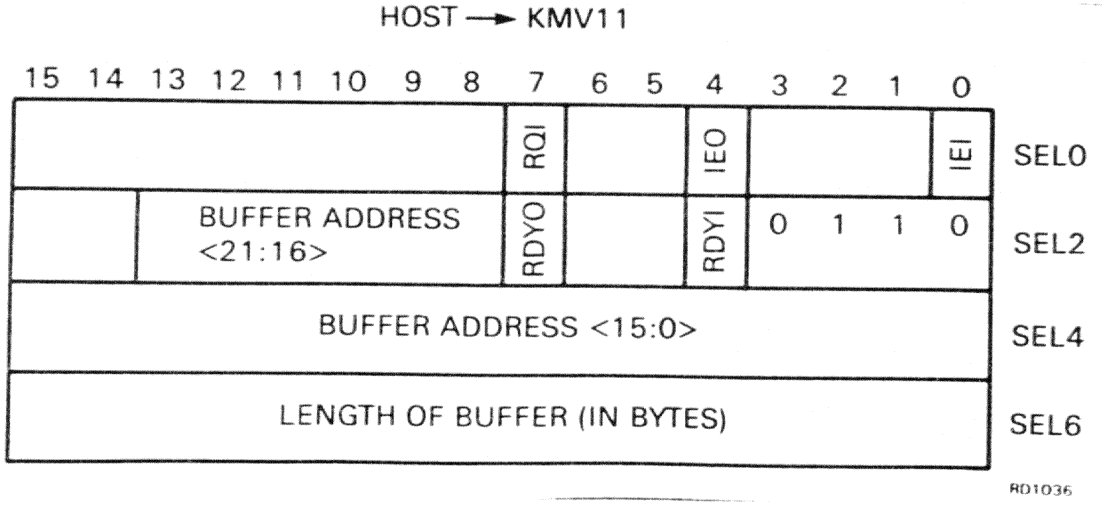


Figure A-20 Reception Buffer Command

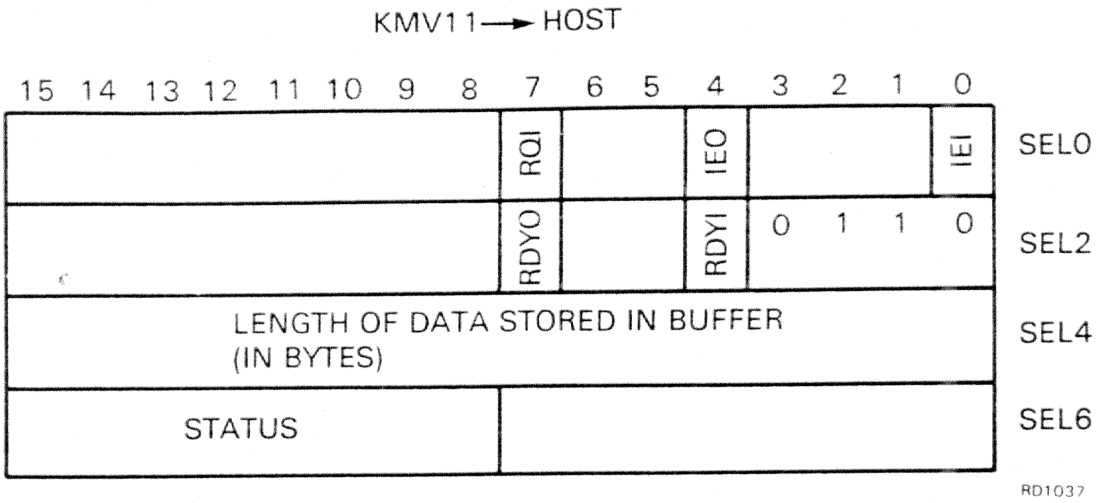


Figure A-21 Reception Buffer Response

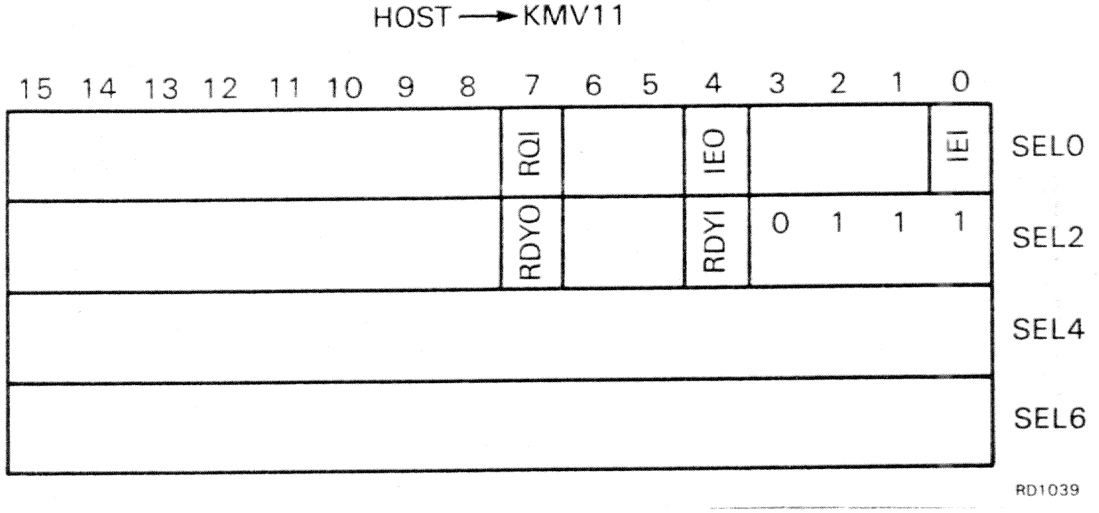


Figure A-22 Transmit Abort Command

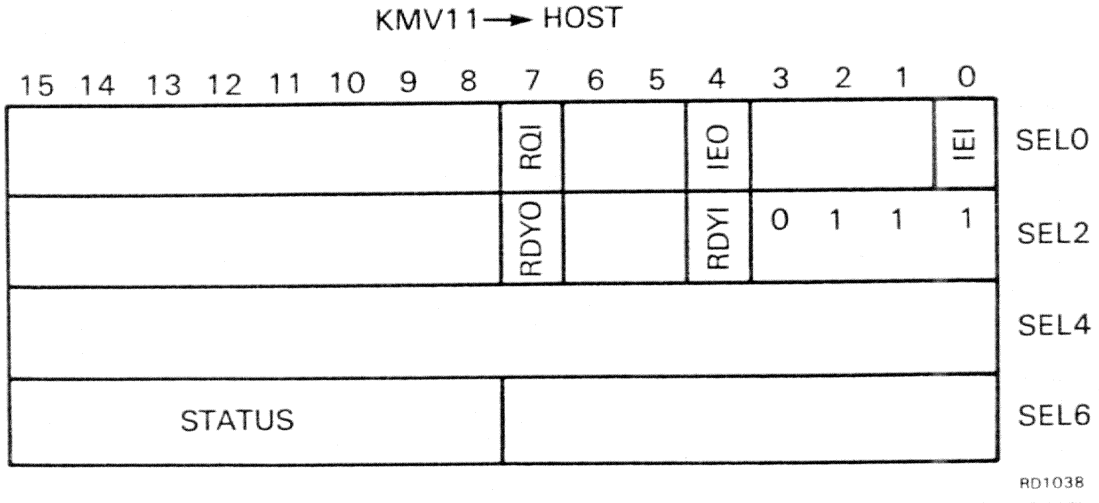


Figure A-23 Transmit Abort Response

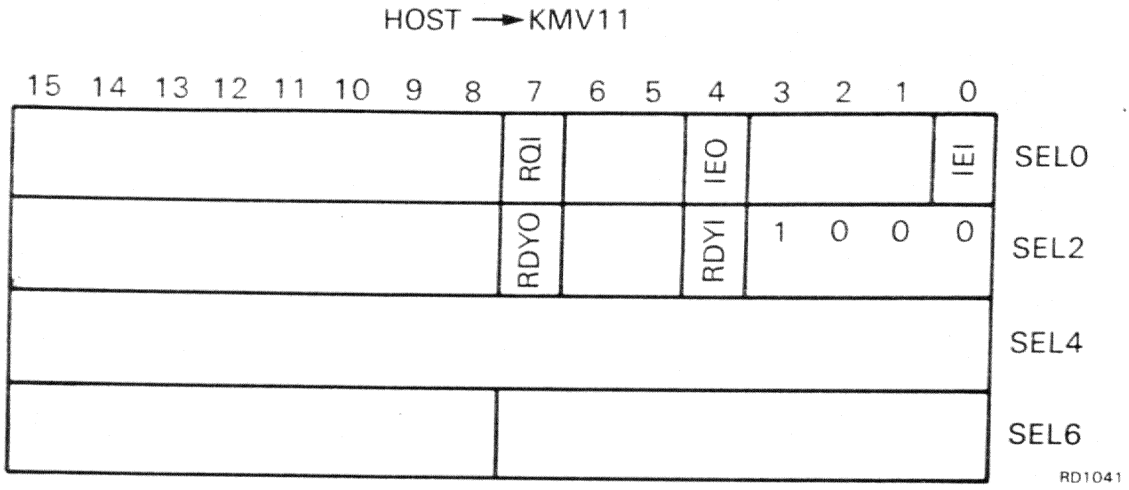


Figure A-24 Receive Abort Command

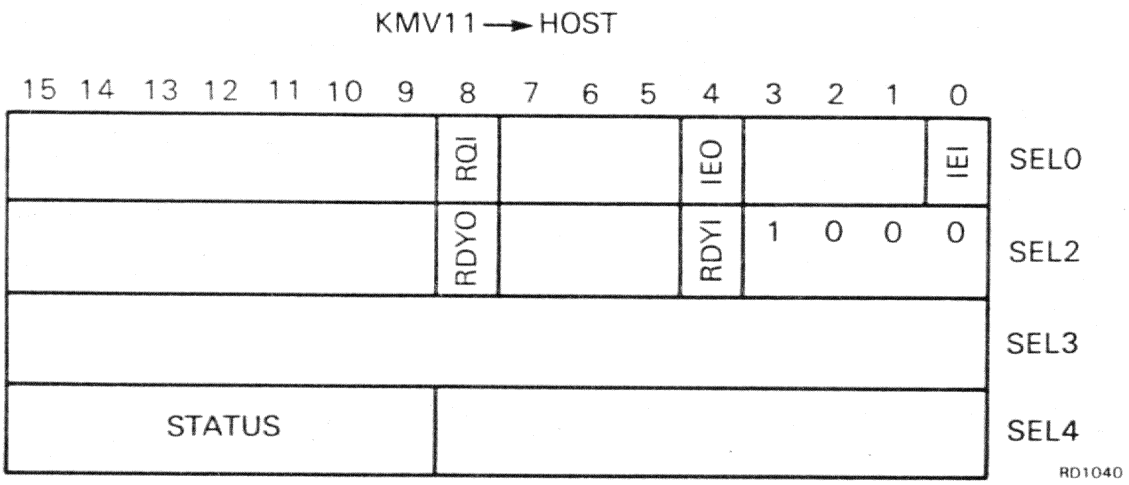


Figure A-25 Receive Abort Response

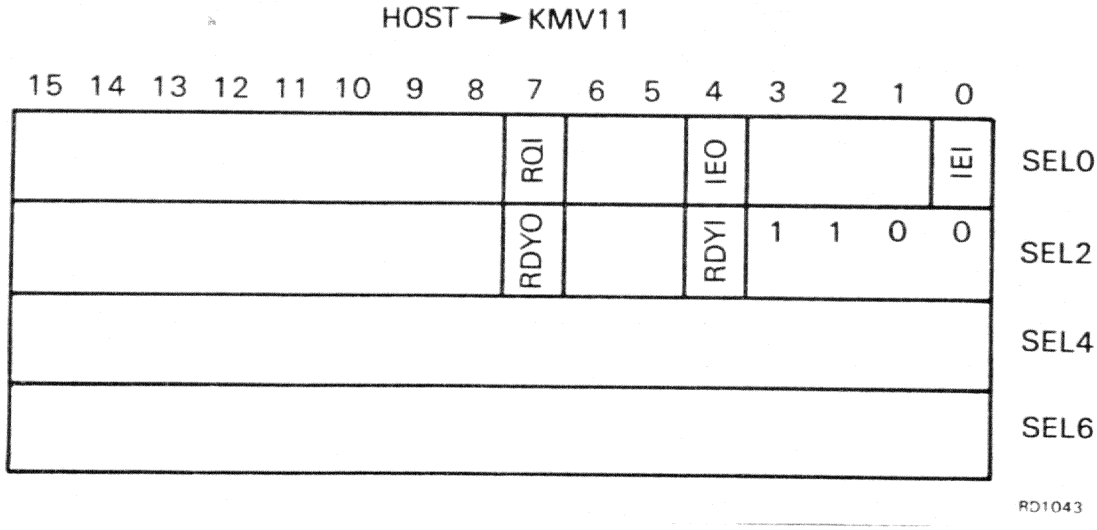


Figure A-26 Read Modem Command

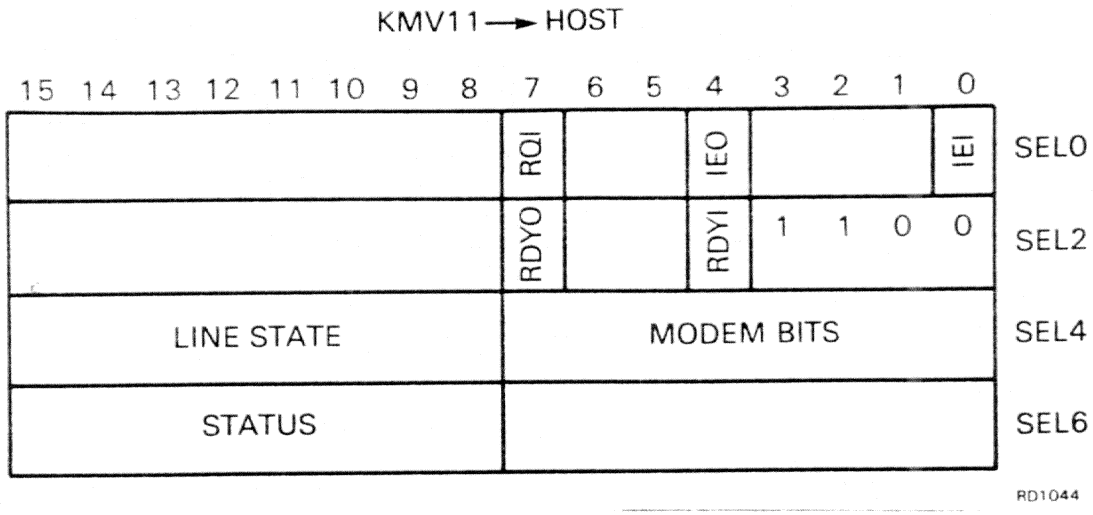


Figure A-27 Read Modem Response

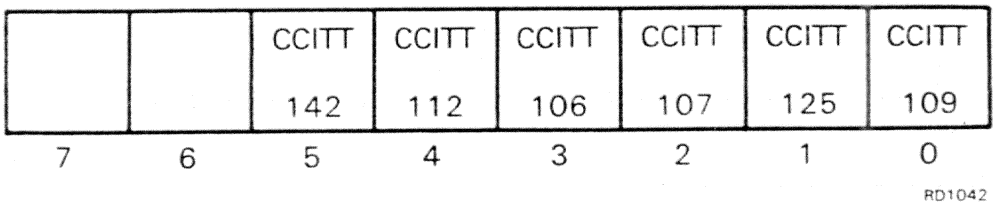


Figure A-28 Returned Modem Bits

CCITT 109 = Carrier Detect
CCITT 125 = Ring Indicator
CCITT 107 = Data Set Ready
CCITT 106 = Clear To Send
CCITT 112 = Data Signal Rate Selector (DCE)
CCITT 142 = Test Indicator

Returned line states:

0 = off-line (S1)
1 = line enabled (S3)
2 = pending start (S5)
3 = data exchange (S6)
4 = line fault (S6A)
5 = line disconnect (S7A)
6 = line deconfigurate (S7B)

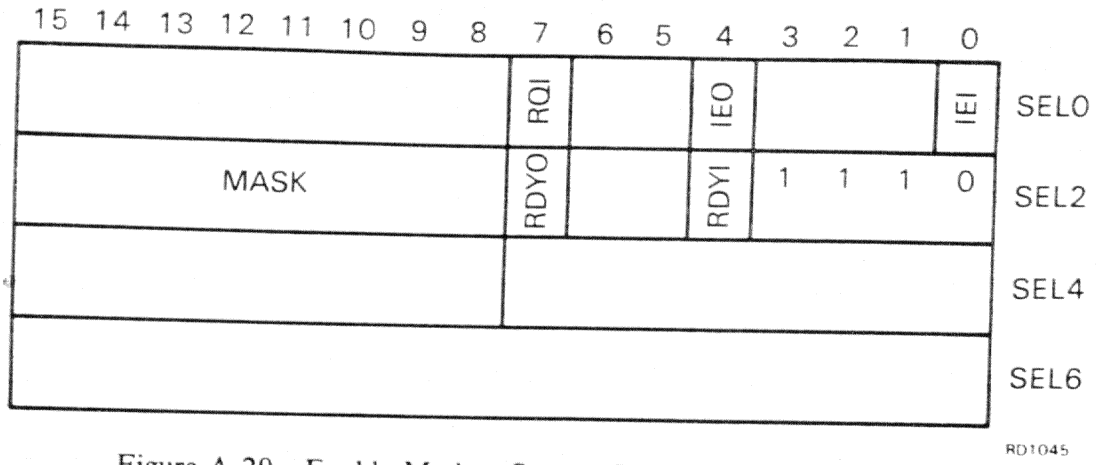


Figure A-29 Enable Modem Survey Command, Host to KMV11

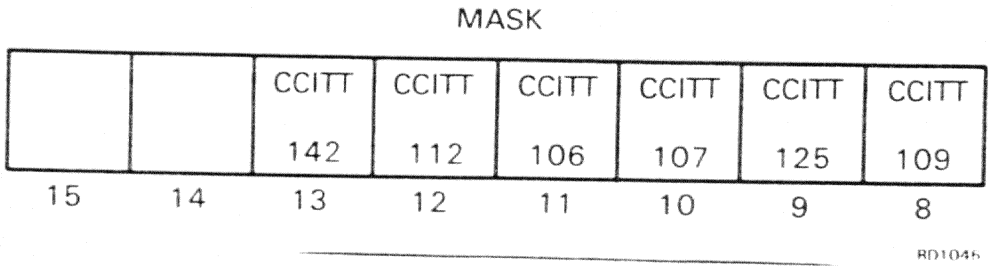


Figure A-30 Modem Bits To Be Checked

CCITT 109 = Carrier Detect
CCITT 125 = Ring Indicator
CCITT 107 = Data Set Ready
CCITT 106 = Clear To Send
CCITT 112 = Data Signal Rate Selector (DCE)
CCITT 142 = Test Indicator

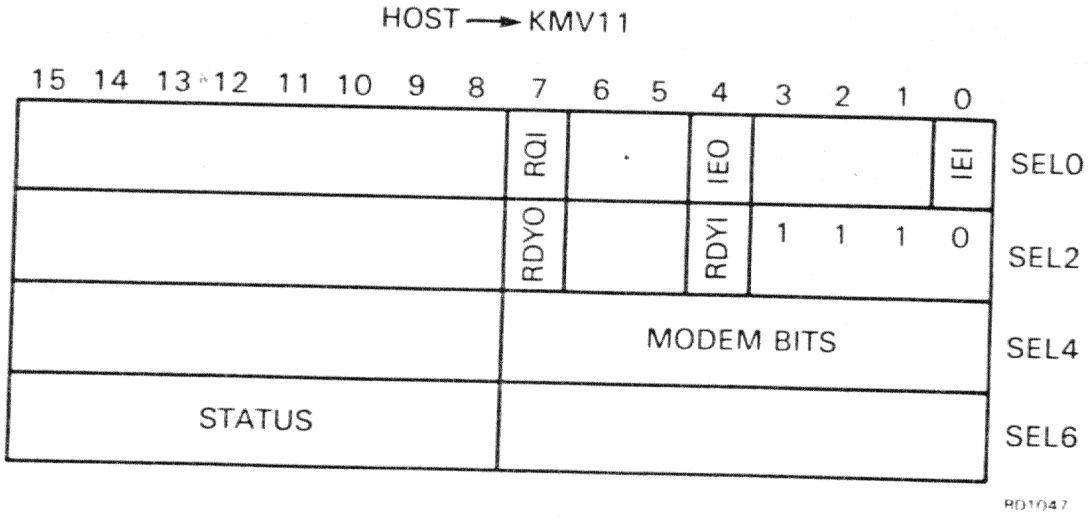


Figure A-31 Enable Modem Survey Response

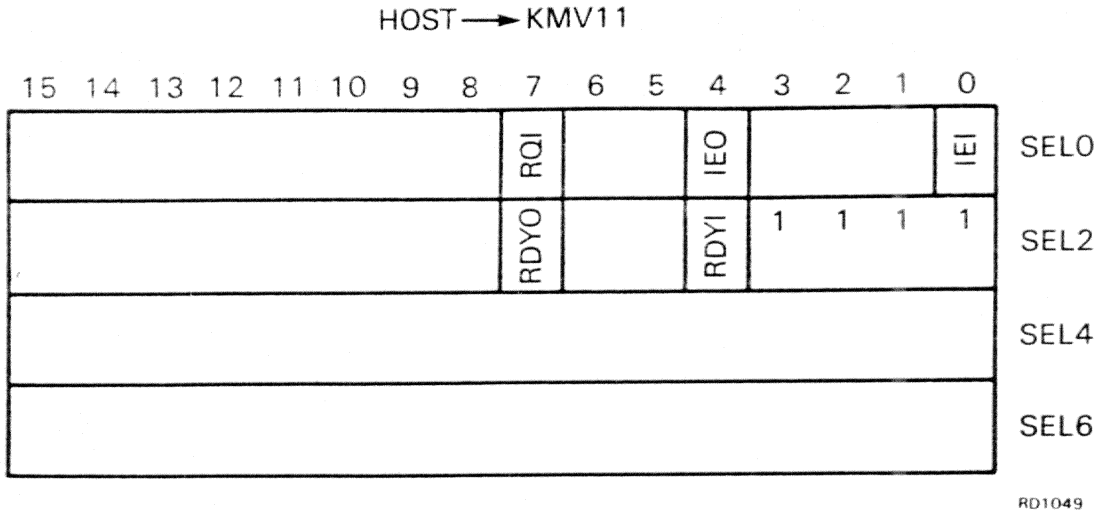


Figure A-32 Disable Modem Survey Command

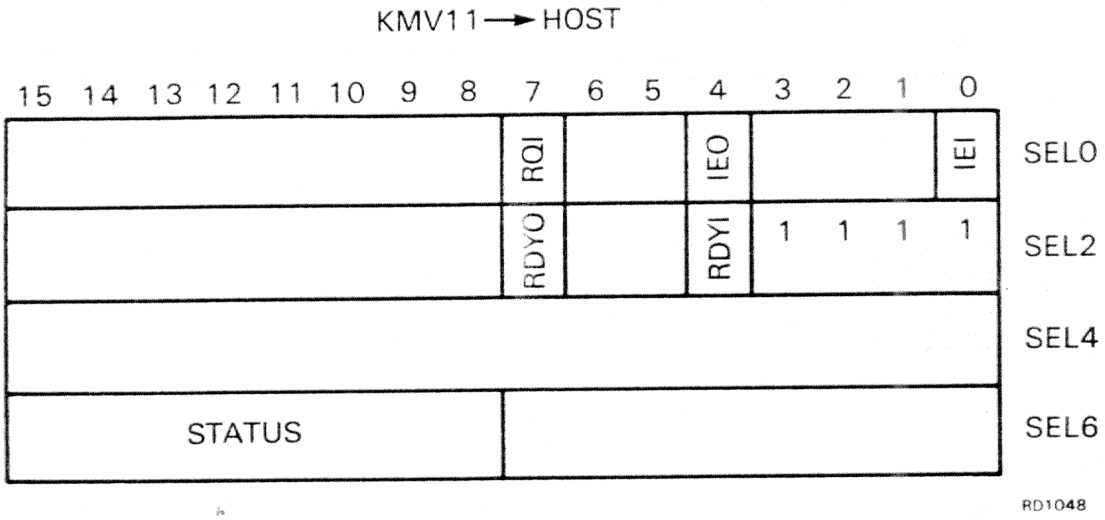


Figure A-33 Disable Modem Survey Response

A.9 KMV11-A POSSIBLE STATUS RETURNS

Table A-4 KMV11-A Possible Status Returns

	Configurate 1	Deconfigurate 2	Modem Change 4	Transmit Buffer 5	Receive Buffer 6	Transmit Abort 7	Receive Abort 10	Read Modem 14	Enable Modem Survey 16	Disable Modem Survey 17	Dummy
Command correctly performed(1)	•	•	•	•	•	•	•	•	•	•	
Nonexistent buffer memory(374)				•	•						
Buffer overflow (373)				•	•						
Frame length error (372)				•							
Out of sequence (371)	•	•		•	•	•	•	•			
Latency error (370)				•	•						
FCS error (367)					•						
Modem down (365)	•			•	•						
Abort received (364)					•						
Double command (363)	•	•							•	•	
Too many buffers (360)				•	•						
KMV11 resource error (357)	•	•	•	•	•	•	•	•	•	•	•
Deconfigurate pending (356)	•										

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