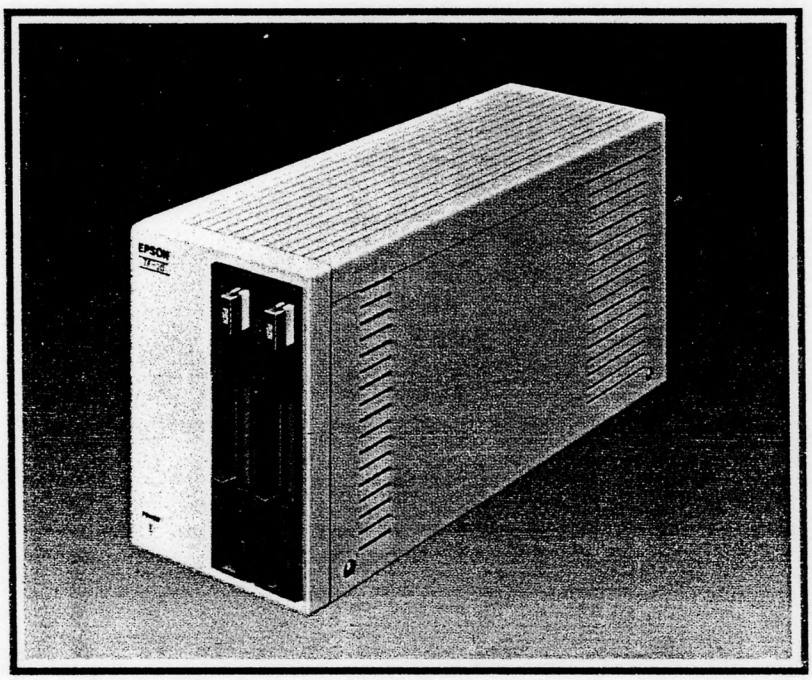
EPSON TERMINAL FLOPPY

TF-20

TECHNICAL MANUAL



EPSON

F8380010-0

This Technical Manual provides technical information on the structure, maintenance, and repairs of the EPSON TERMINAL FLOPPY TF-20.

Major technical modifications, if made in the future, will be notified through Service Bullentins, and the Technical Manual should be revised accordingly. The details of the Manual are subject to change without notice.

All the information given in the Manual concerns the TF-20, and we are not responsible for any troubles with the industrial copyright of a third party that might arise from your application or connection of the TF-20 to other products.

CHAPTER 4 HX-20 FACTORY OPTION

CHAPTER 1 GENERAL

1.1 Features of TF-20

The TF-20 is a compact terminal floppy disk drive unit incorporating two ultra-thin 5.25-inch floppy disk drives.
It is a fruit of EPSON's unrelenting efforts in pursuit of miniaturization, light weight and high performance.
The TF-20 will thus display its intended performance fully, used in linkage with various computers. It can also have "factory option" interface boards to permit its connection to any of the computers which are provided with various interfaces. Merely adding these optional interface boards to the TF-20 will make desired data transfer possible between the computer and the TF-20.

1.2 Factory Option

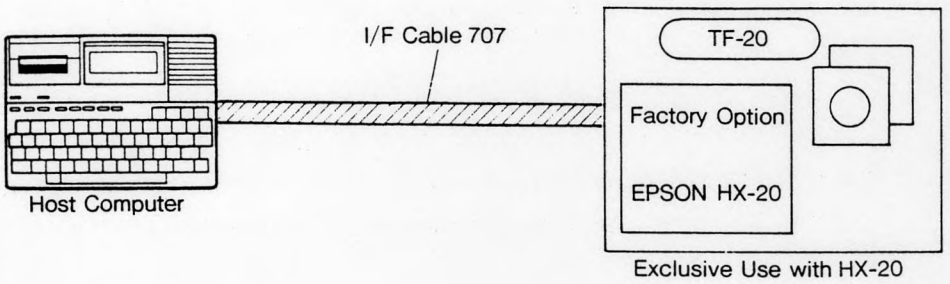
The standard TF-20 comprises the power circuit and two 5.25-inch floppy disk drives with the interface compatible with Shugart's SA450(U.S.A.). In addition, the TF-20 can be an exclusive-use floppy disk drive unit with the following factory option board incorporated in it. The factory option unit, however, can not be added or remodeled once the TF-20 is shipped from the factory.
HX-20 Factory Option:
With this factory option incorporated, the TF-20 becomes an intelligent type of exclusive-use terminal floppy for the HX-20, having the CPU, I/O, 64 KB memory and high-speed serial interface within it.

1.3 Serviceability

The TF-20 has been designed to minimize maintenance and repair in its normal use.
Should maintenance or repair be required, the floppy disk drive mechanism and circuit boards of the TF-20 are readily replaceable. Therefore, the user can perform maintenance and repair quite easily by referring to this manual.

1.4 Connection of TF-20 with Personal Computer

Connection with the EPSON HX-20



1.5 General Specifications of TF-20 (Standard)

(1) Memory capacity (unformat)

Memory capacity per unit: 1000 KB(double density recording)
: 500 KB(single density recording)

(2) Memory system (format, double-side double-density recording)
Memory capacity per unit: 656 KB
Memory capacity per drive: 328 KB
No. of tracks per drive: 80 tracks
No. of sectors per track: 16 sectors
Memory capacity per sector: 256 B

(3) Memory density: 5876 BPI

(4) Data transfer speed: 250 Kbits/sec

(5) Av. track rotation waiting time: 100 msec

(6) Access time
Inter-track access time: 15 msec
Av. inter-track transfer access time: 220 msec
Settling time: 15 msec

(7) Head loading time: 35 msec

(8) Motor start time: 0.5 sec

(9) Motor speed: 300 r.p.m.

(10) R/W head positioning system: Voice coil motor system

(11) Disk drive motor: Outer rotor type brushless transistor motor

(12) Power supply
Voltage: AC115/220/240V
Frequency: 49.5 to 60.5 Hz
Power consumption: 40W

(13) Dimensions
Width: 120 mm
Depth: 350 mm
Height: 165 mm

(14) Weight: 6 kg

(15) Ambient conditions
Temperature (operating): 5° C to 30° C
(non-operating): −30° C to 65° C
Relative humidity (operating): 20% to 80% (no condensation)
(non-operating): 5% to 85% (no condensation)

Shock resistance (operating): 1G for 1ms maximum

(non-operating): 2G for 1ms maximum

Vibration resistance

(operating): No R/W error at 0.6G, 5 to 60Hz

(non-operating): No abnormality at 1.0G, 5 to 60Hz

(16) Insulation resistance/strength

Insulation resistance: 10MΩ min. between AC power supply and case

Insulation strength: Can withstand 1kV (R.M.S.) 50/60Hz applied between AC power supply and case for a minute.

1.6 Timings of Interface Signals of TF-20 (Standard)

(1) Power up mode

The READY signal becomes "LOW" when the INDEX pulse is counted four times or more in one second with the disk rotating, and the Seek and R/W operation become possible.

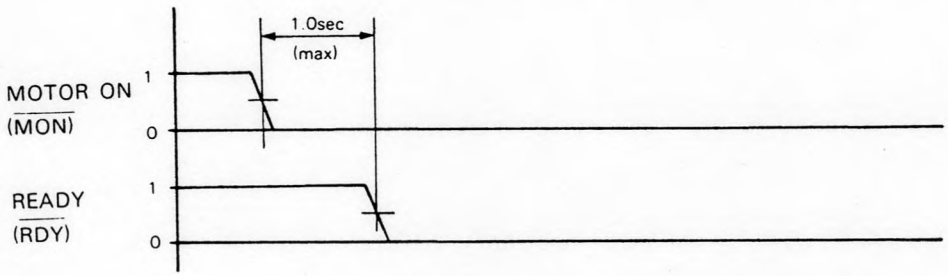


Fig. 1-1 Power Up Timing

(2) Track transfer time

By inputting the "LOW" pulse to the STEP (STP) signal line, the read/write head positioning voice coil motor can be driven in the moving direction specified by the DRTN signal.

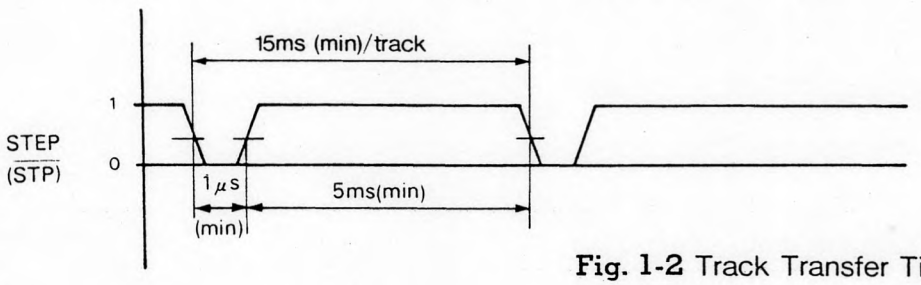


Fig. 1-2 Track Transfer Timing

(3) Seek operation

This is the action timing for moving the magnetic head to the desired track. For a Seek operation, select a drive, set the DIRECTION signal for "LOW" or "HIGH" (specification of direction), then give pulses corresponding to the number of tracks for transfer from the present position to the STEP signal, and the magnetic head is set properly on the specified track.

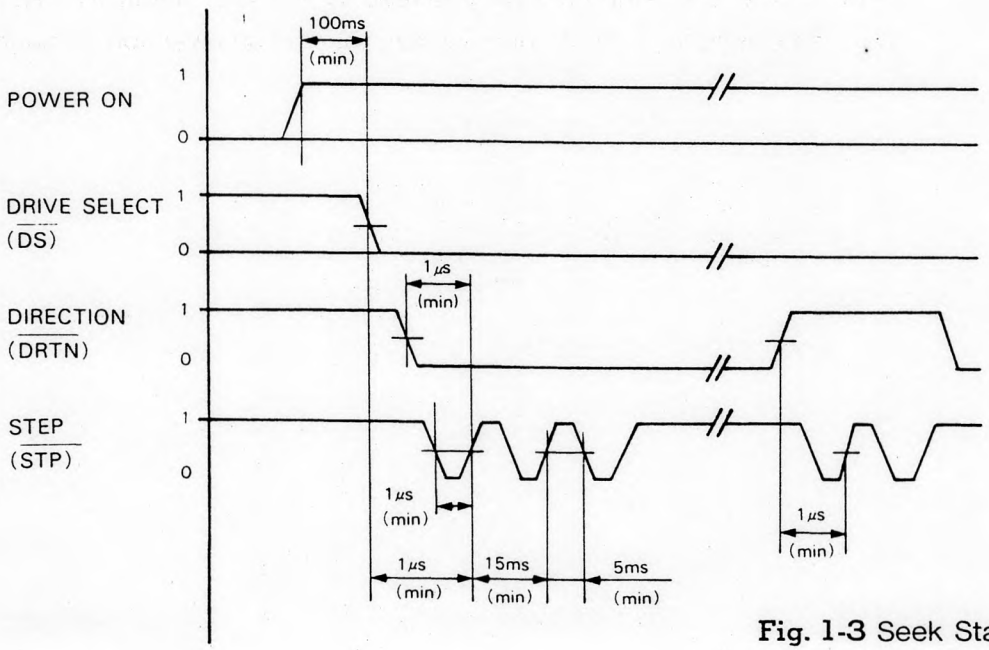


Fig. 1-3 Seek Start Timing

(4) Road Operation

In this mode, data written in the disk is read out. For a Read operation, make certain that the READY signal is "LOW", and select the drive to be used.

Then set the HEAD LOAD signal for "LOW" and specify Side 0 or 1 by the SIDE SELECT signal.

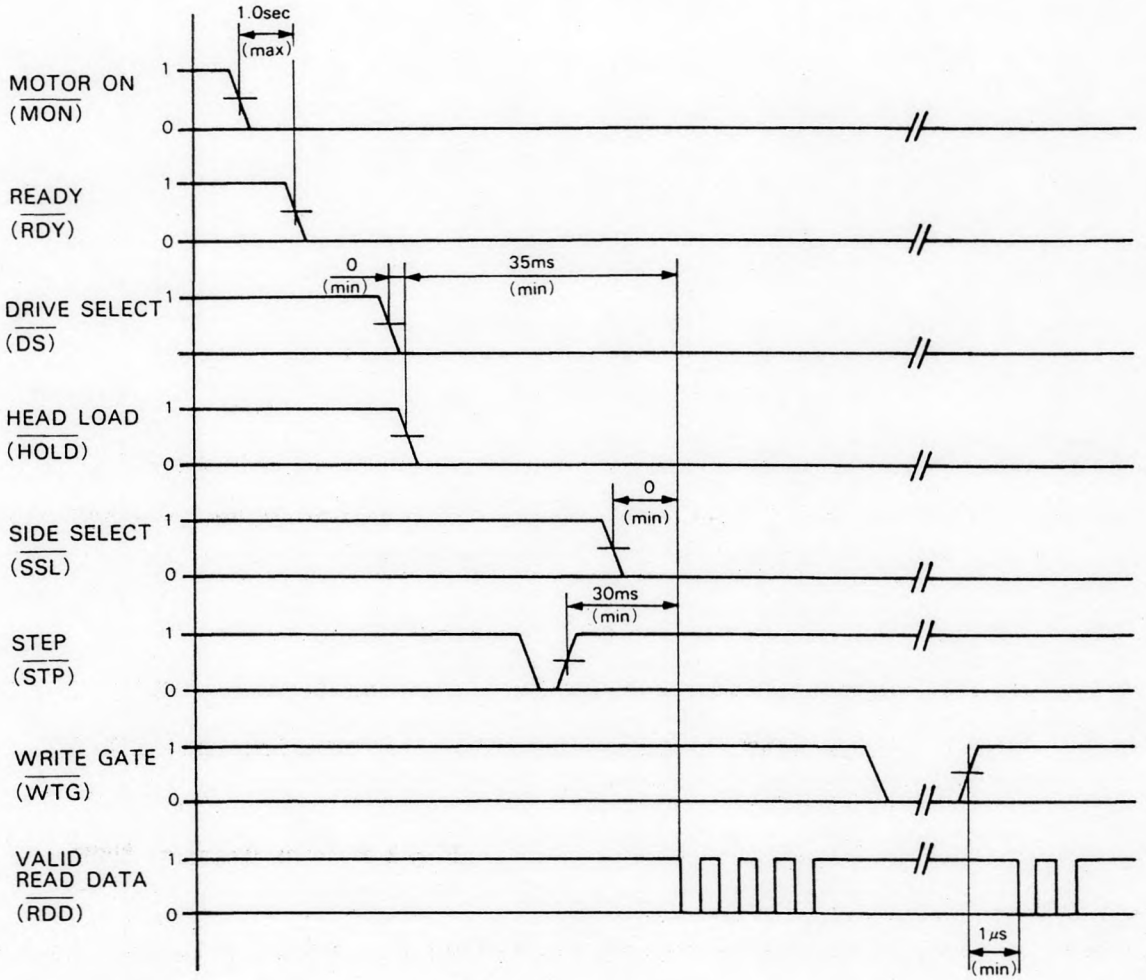


Fig. 1-4 Read Start Timing

The read data to be output is a pulse string of raw data read by the read circuit. The READ DATA signal is normally "HIGH", and outputs a "LOW" pulse where there is an inversion of magnetization on the disk.

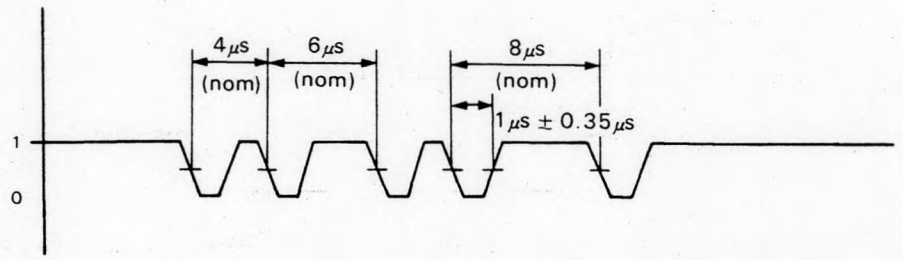


Fig. 1-5 Read Data Timing MFM System

(5) Write operation

In this mode, data is written into the disk. For a Write operation, operate from the READY signal to the SIDE SELECT signal the same way as explained in "Read operation". Then set the WRITE GATE signal for "LOW" and send write data.

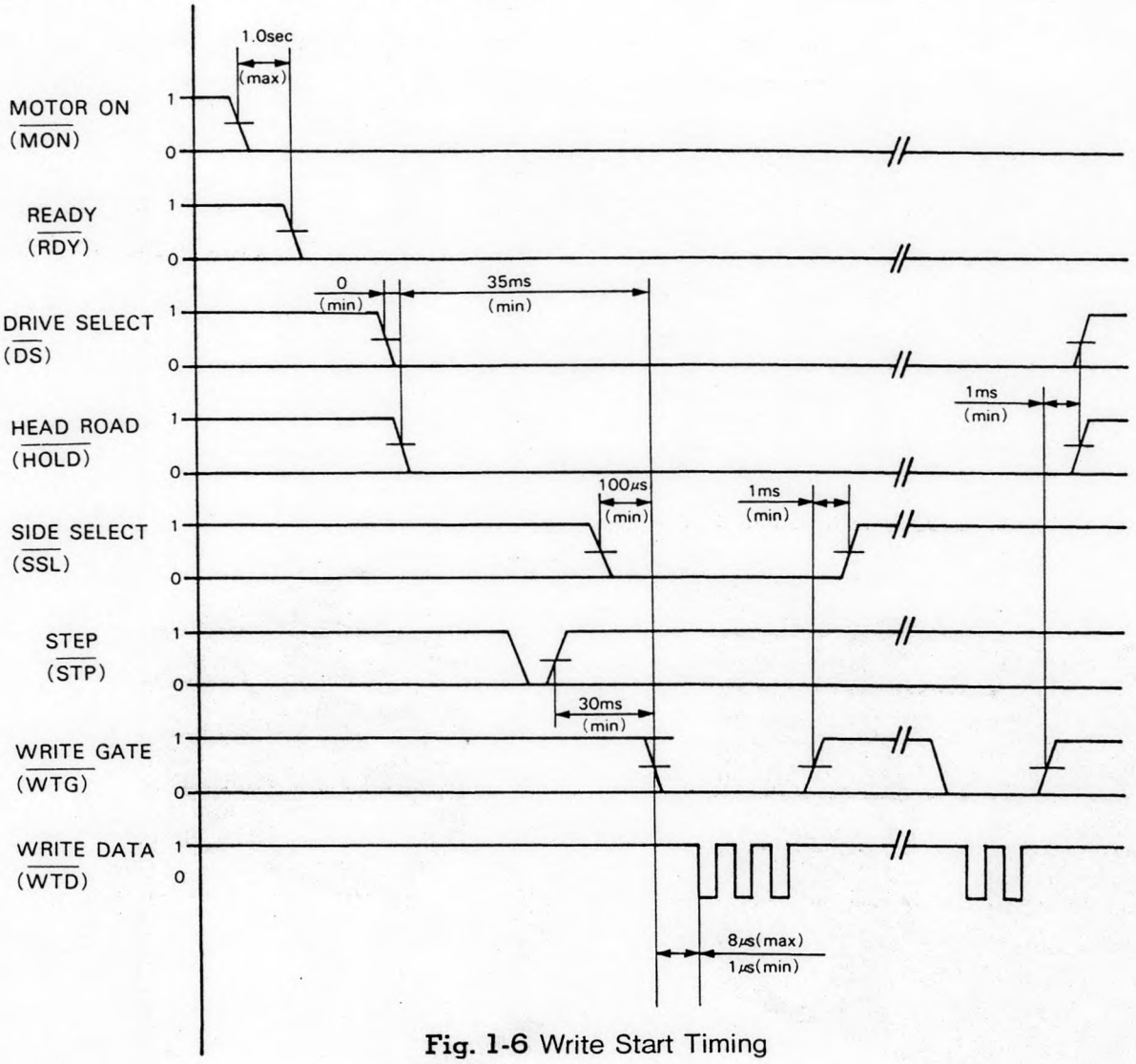


Fig. 1-6 Write Start Timing

The WRITE DATA timing in which data is written into the disk is as follows.

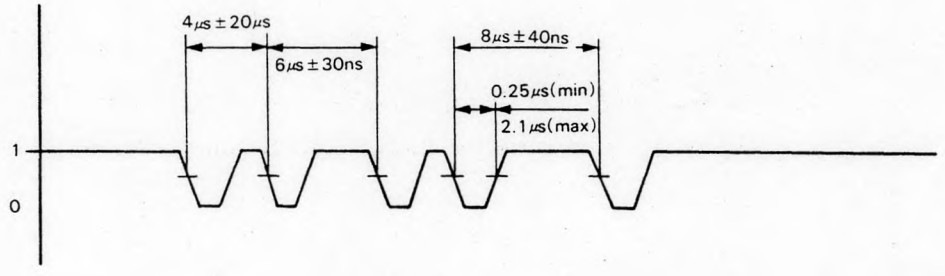


Fig. 1-7 Write Data Timing MFM System

1.7 Main Components

The TF-20 consists mainly of the following four units:

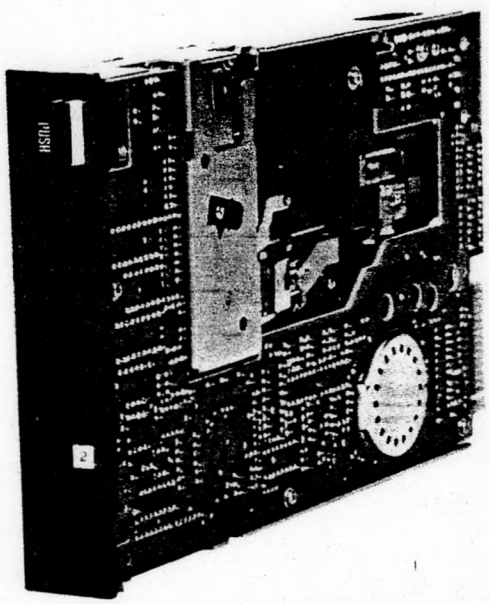
(1) SD-320 mini-floppy disk drive unit

This floppy disk drive unit of the TF-20 comprises the read/write head section, the head access mechanism, the head load mechanism, the disk drive mechanism, the disk protection mechanism, the disk eject mechanism, the index sensor section, the write protect sensor section and the control circuit section with the main and other PC boards.

The R/W head positioning system employs a VCM (voice coil motor) type linear actuator. And most of the control circuits are on the two chips of LSI developed by EPSON. As a result, the disk drive unit features high reliability and an ultra-thin size of 28 mm.

Furthermore, the maintenance is quite easy as is instructed in the Technical Manual of the 5.25 -Inch Floppy Drive Unit SD-320. The TF-20 has two of this drive unit on it.

Fig. 1-8 SD-320 Mini-Floppy Disk Drive Unit



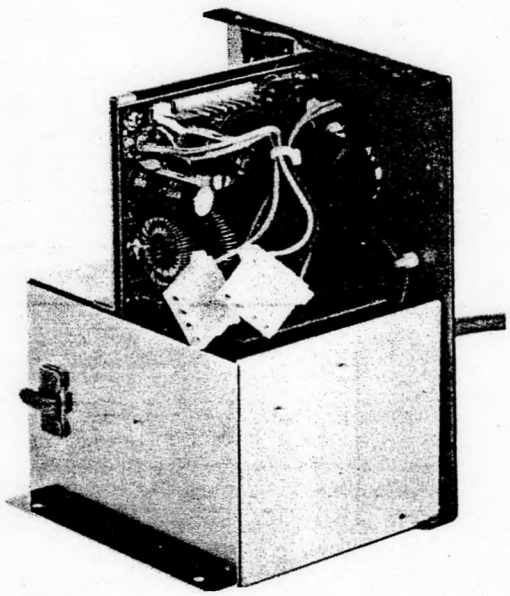


Fig. 1-9 Power Supply Unit

(2) Power supply unit

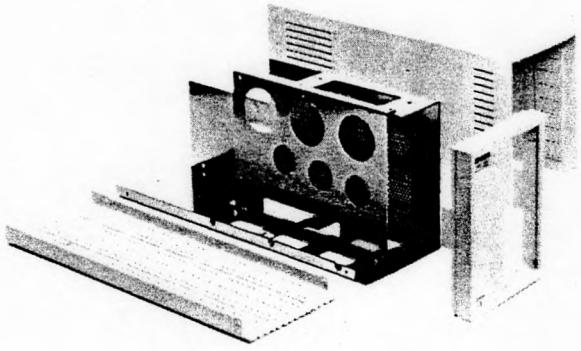
The power supply unit has the switching regulator circuit board mounted on the heat radiation plate. And the power transformer is mounted within the heat radiation plate and the line filter circuit board on it.

This power supply unit supplies all the voltages required for the TF-20. The line filter, consisting of a capacitor, suppresses noise to and from outside.

(3) Frame and case unit

The bottom panel and the floppy mounting plate permit easy installation of the mini-floppy drive unit. The disk drive unit, the power supply unit and the frame components are housed in the cover, bottom plate, front panel and rear panel.

Fig. 1-10 Frame and Case Unit



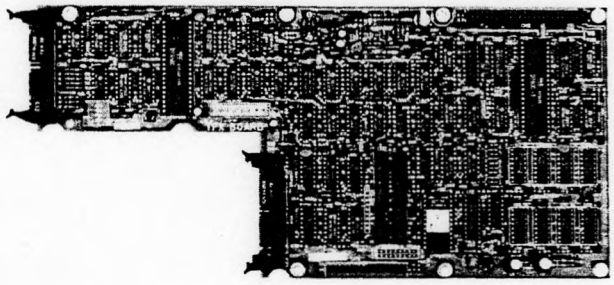


Fig. 1-11 Factory Option Unit

(4) Factory option unit

As a factory option, the following unit can be incorporated at the request of the user. The factory option unit, however, can not be added or remodeled once the TF-20 is shipped from the factory.

Factory Option: FDHC circuit board + TFX circuit board exclusive use with the EPSON HX-20

CHAPTER 2 PRINCIPLES OF OPERATION

2.1 General (Standard Model)

This chapter provides descriptions of the signals at the various connectors of the terminal floppy TF-20 and of the principles of operation of the floppys electric circuits and mechanisms.

2.2 Block Diagram

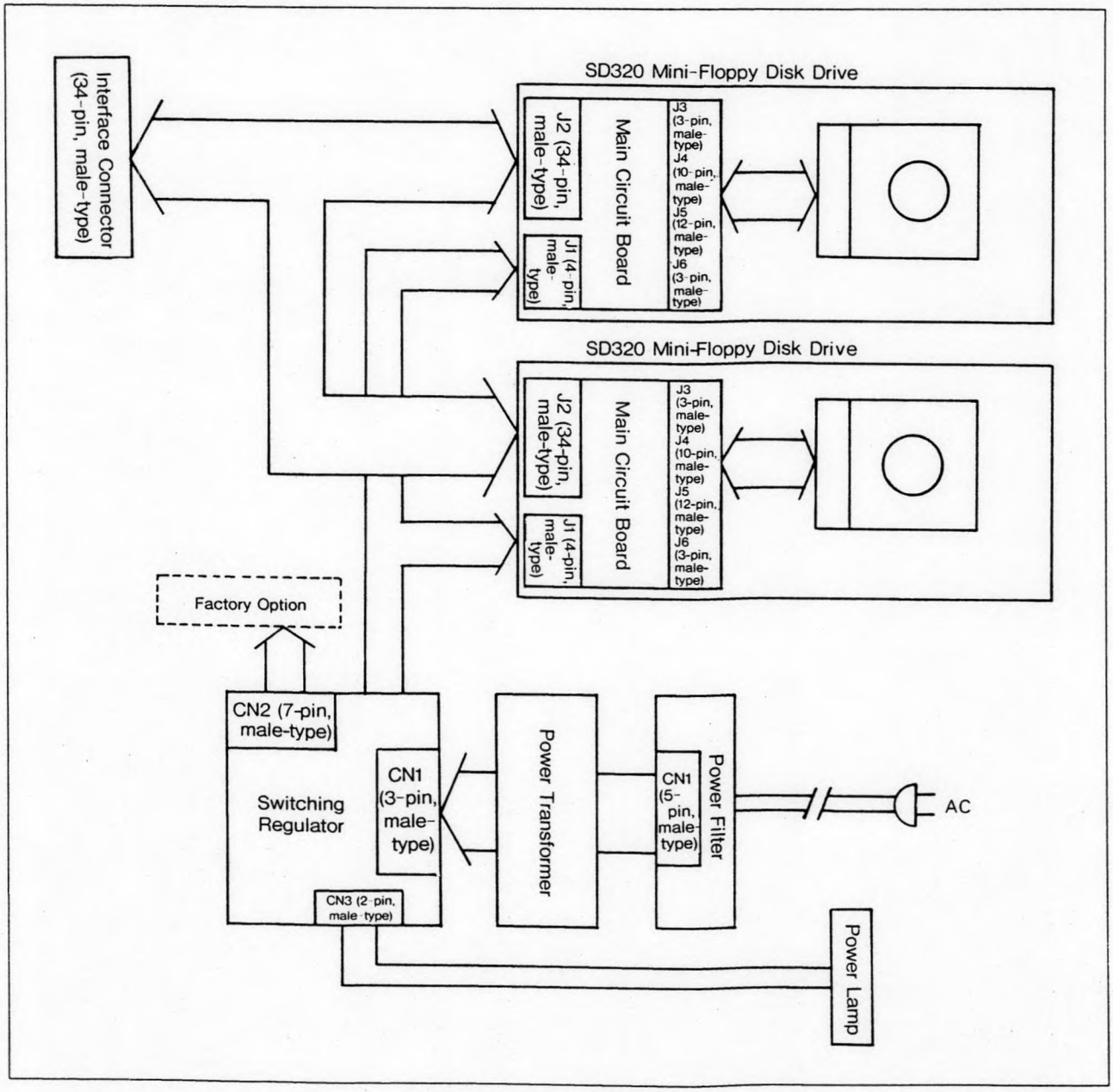


Fig. 2-1 Block Diagram

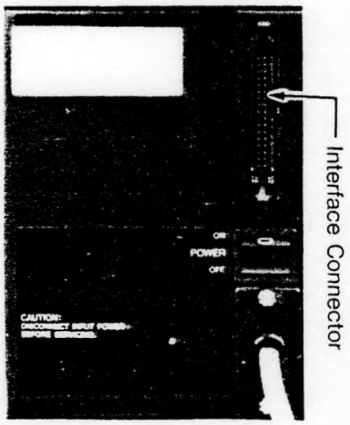
(1) Interface Connector

(a)Use: This connector is used for data exchange between the TF-20 and an external computer.

(b)Number of pins: 34 pins

(c)Part number: DDK FRC2-PA34-30LN

(d)Pin assignment: Refer to Table 2-1 below.



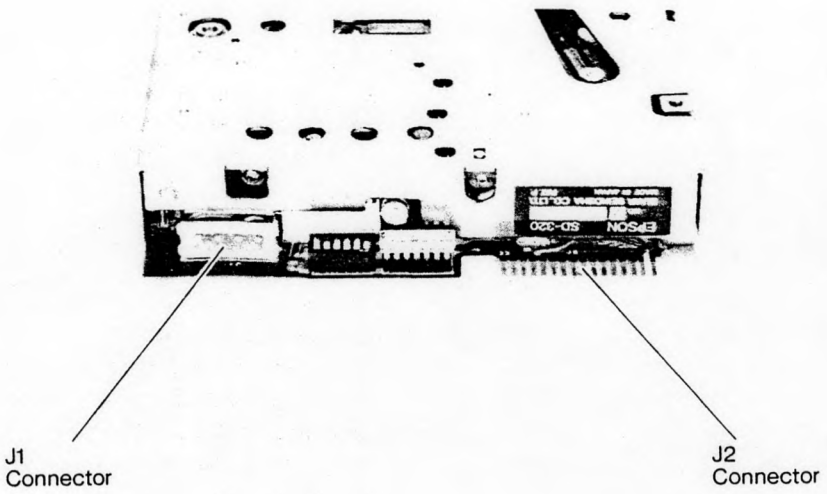
Interface Connector

Table 2-1 Pin Assignment of Interface Connector

Interface Connector Signal Pin No.	Drive SD-320 J2Connector Signal Pin No.	Signal	Direc-tion	Description
2		NC		
4	4	$\overline{\text{HOLD}}$	In	The HEAD LOAD signal at Logic "0" causes the read/write head to be loaded on the disk. (Pin 5 and Pin 6 of the DIP switch SS1 in the SD 320 mini disk drive can make head loading possible at a DRIVE SELECT signal.)
6	6	$\overline{\text{DS3}}$	In	This is the DRIVE SELECT 3 signal. Up to 4 mini disk drives can be connected in a daisy chain by the switching of the DRIVE SELECT signals. (The drive selection is made by pin 4 of the DIP switch SS1 on the SD-320 mini disk drive.)
8	8	$\overline{\text{IDX}}$	Out	The INDEX signal causes a Logic "0" pulse to be generated at each complete revolution of the floppy disk. The trailing edge of Logic "1" to Logic "0" indicates the beginning of data on the specified track.
10	10	$\overline{\text{DS0}}$	In	This is the DRIVE SELECT 0 siganl. (The drive selection is made by pin 1 of the DIP switch SS1 on the SD-320 mini disk drive.)
12	12	$\overline{\text{DS1}}$	In	This is the DRIVE SELECT 1 signal. (The drive selection is made by pin 2 of the DIP switch SS1 on the SD-320 mini disk drive.)
14	14	$\overline{\text{DS2}}$	In	This is the DRIVE SELECT 2 signal. Up to 4 mini disk drives can be connected in a daisy chain. (The drive selection is made by pin 3 of the DIP switch SS1 on the SD-320 mini disk drive.)
16	16	$\overline{\text{MON}}$	In	The MOTOR ON signal at Logic "0" causes the disk drive motor to start.
18	18	$\overline{\text{DRTN}}$	In	The DIRECTION signal determines the moving direction of the voice coil motor. The motor moves from track 00 to track 39 at Logic "0" or from track 39 to track 00 at Logic "1".

Interface Connector Signal Pin No.	Drive SD-320 J_2 Connector Signal Pin No.	Signal	Direc-tion	Description
20	20	$\overline{STP}$	In	When a pulse is input to the STEP signal line, the voice coil motor, which controls the position of the read/write head, moves in the direction specified by the DRTN signal. When the WRITE GATE signal is at Logic "0", the STEP signal is inhibited.
22	22	$\overline{WTD}$	In	The WRITE DATA signal line transfers data to be written into the disk. When the input pulse falls from Logic "1" to Logic "0", the write current flows in the opposite direction and enters the read/write head, causing a change in the magnetic flux. This signal is valid only when the WRITE GATE signal is at Logic "0".
24	24	$\overline{WTG}$	In	The WRITE GATE signal controls both Read Data and Write Data signals. When this signal is at Logic "0", the Write Data is valid, whereas when it is at Logic "1", the Read Data is valid.
26	26	$\overline{TKOO}$	Out	The TRACK 00 signal becomes Logic "0" when the read/write head is at the track 00 position.
28	28	$\overline{WPT}$	Out	The WRITE PROTECT signal notifies the host of the disk attached with a write protect label. It becomes Logic "0" when the disk has a write protect label attached.
30	30	$\overline{RDD}$	Out	The READ DATA signal causes a pulse string of raw data to be output from the read circuit. Normally, this signal becomes Logic "0" when the inversion of magnetization exists on the disk at logic level "1".
32	32	$\overline{SSL}$	In	The SIDE SELECT signal is used to select the upper or the lower read/write head. Side 1 (upper head) is selected at Logic "0", and Side 0 (lower head) at Logic "1".
34	34	$\overline{RDY}$	Out	The READY signal becomes Logic "0" when the power is turned on and a disk loaded rotates normally (INDEX pulse : 4 pulses).
1 \ add pin 33	1 \ add pin 33	$\overline{GND}$		Twisted Pair Return signal GND Level.

(2) SD-320 Mini-Floppy Disk Drive Connectors



1) J1 Connector

(a)Use: This connector is used to supply + 5V and + 12V from constant-voltage power supply to the mini-floppy disk drive.

(b)Number of pins: 4 pins

(c)Part number: Japan AMP C-172349

(d)Pin assignment: Refer to Table 2-2 below.

Table. 2-2 Pin Assignment of J1 Connector

Pin No.	Signal	Lead Wire Color	Use
1	+12V	Orange	+12V
2	GND	Black	Signal GND level
3	GND	Black	Signal GND level
4	+5V	Red	+5V DC

2) J2 connector

(a)Use: This connector is used for data exchange between the interface connector and the SD320 mini-floppy disk drive.

(b)Number of pins: 34 pins

(c)Part number: DDK 225F-A34-3

(d)Pin assignment: Refer to Table 2-1.

3) J3 connector

(a)Use: This connector is used to send the drive motor control signal from the main circuit board to the DM control circuit board.

(b)Number of pins: 3 pins

(c)Part number: Japan MOLEX 3022-3A

(d)Pin assignment: Refer to Table 2-3 below.

Table. 2-3 Pin Assignment of J3 Connector

Pin No.	Signal	Mating Connector	Use
1	CONT	P3 connector pin 1	Drive motor control signal
2	+12V	P3 connector pin 2	+12V DC
3	GND	P3 connector pin 3	Signal GND level

4) J4 connector

(a)Use: This connector is used to transfer the control signals of the main circuit board and the VCM adjustment circuit board.

(b)Number of pins: 10 pins

(c)Part number: Japan MOLEX 3022-10A

(d)Pin assignment: Refer to Table 2-4 below.

Table. 2-4 Pin Assignment of J4 Connector

Pin No.	Signal	Mating Connector	Use
1	HEAD LOAD SOL	P4 connector pin 1	The HEAD LOAD SOL signal at Logic "O" causes the read/write head to be loaded on the disk
2	+12V	P4 connector pin 2	+12V DC
3	VELOCITY DET	P4 connector pin 3	The speed detection voltage of the VCM adjustment circuit boad is input.
4	NEUTRAL	P4 connector pin 4	The reference voltage of the speed detection coil of the VCM adjustment circuit board is output.
5	VCM FWD	P4 connector pin 5	When the VCM FWD signal is more than +6V the read/write head moves in the direction of track 00 to track 39.
6	VCM BWD	P4 connector pin 6	When the VCM BWD signal is less than +6V, the read/write head moves in the direction of track 39 to track 00 .
7	GND	P4 connector pin 7	Signal GND level
8	TRACK 00 IN	P4 connector pin 8	When the read/write head is on track00, the TRACK 00 IN signal is at Logic "0".

Pin No.	Signal	Mating Connector	Use
9	POSITION 1	P4 connector pin 9	Step Timing signal from the position sensor of the VCM adjustment circuit.
10	POSITION 2	P4 connector pin 10	Step Timing signal from the position sensor of the position sensor of the VCM adjustment circuit.

5) J5 connector

(a)Use:This connector is used to transfer the signals of the main circuit board and the read/write head.

(b)Number of pins: 12 pins

(c)Part number: Honda HKP-12ML2L-4B

(d)Pin assignment: Refer to Table 2-5 below.

Table. 2-5 Pin Assignment of J5 Connector

Pin No.	Signal	Use
1	ERASE	The signal is transferred to the erase coil of the read/write head of Side 1.
2	ERASE	The signal is transferred to the erase coil of the read/write head of Side 0.
3	R/W COIL	The signal is transferred at the read/write head of Side 1.
4	R/W COIL	The signal is transferred at the read/write head of Side 0.
5	CENTER	+5V is supplied to the read/write coil of Side 1.
6	CENTER	+5V is supplied to the read/write coil of Side 0.
7	NC	
8		
9	R/W COIL	The signal is transferred at the read/write head of Side 1.
10	R/W COIL	The signal is transferred at the read/write head of Side 0.
11	GND	Signal GND of Side 1.
12	GND	Signal GND of Side 0.

6) J6 conector

(a)Use: This connector is used to transfer the signals of the main circuit board and the index sensor.

(b)Number of pins: 3 pins

(c)Part number: Honda FFC-(3) TAMEP-1

(d)Pin assignment: Refer to Table 2-6 below.

Table 2-6 Pin Assignment of J6 Connector

Pin No.	Sigal	Mating Connector	Use
1	+5V	P6 connector pin 1	+5V DC is supplied to the index sensor.
2	GND	P6 connector pin 2	Signal GND level
3	INDEX IN	P6 connector pin 3	The signal is transferred from the index sensor.

7) Functions of DIP and DIC switches

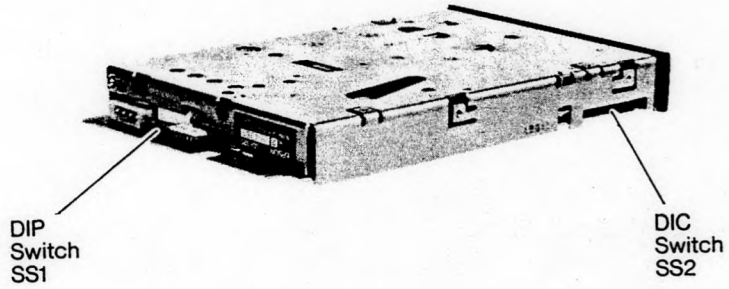


Table 2-7 Functions of DIP switches SS1

Switch No.	Function
SS-1	Drive 1 is set at ON.
2	Drive 2 is set at ON.
3	Drive 3 is set at ON.
4	Drive 4 is set at ON.
5	Head loading is made at HDLD signal by ON
6	Head loading is made at DS signal by ON

Table 2-8 Functions of DIC switches SS2 and SS3

Switch No.		Function
SS2	COM-MS	Head loading is made at MON signal.
	COM-HS	Head loading is made at the signal selected by switch SS1-5 or 6.
SS3	COM-DS	LED comes on at DS signal
	COM-HL	LED comes on at HDLD signal.

(3) Switching Regulator Connectors

1) CN1 connector

(a)Use: This connector is used to supply voltage from the power transformer to the switching regulator board.

(b)Number of pins: 3 pins

(c)Part number: MOLEX 5239-3

(d)Pin assignment: Refer to Table 2-9 below.

Table 2-9 Pin Assignment of CN1 Connector

Pin No.	Signal	Leab Wire Color	Use
1	AC 20V	Purple	AC voltage is supplied from the power transformer
2	NC		
3	AC 20V	Purple	AC voltage is supplied from the power transformer.

2) CN2 connector

(a)Use: This connector is used to supply + 5V and + 12V from the switching regulator board to the factory option board.

(b)Number of pins: 7 pins

(c)Part number: MOLEX 5265-7

(d)Pin assignment: Refer to Table 2-10 below.

Table 2-10 Pin Assignment of CN2 Connector

	Signal	Lead Wire Color	Use
1	GND	Black	Signal GND level
2	GND	Black	Signal GND level
3	GND	Black	Signal GND level
4	+5V	Red	+5V DC
5	+5V	Red	+5V DC
6	+12V	Orange	+12V DC
7	+12V	Orange	+12V DC

3) CN3 connector

(a)Use:This connector is used to supply voltage from the switching regulator board to the power lamp.

(b)Number of pins: 2 pins

(c)Part number: MOLEX 5051-02

(d)Pin assignment: Refer to Table 2-11 below.

Table 2-11 Pin Assignment of CN3 Connector

Pin No.	Signal	Lead Wire Color	Use
1	GND	Black	Cathode of the power lamp
2	LED	Red	Anode of the power lamp

(4) Power Filter Connector

1) CN1 connector

(a)Use: This connector is used to supply AC voltage from the power filter to the power transformer.

(b)Number of pins:5 pins

(c)Part number: MOLEX 5239-5

(d)Pin assignment: Refer to Table 2-12 below.

Table 2-12 Pin Assignment of CN1 Connector

Pin No.	Signal	Lead Wire Color	Use
2	AC voltage	White	AC voltage is supplied to the transformer.
5	AC voltage	Blue	AC voltage is supplied to the transformer.

2.3 Principles of Operation (TF-20 Standard Model)

The SD-320 mini-floppy disk drive outputs the IDX signal to determine the beginning of track, the TK00 signal to show the read/write head in the track 00 position, and the RDY signal to identify the normal rotation of the disk. Also, the WPT signal is output to identify the presence or absence of writing into the disk.

These four signals determine the operation of the floppy disk. The signals sent to the disk drive are the drive signal for the drive head solenoid, the drive signal for the disk drive motor and the control signal for the head positioning VCM mechanism.

All these signals are converted to match the operation timings of the various mechanisms by the custom LSI SDF 9401F on the control circuit board within the disk drive. And the mechanisms of the disk drive performs operations according to these signals.

Refer to 2.4 and the separate SD-320 Technical Manual for detailed description of the electric circuits and mechanical operations.

Also, refer to chapter 4 for the operation principles of the control circuit of the factory option unit.

2.4 Electrical Circuit

2.4.1 Fuse and filter circuit

The fuse and filter circuit is located on a Bakelite circuit board, together with the power switch which turns on and off the primary AC input voltage. Fig.2-2 shows the layout of the respective components on the fuse and filter circuit, and Fig.2-3 shows the connection diagram of this circuit.

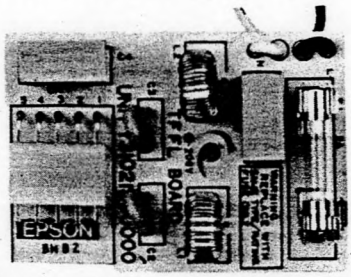


Fig. 2-2 Component Layout of Fuse & Filter Circuit

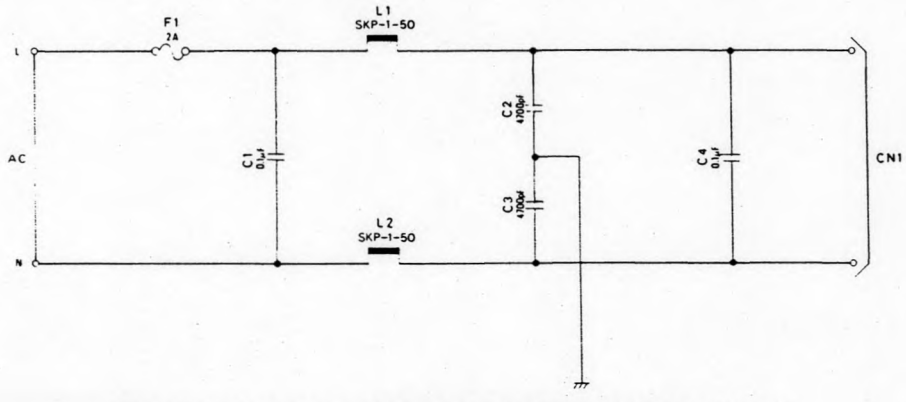


Fig. 2-3 Conection Diagram of Fuse & Filter Circuit

The AC Voltage from the power line first flows through the double-throw power switch and enters fuse F1.

Noise suppressing choke coils L1 and L2 are connected to this line. And between this line and ground, four noise suppressing capacitors C1 to C5 are connected. They function to filter the line noise from the power source as well as the noise from the disk drive unit to the power line, so that the digital circuits within the disk are not affected by external noise and any noise from the disk does not leak out to external lines.

2.4.2 Power transformer

The power transformer of the TF-20 lowers the AC Voltage from the primary side and supplies the voltages required for the floppy disk drive circuit and the control circuit of the factory option unit. Fig. 2-4 shows the layout of the power transformer, and Fig. 2-5 shows the circuit diagram.

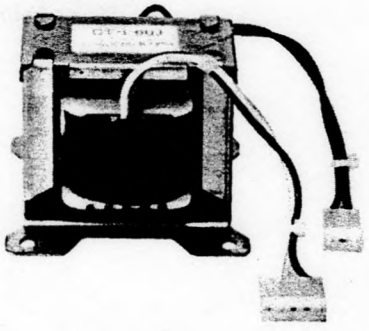


Fig. 2-4 Layout of Power Transformer

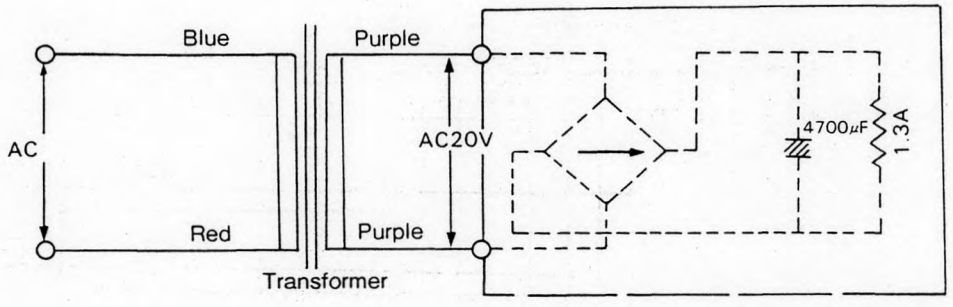
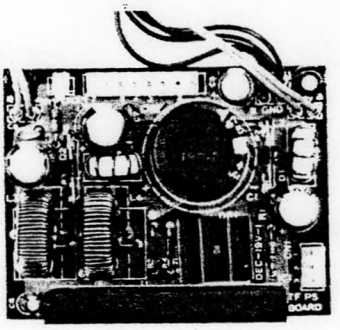


Fig. 2-5 Circuit Diagram of Power Transformer

2.4.3 Switching regulator circuit

The voltages lowered by the power transformer are converted into required voltages by the rectifier and switching regulator circuit. Fig. 2-6 shows the layout of the switching regulator circuit board, and Fig. 2-7 shows the circuit diagram.

Fig. 2-6 Layout of Switching Regulator



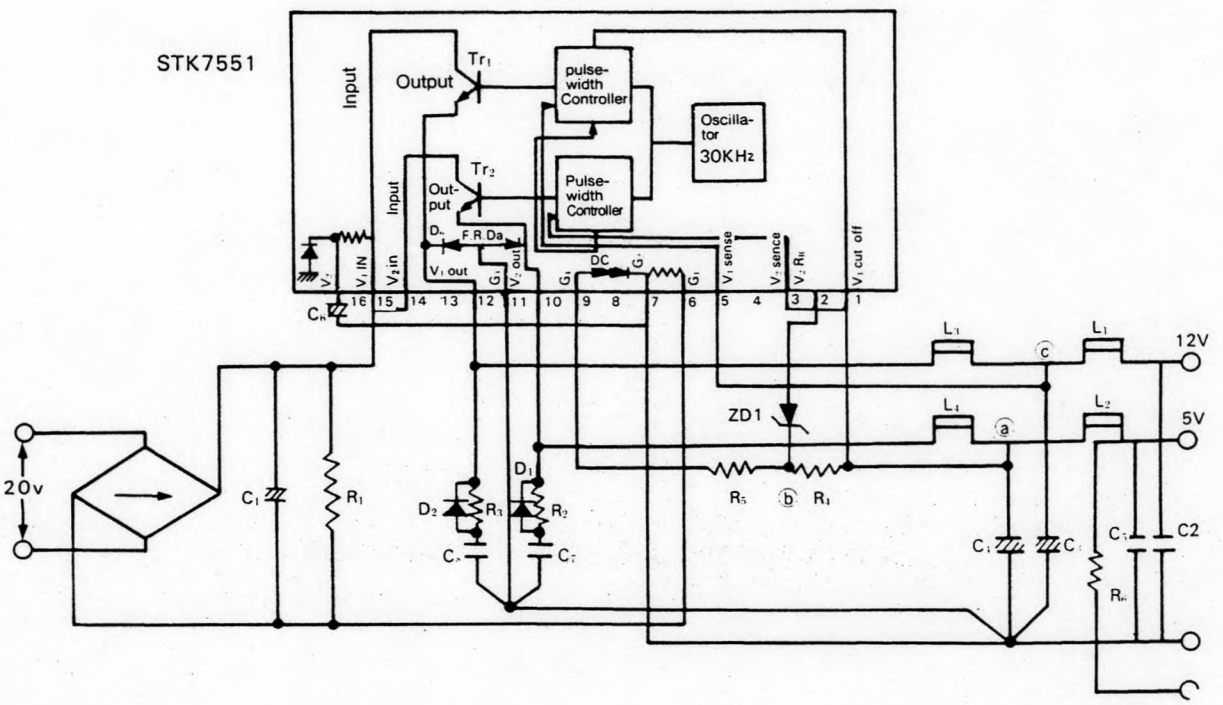


Fig. 2-7 Circuit Diagram of Switching Regulator

In the switching requlator circuit, the following voltages are produced:

+5V
+12V } Power supply for floppy disk drive and factory option.

K
A } Power supply for power lamp.

2.4.4.1 Read/write logic and amplifier circuit

Fig. 2-12 shows the structure and the block diagram of the magnetic head.

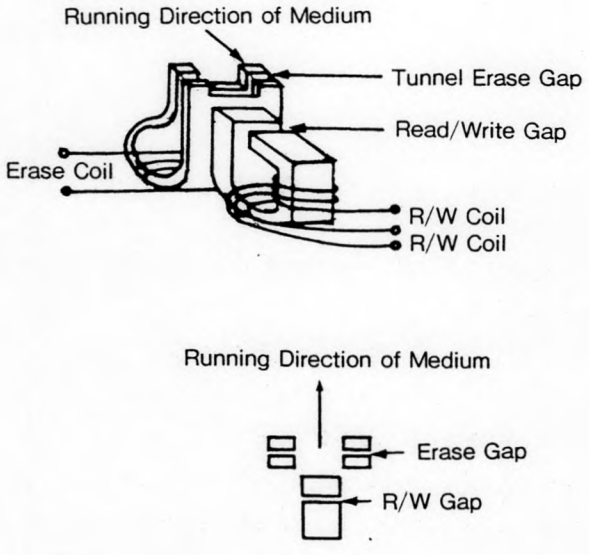


Fig. 2-11 Structure of Magnetic Head

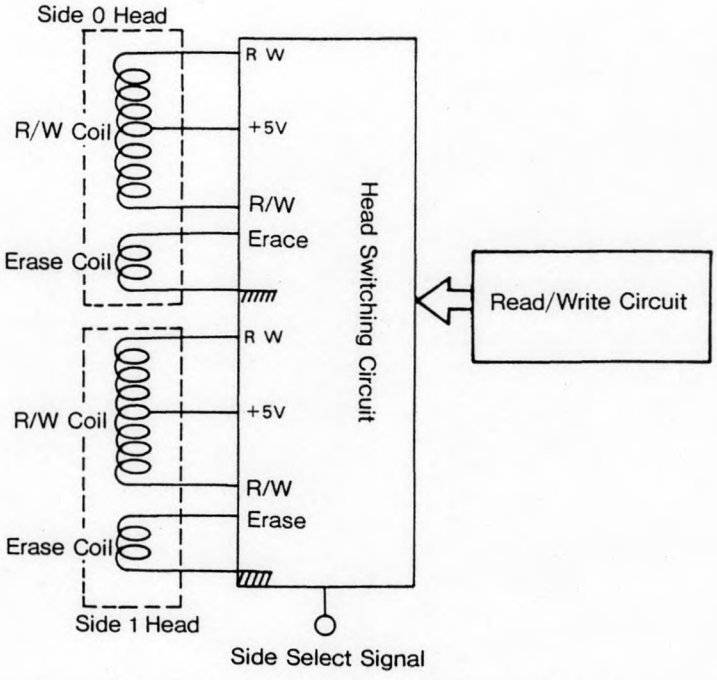


Fig. 2-12 Block Diagram of Magnetic Head

The magnetic head is of such a structure that it has an erase gap on both sides of the read/write gap. The erase gaps are located behind the read/write gap as viewed in the running direction of the medium. These erase gaps are designed to trim through data of one track and prevent interference by data of the adjacent tracks.

Fig.2-13 shows the read/write amp circuit diagram, and Fig.2-14 the block diagram of the read amp circuit. And Fig-15 shows the waveforms at various parts of write/read operations.

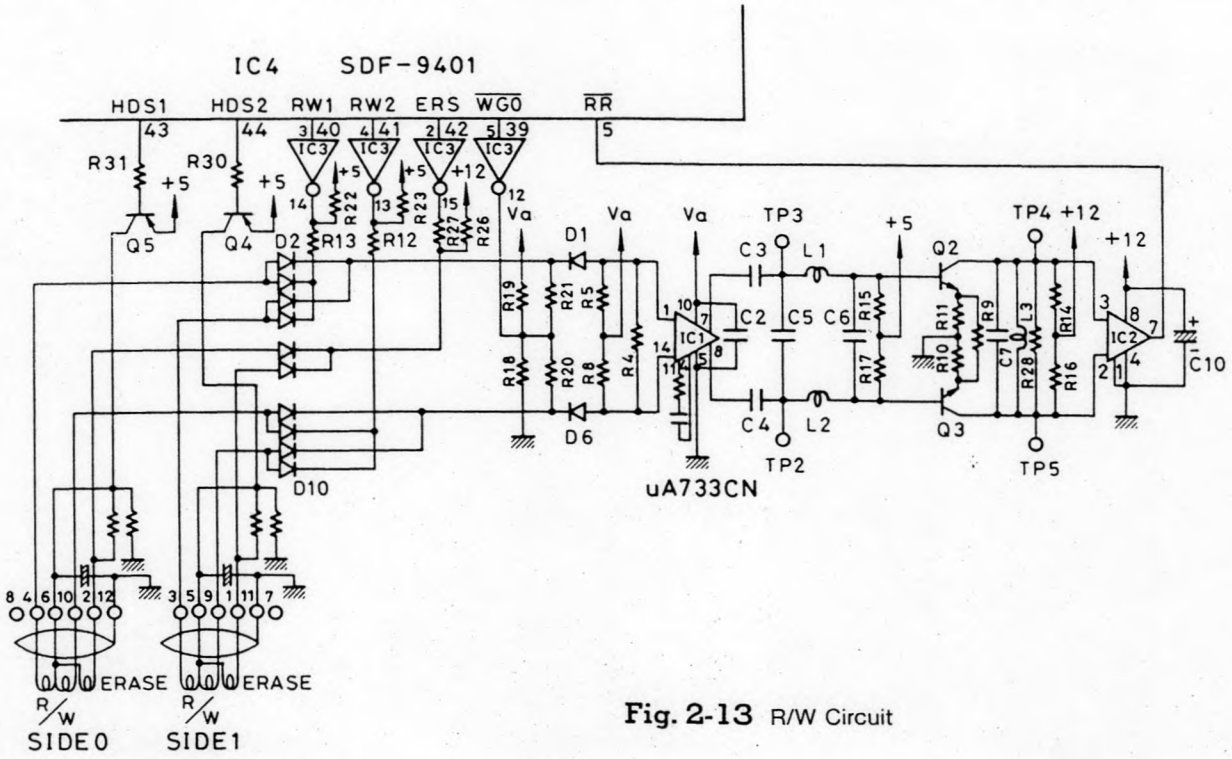


Fig. 2-13 R/W Circuit

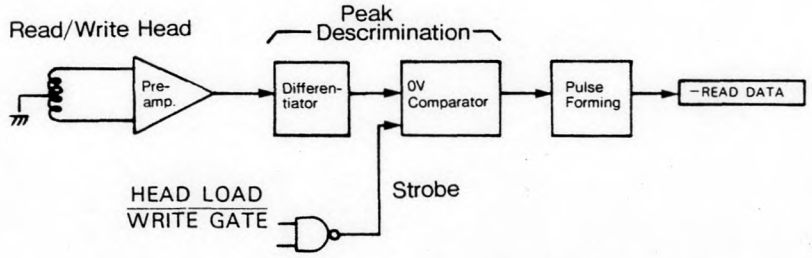


Fig. 2-14 Block Diagram of Read Amp Circuit

Write data sent to the drive from the controller has gone through FM modulation. It is frequency -divided by the flip-flop in IC4 to become a rectangular signal to be inverted at the Write Data pulse. This signal inverts the polarity of the head current, thus causing a flux inversion in synchronism with the Write Data pulse.

When pin 43 (HDSI) of IC4 becomes "LOW", a voltage of +5V is supplied to the R/W coil and erase coil of Side 0 from the current driver TrQ5. When pin 44 (HDS2) of IC4 becomes "LOW", a voltage of +5V is supplied to the R/W coil and erase coil of Side I from the current driver TrQ4. Selection of Side 0 or Side 1 is controlled by the Side Select signal sent to the drive from the controller.

At Read, the magnetic flux caused by the residual magnetism on the disk is detected by the head and is amplified by the preamplifier of IC1, Then it is passed through the low-pass filter circuit of differentiator C3, C4, C5, C6, L1 and L2 and the peak is detected by the 0V comparator at TrQ2 and Q3. And after going through the pulse forming by the comparator IC2, it is output at pin 5 (RR) of IC4.

Read data is not output when the Wait Gate (pin 39 of IC4) is at the "LOW"level.

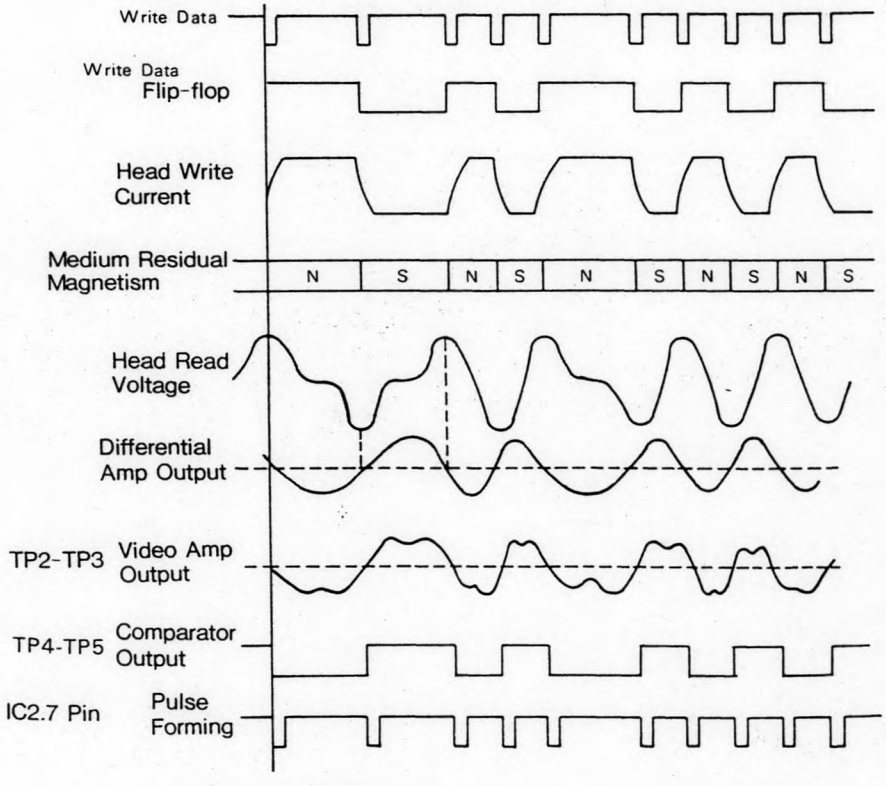
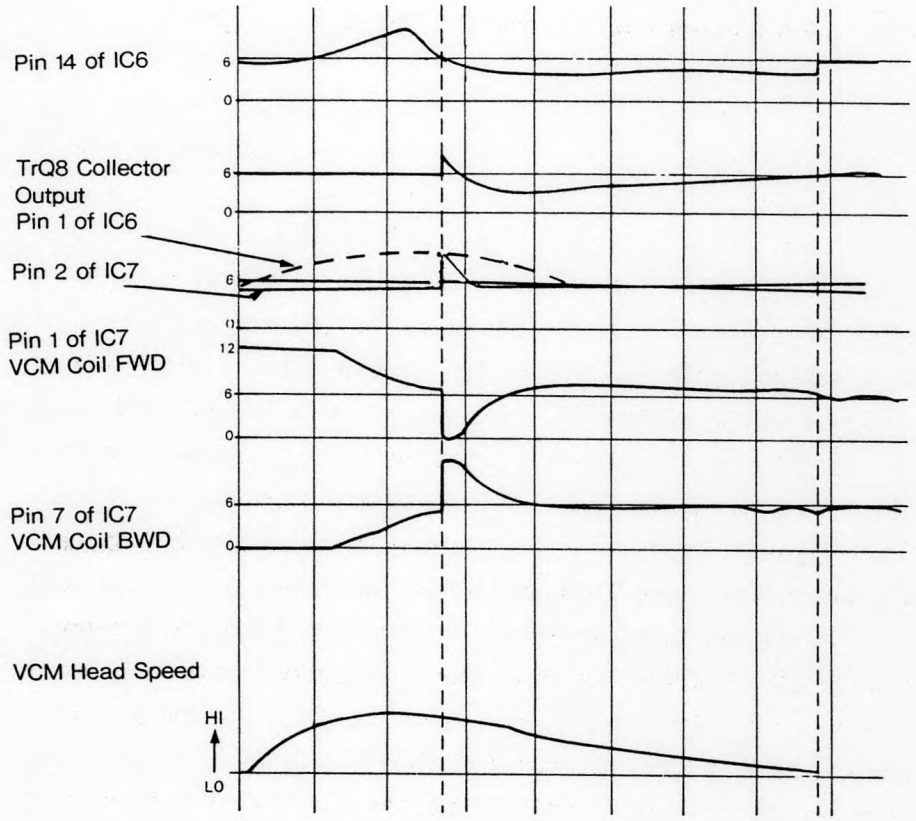
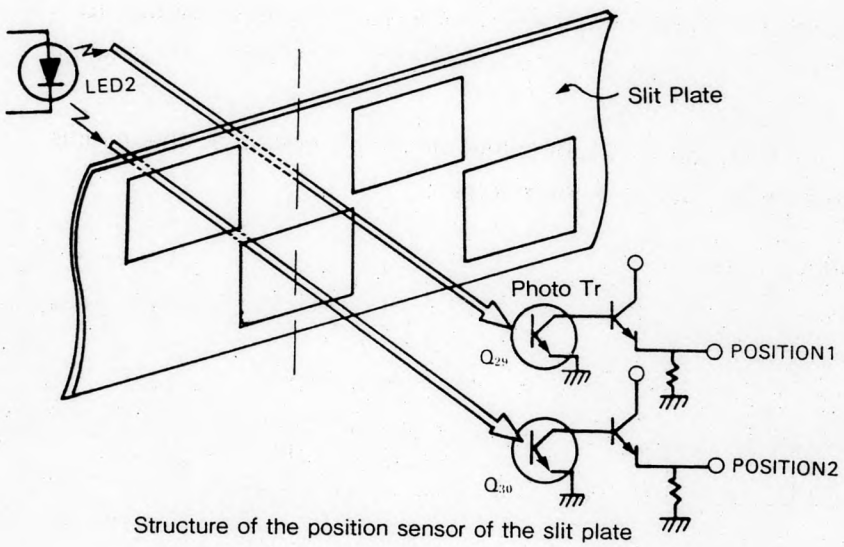


Fig. 2-15
Waveforms at Various Parts of Write/Read Operations



ig. 2-19

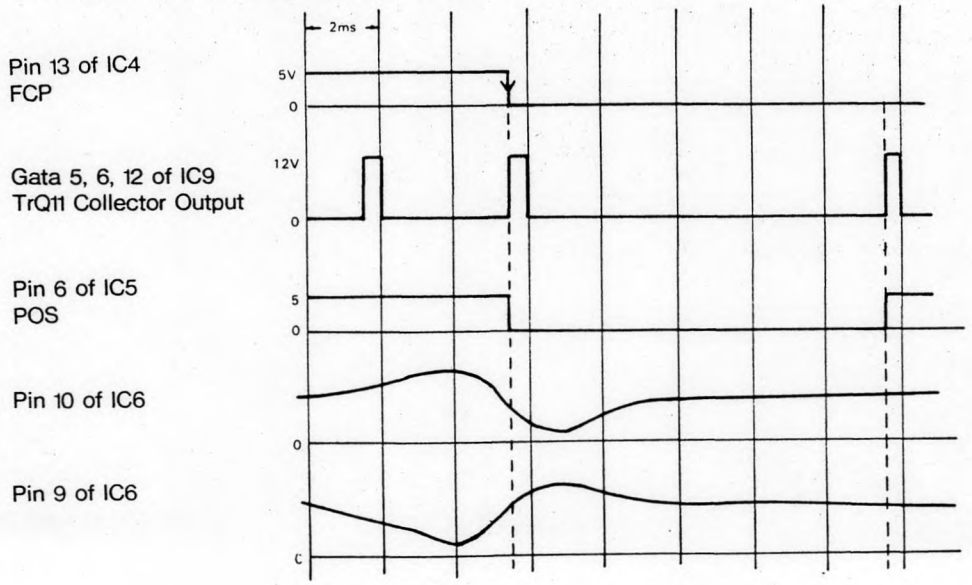


Structure of the position sensor of the slit plate

IC7 becomes a 2V level through inversion as shown in Fig. 2-18. Thus, a voltage is applied in the forward direction to the voice coil, which triggers the movement of the head from track 00 to track 39.

The voltage in proportion to the movement of the head is detected by the speed sensor coil and amplified by OP AMP, and it is subjected to a negative feedback in a voltage of +6V or above from pin 1 of IC6 to pin 2 of IC7. By this signal, the speed of the VCM head is kept constant. When it is 4.8 to 5.0 msec after the rising of pin 13 (FCP) signal of IC4 to +5V, the timing of the position sensor signals position 1 and 2 of the slit plate Where it is inputed to pin 9 and pin 10 of IC6 goes through an inversion. At the same time, pin 13 (FCP) signal of IC4 becomes 0V and TrQ8 is cut off. Since the voltage from the speed sensor coil at pin 1 of IC6 is +6V or above, the voltages at pin 1 and pin 7 of IC7 become 2V and +10V respectively as shown in Fig. 2-18. Thus the voice coil motor is braked once by the application of a voltage in the reverse direction. Then a voltage of +6V or below is supplied from pin 14 of IC6, and as a result a voltage in the forward direction works on the voice coil, thus decelerating the head gradually.
Now the timing of Positions 1 and 2 is inverted again, and out put at pin14 of IC6 become a low impedance, by the gate signal of pin 5, 6, 12 of IC9. which causes the voltage rise to +6V by charging the capacitor C20. The pulse at this time passes through the capacitor C21 and is input to pin 2 of IC7. This will brake the voice coil again and stops the head.
Fig. 2-19 shows the structure of the position sensor of the slit plate, the output voltage from the phototransistor of the position sensor of the slit plate and the start position. braking position and stop position of the position sensor of the slit plate. Then the movement of the VCM head from track 39 to track 00 is made on the same principle as that of the head from track 00 to track 39. In the operation, the pin 14 (BCP) signal of IC4 becomes 0V, and turns on TrQ7 to output + 12V. This will apply a voltage in the reverse direction to the voice coil and move the head from track 39 to track 00. Except for the gate pulse voltages at pin 5 of IC5 and pin 5, 6, 12 of IC9, the timing voltages at various parts are all opposite to those of the head movement from track 00 to track 39. Fig. 2-19 shows the start position, braking position and stop position of the position sensor of the slitplate.
As was mentioned already, the voice coil motor reaches the maximum speed at the middle position and after that is rapidly decelerated by the speed sensor.

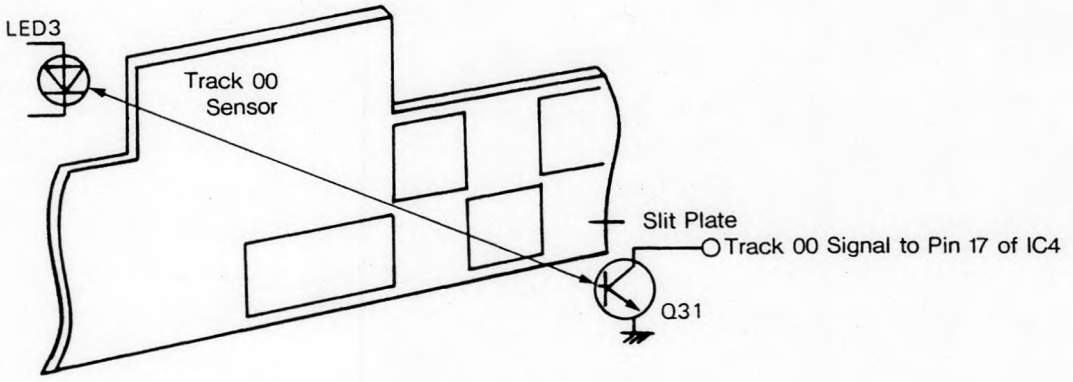
Fig. 2-18 Timing Waveforms at Various Parts



2.4.4.3 Track 00 sensor circuit

When the read/write head is at track 00, a Track 00 sensor signal is given. As shown in Fig. 2 -20. the light from LED3 passes through the track 00 sensor part of the slit plate, turns off the phototransistor Q31 and makes a "HIGH" evel at pin 17 of IC4, thus signaling the track 00 position of the R/W head.

Fig. 2-20 Structure of Track 00 Signal Sensor



2.4.4.4 Head load drive circuit

At a "HIGH" signal from pin 4 (HEAD) of IC5, the head load solenoid is energized, causing the pad lever to be pulled downward.

With the DIP and DIC switches set as in Table 2-13, the head load timing can be changed:

Tnble 2-13

DIP Switch SS1-5: ON Head loading at HOLD signal

6: ON Head loading at DS signal

DIC Switch SS2 = CM-MS: Head loading at MON signal

COM-HS: Head loading at signal selected by DIP switch SS1-5 and 6

2.4.4.5 Index sensor circuit

As shown in Fig. 2-21, the index sensor consists of a pair of light emitting diode LED and phototransistor Q32.

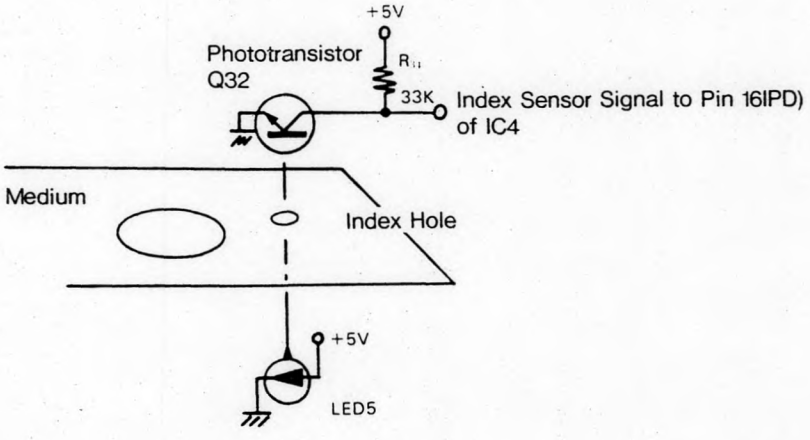
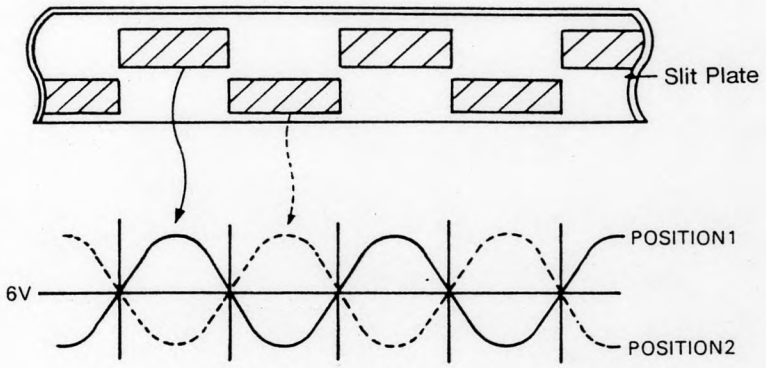
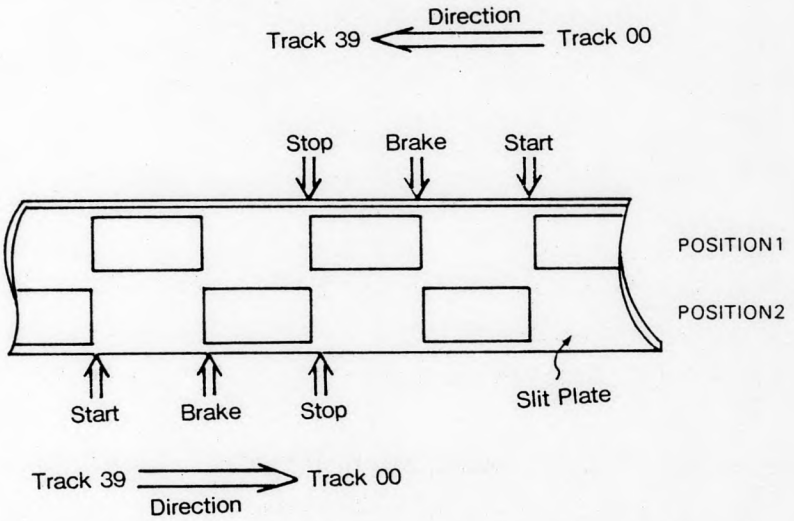


Fig. 2-21



POSITION1,2 のスリット板の位置とフォト Tr からの出力電圧



moving the head from track 00 to track 39 or from track 39 to track 00

2.4.4.6 Side select circuit

See the read/write circuit.

2.4.4.7 Write protect circuit

The write protect circuit, consisting of a pair of LED and phototransistor Q1, detects the presence or absence of a write protect lable attached to the notch in the jacket.

2.4.4.8 Drive select circuit

Drives 1 to 4 are respectively selected by the DIP switch SS1-1 to 3.

2.4.4.9 Drive motor control circuit

The disk drive motor is an outer-rotor-type DC motor featuring long service life.

As shown in Fig. 2-22, the motor mechanism consists of a frequency generator (FG) to generate the frequency proportional to the rotation of the rotor and a motor drive section.

When a current is fed to the drive coil in a stepping manner, the magnet rotor starts to run. With the magnet rotating, the frequency generator (FG) coil becomes a generator outputting the frequency proportional to the speed of rotation. The timing of the current sent to the drive coil is determined by the notch in the magnet passing the Hall element.

When the motor control output at pin 33 (MS) of IC4 becomes "HIGH", pin 10 of IC3 becomes "LOW", thus setting the emitters of TrQ33 and Tr Q20 for GND. At the same time, the base of TrQ33 becomes 0V and TrQ20 reseats switching by the pulse voltage from pin 5 of IC10.

When TrQ20 is on, the emitters of TrQ21, Q22, Q23 and Q24 are set at the 0V level. And the transistor selected by the Hall element of HD1 and HD2 turns on to supply current to the drive coil and causes the drive motor to run. The speed of the drive motor is determined by the pulse width from pin 5 of IC10, and the frequency at pin 5 of IC10 is determined by the frequency of the frequency generator (FG) coil and the variable resistance VR2.

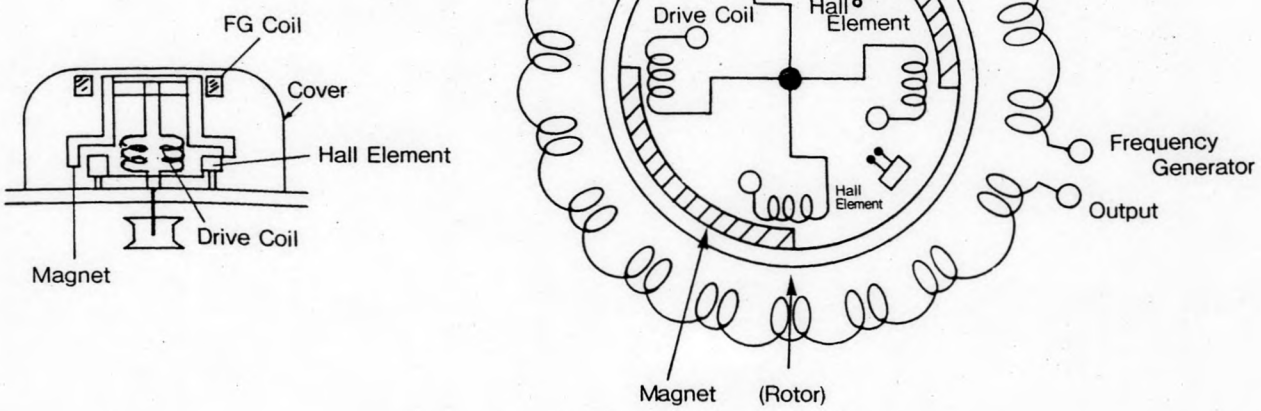
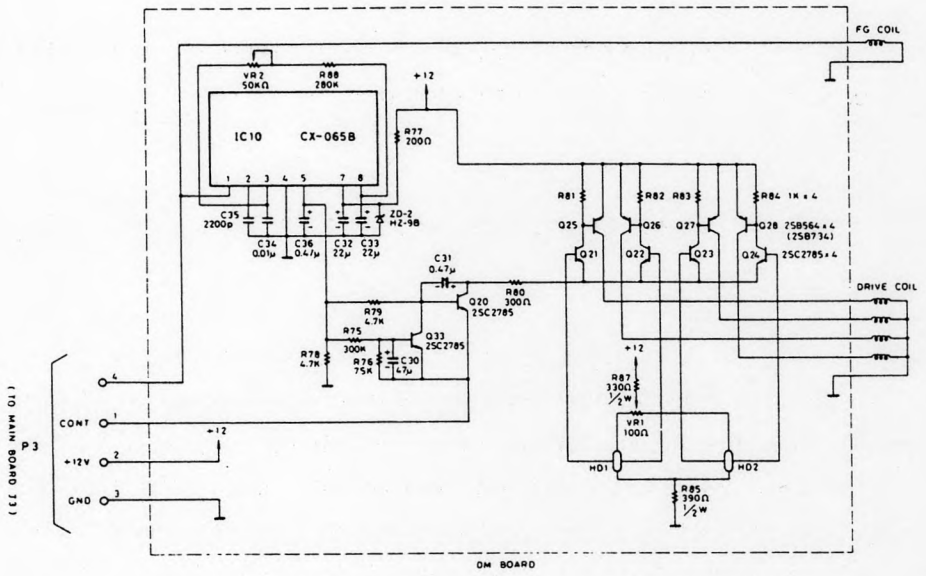


Fig. 2-22 Principle of Operation

Fig. 2-23 shows the drive motor control circuit
Fig. 2-23 DM Control Circuit



CHAPTER 3 DISASSEMBLY & ASSEMBLY

CHAPTER 4 HX-20 FACTORY OPTION

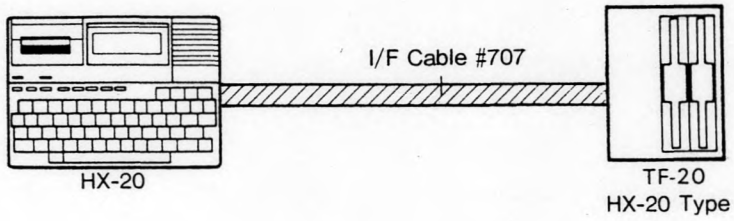
4.1 General

4.1.1 Features of TF-20 (HX-20 Type Model)

With the HX-20 factory option incorporated, the TF-20 becomes an intelligent type of exclusive -use terminal floppy for the HX-20, having the CPU, 64KB memory and high-speed serial interface within it. The TF-20 performs all the file manage-ment and exchanges necessary information with the HX-20. Accordingly, this TF-20 lightens the burden of file management on the HX-20 and reduces the OS of the HX-20's memory.

4.1.2 Connection

(1) Connection with the HX-20



(2) Connection with the HX-20 and Display-Controller

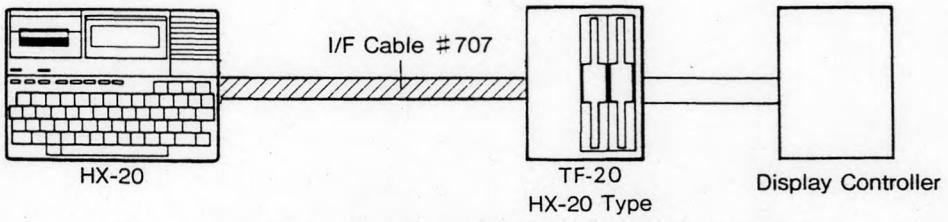


Fig. 1-1 Connection of HX-20 Factory Option TF-20

4.1.3 Specifications

(1) Memory capacity
Memory capacity per unit: 656 KB
Memory capacity per drive: 328 KB
No. of tracks per drive: 80 tracks (40x2)
No. of sectors per track: 16 sectors
Memory capacity per sector: 256 B

(2) Access time
Inter-track access time: 15 msec
Communication with HC-20: 38.4 KBps

(3) Power supply
Voltage: AC115/220/240 V
Frequency: 49.5 to 60.5 Hz
Power consumption: 40 VA max.

(4) Dimensions and weight

Width: 120mm

Depth: 350mm

Height: 165mm

Weight 6kg

(5) Ambient conditions

Temperature (operating): 5°C to 30°C

(non-operating): −30°C to 65°C

Relative humidity (operating): 20% to 80% (no condensation)

(non operating): 5% to 85% (no condensation)

(6) Insulation resistance/strength

Insulation resistance: 10 M min. between AC power supply and case (by DC500V megger)

Insulation strength: Can withstand 1KV (R.M.S.) 50/60Hz applied between AC power supply and case for 1 min or more.

Shock resistance (operating): 1G for 1ms maximum

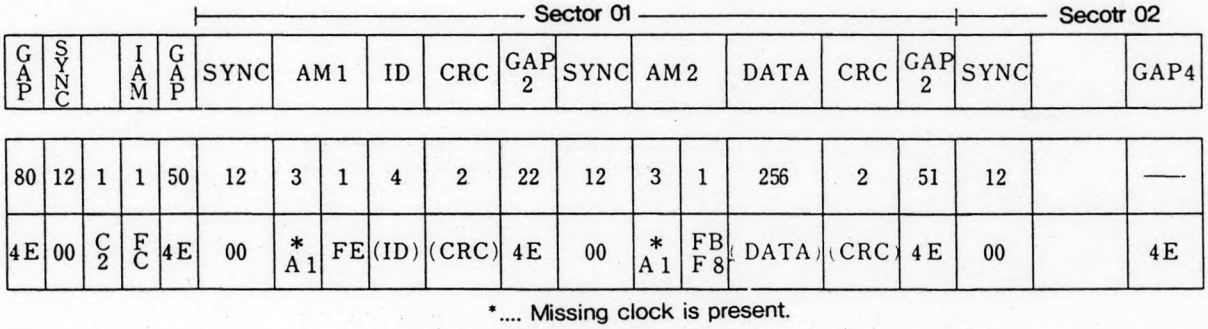
(non-operating): 2G for 1ms maximum

Vibration resistance

(operating):0.25G, 5-55Hz

(non-operating): 1G, 5-55Hz

4.1.4 Format specification



*.... Missing clock is present.

Fig. 1-2 Format

One floppy disk has a memory capacity of 278KB. It is divided into blocks of 2KB each. Accordingly, a floppy disk has 139 blocks.

The floppy disk is used block by block in filing. Disk BASIC assigns one block for each 16 records, namely, one block for records 1 to 16 and another for records 17 to 32.

(One record consists of 128B. 16 records are 16x128=2048B, or 2KB.)

When a file requires a newblock, Disk BASIC secures for the file a block which has not been used on the floppy disk. At an erasure of a file, all the block having been used by the file are vacated for use by other files.

With the blocks used in this manner, the memory area on the floppy disk is utilized effectively.

4.1.5 Interface connector

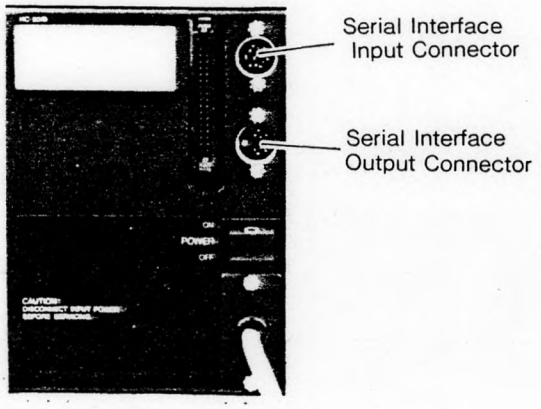


Fig. 2-3 Interface Connector

(1) Serial Interface Input Connector

(a) Use : This connector is used for data exchange between the TF-20 and the **HX**-20 computer.

(b) Number of pins : 6 pins

(c) Part number : TCS0260-01-1101 (Hoshi Denki)

(d) Pin assignment : Refer to Table 1-1 below.

Table 1-1 Pin Assigment of Serial Intertace Connector for HX-20.

Pin No.	Signal	Direction (as viewed from floppy)	Description
1	RXS	Out	This signal output from the terminal floppy is connected to another terminal or HX-20 serial input.
2	PINS	Out	This is the OR signal of PINC and DTRA of serial controller μPD7201 inside. This signal is not used usually.
3	TXS	In	This is a serial input signal to the terminal floppy from the HX-20.
4	POUTS	In	This input signal is connected to the CTSA terminal of serial controller μPD7201 inside via the line receiver. It means that a serial output at "HIGH" level is permitted.
5	GNDS	—	GND

(2) Serial Interface Output Connector

(a) Use : This connector is used for data exchange between the TF-20 and the HX-20 display controller or some other terminal.
It is an interface connector for the extension drive of theTF-20 (exclusive use with HX-20).

(b) Number of pins : 5 pins

(c) Part number : TCSO250-01-1301

(d) Pin assignment : Refer to Table 1-2 below.

Table 1-2 Pin Assignment of Serial Interface Connector for HX-20 Display Controller

Pin No.	Signal	Direction (as viewed from floppy)	Description
1	GNDC		GND
2	TXC	Out	This serial signal output from the terminal floppy is connected to another teminal (display controller) of the HX-20.
3	RXC	In	When this input signal is at "LOW" level, a signal from the terminal floppy is output from RXS.
4	POUTC	Out	This output signal functions the same way as the POUTS signal. (It is not use in this application.)
5	PINC	In	The OR signal of this signal and DTRA of the serial controller μPD7201 is output at PINS. (It is not used in this application.)

4.1.6 Constitution of TF-20 (HX-20 Type Model)

The TF-20 (exclusive use with HX-20) consists of the TF-20 standard model section and the HX-20 factory option section. The HX-20 factory option comprises the FDHC board and the TFX board as shown in Fig. 1-3.

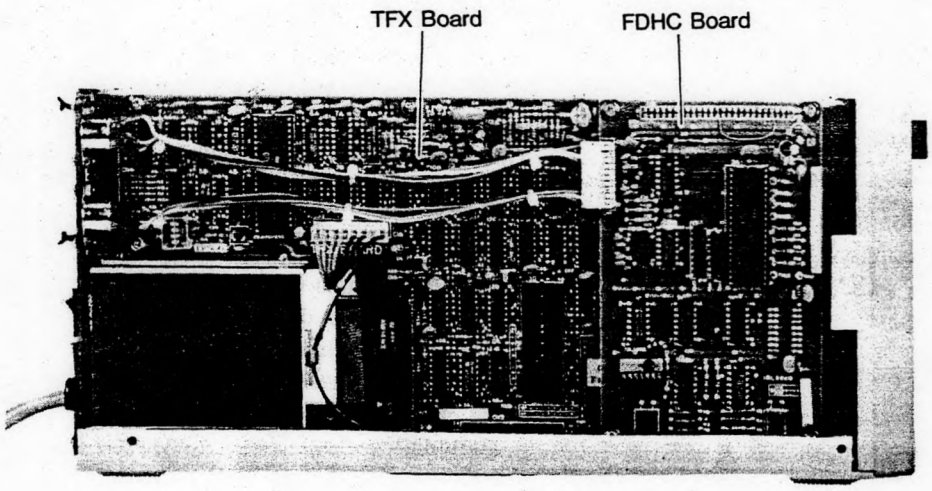


Fig. 1-3 Constitution of TF-20 (Exclusive Use with HX-20)

4.2 Principles of Operation

4.2.1 General

This chapter provides descriptions of the signals at the various connectors of the TF-20 for exclusive use with the HX-20 and of the principles of operation of the floppy's electric circulits. For detailed description of the operation of the drive SD-320 and the power supply unit,refer to the chapter on the TF-20 (Standard Model) and the separate SD-320 Technical Manual.

4.2.2 Block Diagram

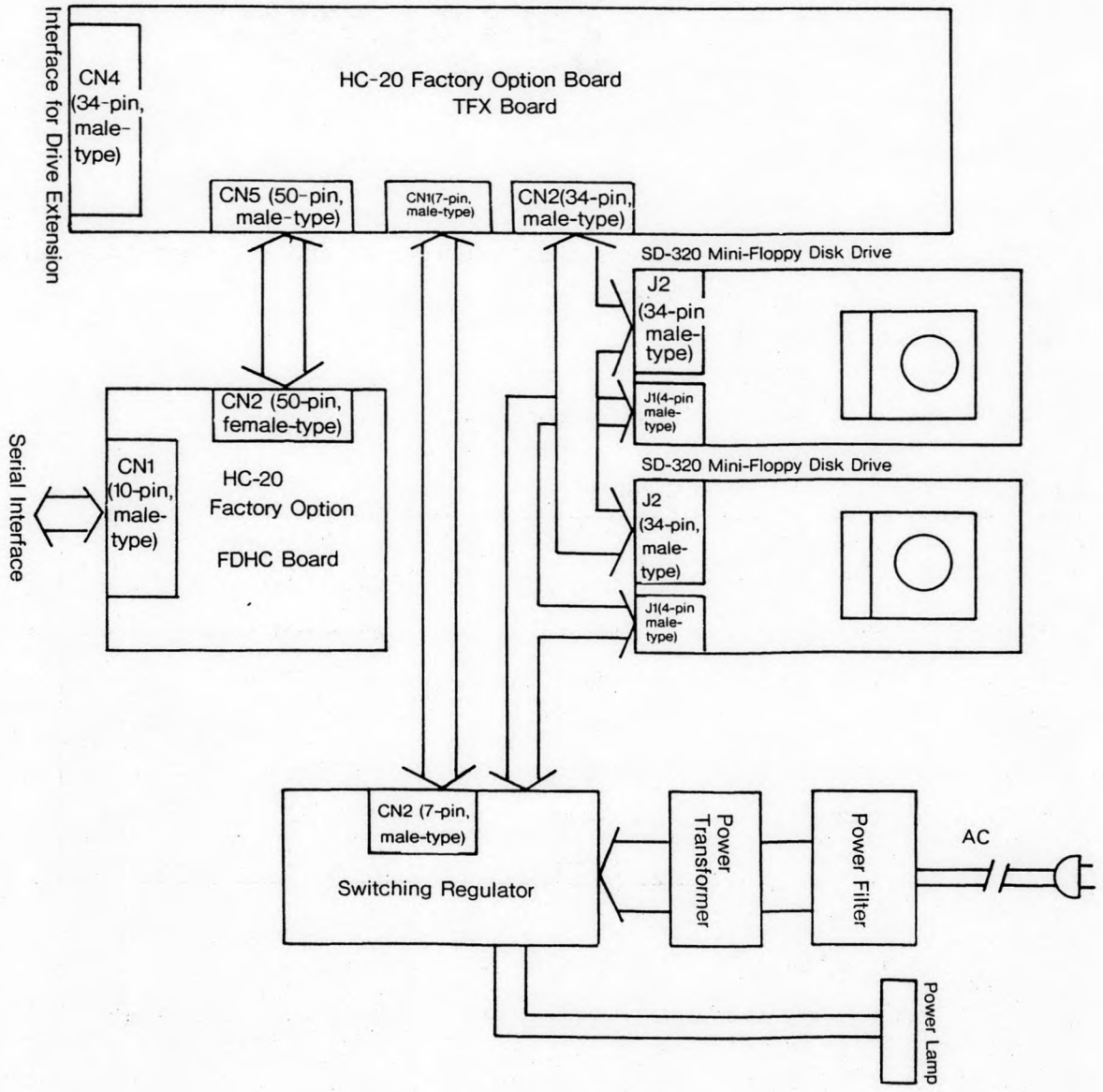
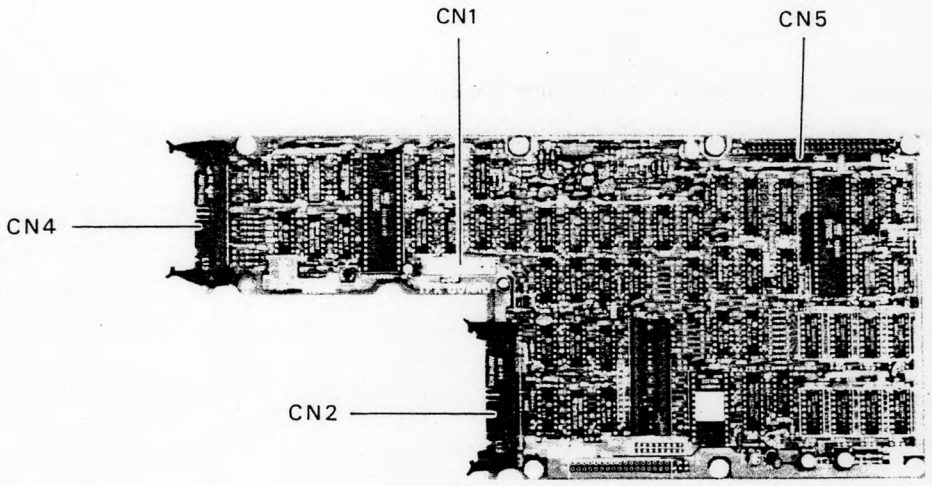


Fig. 2-1 BlockDiagram

(1) TFX Board Connectors



1) CN1 connector

(a) Use : This connector is used to supply +5V and +12V from the switching regulator board.

(b) Number of pins : 7 pins

(c) Part number : MOLEX 5275-07

(d) Pin assignment : Refer to Table 2-1 below.

Table 2-1 Pin Assignment of CN1 Connector

Pin No.	Signal	Lead Wire Color	Use
1	GND	Black	Signal GND level
2	GND	Black	Signal GND level
3	GND	Black	Signal GND level
4	+5V	Red	+5V DC
5	+5V	Red	+5V DC
6	+12V	Orange	+12V DC
7	+12V	Orange	+12V DC

2) CN2 connector

(a) Use : This connector is used to transfer the signals of floppy disk drive

(b) Number of pins : 34 pins

(c) part number : DDK FRC2-AA34-30S

(d) Pin assignment : Refer to Table 2-2 below.

Table 2-2 Pin Assignment of CN2 connector

CN2 Connector Signal Pin No.	Signal Pin No.	Signal	Direc-tion	Description
2		NC		
4	4	$\overline{\text{HOLD}}$	In	The HEAD LOAD signal at Logic "O" causes the read/write head to be loaded on the disk. (Pin 5 and Pin 6 of the DIP switch SS1 in the SD 320 mini disk drive can make head loading possible at a DRIVE SELECT signal.)
6	6	$\overline{\text{DS3}}$	In	This is the DRIVE SELECT 3 signal. Up to 4 mini disk drives can be connected in a daisy chain by the switching of the DRIVE SELECT signals. (The drive selection is made by pin 4 of the DIP switch SS1 on the SD-320 mini disk drive.)
8	8	$\overline{\text{IDX}}$	Out	The INDEX signal causes a Logic "0" pulse to be generated at each complete revolution of the floppy disk. The trailing edge of Logic "1" to Logic "0" indicates the beginning of data on the specified track.
10	10	$\overline{\text{DSO}}$	In	This is the DRIVE SELECT 0 siganl. (The drive selection is made by pin 1 of the DIP switch SS1 on the SD-320 mini disk drive.)
12	12	$\overline{\text{DS1}}$	In	This is the DRIVE SELECT 1 signal. (The drive selection is made by pin 2 of the DIP switch SS1 on the SD-320 mini disk drive.)
14	14	$\overline{\text{DS2}}$	In	This is the DRIVE SELECT 2 signal. Up to 4 mini disk drives can be connected in a daisy chain. (The drive selection is made by pin 3 of the DIP switch SS1 on the SD-320 mini disk drive.)
16	16	$\overline{\text{MON}}$	In	The MOTOR ON signal at Logic "0" causes the disk drive motor to start.
18	18	$\overline{\text{DRTN}}$	In	The DIRECTION signal determines the moving direction of the voice coil motor. The motor moves from track 00 to track 39 at Logic "0" or from track 39 to track 00 at Logic "1".

2) CN2 connector

(a) Use : This connector is used to transfer the signals of floppy disk drive

(b) Number of pins : 34 pins

(c) part number : DDK FRC2-AA34-30S

(d) Pin assignment : Refer to Table 2-2 below.

Table 2-2 Pin Assignment of CN2 connector

CN2 Connector Signal Pin No.	Signal Pin No.	Signal	Direc-tion	Description
2		NC		
4	4	$\overline{\text{HOLD}}$	In	The HEAD LOAD signal at Logic "O" causes the read/write head to be loaded on the disk. (Pin 5 and Pin 6 of the DIP switch SS1 in the SD 320 mini disk drive can make head loading possible at a DRIVE SELECT signal.)
6	6	$\overline{\text{DS3}}$	In	This is the DRIVE SELECT 3 signal. Up to 4 mini disk drives can be connected in a daisy chain by the switching of the DRIVE SELECT signals. (The drive selection is made by pin 4 of the DIP switch SS1 on the SD-320 mini disk drive.)
8	8	$\overline{\text{IDX}}$	Out	The INDEX signal causes a Logic "0" pulse to be generated at each complete revolution of the floppy disk. The trailing edge of Logic "1" to Logic "0" indicates the beginning of data on the specified track.
10	10	$\overline{\text{DSO}}$	In	This is the DRIVE SELECT 0 siganl. (The drive selection is made by pin 1 of the DIP switch SS1 on the SD-320 mini disk drive.)
12	12	$\overline{\text{DS1}}$	In	This is the DRIVE SELECT 1 signal. (The drive selection is made by pin 2 of the DIP switch SS1 on the SD-320 mini disk drive.)
14	14	$\overline{\text{DS2}}$	In	This is the DRIVE SELECT 2 signal. Up to 4 mini disk drives can be connected in a daisy chain. (The drive selection is made by pin 3 of the DIP switch SS1 on the SD-320 mini disk drive.)
16	16	$\overline{\text{MON}}$	In	The MOTOR ON signal at Logic "0" causes the disk drive motor to start.
18	18	$\overline{\text{DRTN}}$	In	The DIRECTION signal determines the moving direction of the voice coil motor. The motor moves from track 00 to track 39 at Logic "0" or from track 39 to track 00 at Logic "1".

CN2 Connector Signal Pin No.	Signal Pin No.	Signal	Direc-tion	Description
20	20	$\overline{STP}$	In	When a pulse is input to the STEP signal line, the voice coil motor, which controls the position of the read/write head, moves in the direction specified by the DRTN signal. When the WRITE GATE signal is at Logic "0", the STEP signal is inhibited.
22	22	$\overline{WTD}$	In	The WRITE DATA signal line transfers data to be written into the disk. When the input pulse falls from Logic "0", the write "0", the write current flows in the opposite direction and enters the read/write head, causing a change in the magnetic flux. This signal is valid only when the WRITE GATE signal is at Logic "0".
24	24	$\overline{WTG}$	In	The WRITE GATE signal controls both Read Data and Write Data signals. When this signal is at Logic "0", the Write Data is valid, whereas when it is at Logic "1", the Read Data is valid.
26	26	$\overline{TKOO}$	Out	The TRACK 00 signal becomes Logic "0" when the read/write head is at the track 00 position.
28	28	$\overline{WPT}$	Out	The WRITE PROTECT signal notifies the host of the disk attached with a write protect label. It becomes Logic "0" when the disk has a write protect label attached.
30	30	$\overline{RDD}$	Out	The READ DATA signal causes a pulse string of raw data to be output from the read circuit. Normally, this signal becomes Logic "0" when the inversion of magnetization exists on the disk at logic level "1".
32	32	$\overline{SSL}$	In	The SIDE SELECT signal is used to select the upper or the lower read/write head. Side 1 (upper head) is selected at Logic "0", and Side 0 (lower head) at Logic "1".
34	34	$\overline{RDY}$	Out	The READY signal becomes Logic "0" when the power is turned on and a disk loaded rotates normally (INDEX pulse : 4 pulses).
1 add ⟩ pin 33	1 add ⟩ pin 33	$\overline{GND}$		Twisted Pair Return signal GND Level.

3) CN4 connector

(a) Use : Connector for daisy chain

(b) Number of pins : 34 pins

(c) Part number : FRC2-C34U3-OL DDK

(d) Pin assignment : Refer to Table 2-2

4) CN5 connector

(a) Use : This connector is used to transfer the signals of the TFX board and the FDHC board.

(b) Number of pins : 50 pins, male-type

(c) Part number : Honda HKP-50MS3A

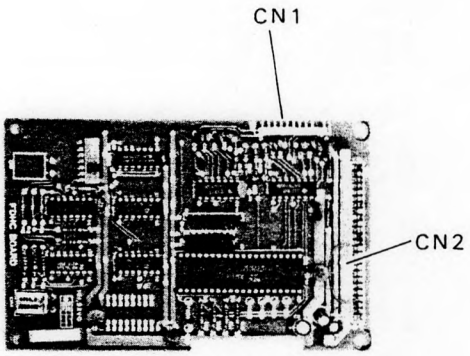
(d) Pin assignment : Refer to Table 2-3

Table 2-3 Pin Assignment of CN5 Connector

Pin No.	Signal	Direction	Description
1 ⟩ 16	ADDRESS 0 ⟩ 15	Out Out	These signals represent bits of ADDRESS signal line No. 0 to 15.
17 ⟩ 24	DATA 7 ⟩ 0	In/Out	These signals represent bits of DATA signal line No. 0 to 7.
25	GND		Twisted Pair Return signal GND level
26	+5V		+5VDC
27	GND		Twisted Pair Return signal GND level
28	$\overline{INT}$	In	Interrupt signal "Active LOW"
29	GND		Twisted Pair Return signal GND level
30	$\overline{MI}$	Out	Machine Cycle "Active LOW"
31	GND		Twisted Pair Return signal GND level
32	$\overline{IORQ}$	Out	I/O Request signal "Active LOW"
33	GND		Twisted Pair Return signal GND level
34	$\overline{MERQ}$	Out	Memory Request signal "Active LOW"
35	GND		Twisted Pair Return signal GND level
36	$\overline{RD}$	Out	Data Read signal "Active LOW"
37	GND		Twisted Pair Return signal GND level
38	$\overline{WR}$	Out	Data Write signal "Active LOW"
39	GND		Twisted Pair Return signal GND level
40	RESET	Out	Reset at "HIGH"
41	GND		Twisted Pair Return signal GND level
42	ϕ	Out	Clock Pulse

43	+5V	Out	+5V DC
44	+5V	Out	
45	+5V	Out	
46			
47	+12V	Out	+12V DC
48	+12V	Out	
49	−12V	Out	−12V DC
50	−12V	Out	

(2) FDHC Board Connectors



1) CN1 connector

(a) Use : This connector is used to transfer data from the FDHC board and the HX-20 serial interface or HX-20 display controller serial interface connector .

(b) Number of pains : 10 pins,male-type

(c) Part number : MOLEX 5049-10A

(d) pin assignment : Refer to Table 2-4 below.

Table 2-4 Pin Assignment of CNI Connector

Pin No.	Signal	Direction (as viewed from floppy)	Description
1	RXS	Out	This signal output from the terminal floppy is connected to another terminal or HX-20 serial input.
2	PINS	Out	This is the OR signal of PINC and DTRA of serial controller μPD7201 inside. This signal is not used usually.
3	TXS	In	This is a serial input signal to the terminal floppy from the HX-20.
4	POUTS	In	This input signal is connected to the CTSA terminal of serial controller μ PD7201 inside via the line receiver. In means that a serial output at "HIGH" level is permitted.
5	GNDS	—	GND
6	GNDC		GND
7	POUTC	Out	This output signal functions the same way as the POUTS signal. (It is used in this application.)
8	TXC	Out	This serial signal output from the terminal floppy is connected to another terminal (display controller) of the HX-20.
9	PINC	In	The OR signal of this signal and DATA of the serial controller μPD7201 is output at PINS. (It is not used in this application)
10	RXC	In	When this input signal is at "LOW" level, a signal from the terminal floppy is output from RXS.

2) CN2 connector

(a) Use : This connector is used to transfer the signals of the TFX board and the FDHC board.

(b) Number of pains : 50 pins,male-type

(c) Part number : HKD-50FD2-3A

(d) pin assignment : Refer to Table 2-5 below.

Tab. 2-5 Pin Assignment of CN2 connector

Pin No.	Signal	Direction	Description
1	ADRESS 0	IN	These signals represent bits of ADDRESS signal line Nos. 0 to 7.
2	1	IN	
3	2	IN	
4	3	IN	
5	4	IN	
6	5	IN	
7	6	IN	
8	7	IN	
9	NC		
10	NC		
11	NC		
12	NC		
13	NC		
14	NC		
15	NC		
16	NC		
17	DATA 7	In/Out	These signals represent bits of DATA signal line Nots. 0 to 7.
18	6	OUT	
19	5	In/Out	
20	4	In/Out	
21	3	In/Out	
22	2	In/Out	
23	1	In/Out	

24	DATA 0	In/Out	
25	GND		Twisted Pair Return signal GND level
26	+5V		+5V DC
27	GND		Twisted Pair Return signal GND level
28	NC		
29	GND		Twisted Pair Return signal GND Level
30	NC		
31	GND		Twisted Pair Return signal GND Level
32	IORQ	In	I/O Request signal "Active LOW"
33	GND		Twisted Pair Return signal GND level
34	NC		Twisted Pair Return signal GND Level
35	GND		
36	RD	In	Data Read signal "Active LOW"
37	GND		Twisted Pair Return signal GND level
38	WR	In	Data Write signal "Active LOW"
39	GND		Twisted Pair Return signal GND level
40	RESET	In	Reset at "HIGH"
41	GND		Twisted Pair Return signal GND level
42	ϕ	In	Clock Pulse
43	5V	In	5V DC
44	5V	In	
45	5V	In	
46			
47	12V	In	12V DC
48	12V	In	
49	12V	In	12V DC
50	12V	In	

(3) Setting of DIP and DIC Switches

1) TFX board DIP switches

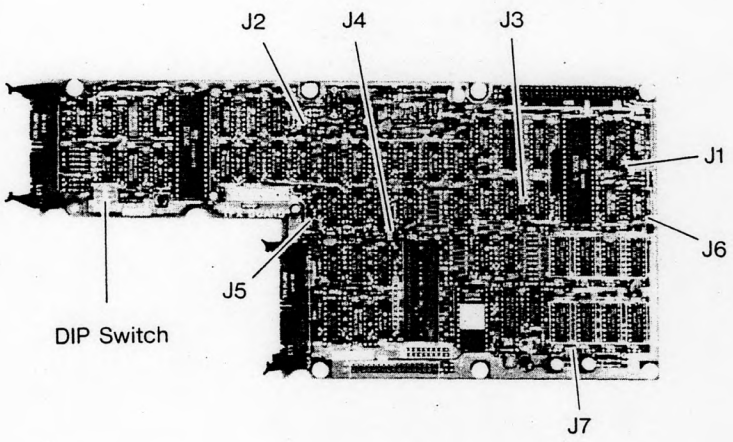


Table. 2-6 Setting of TFX Board DIP Switches

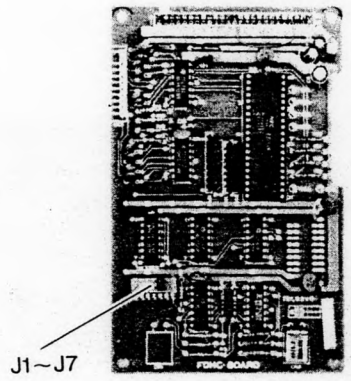
DIP Switch	Description	A & B Drive	C & D Drive
1	Drive extension	ON	ON
2	〃	ON	ON
3	〃	ON	ON
4	〃	ON	OFF

2) TFX board DIC switches

Tab. 2-7 Setting of TFX Board DIC Switches

Jamper No.	Description	At Shipment
J1	1 : 16kbyte (μPD416-3) mounted 2 : 64kbyte (μPD4164-3) mounted	2
J2	1 : Precompensation for write assurance 2 : None	2
J3	1 : 2732 2 : 2726 mounted 3 : 2332	2
J4	1 : 2732 2716 mounted 2 : 2332	1
J5	1 : μPD765AC always ready 2 : FDD READY	1
J6	1 : 16kbyte (μPD416-3) mounted 2 : 64kbyte (μPD4164-3) mounted	2
J7	1 : 16kbyte (μPD416-3) mounted 2 : 64kbyte (μPD4164-3) mounted	2

3) FDHC board DIC switches



Tab. 2-8 Setting of FDHC Board DIC Switches

Jamper	Description	At Shipment
J1	Serial baud rate 2400 bps	OFF
2	〃 4800	OFF
3	〃 9600	OFF
4	〃 19.2k	OFF
5	〃 38.4k	ON
6	〃 76.8k	OFF
7	Baud rate generating quartz swtching ON : CR1 selection OFF : CR2 selection (4. 9152 MHz)	OFF

4.2.3 Principles of operation

In the TF-20 (exclusive use with HX-20),the 2KB ROM2716 starts to run at the supply of power and copies its own $100 to $500 into the $F800 to $FC00 of the 64KB Dynamic RAMμPD4164-3.Then the program counter it transferred to $F800,the ROM is separated and oparation is made according to the program within the DRAM.

The parameter data necessary for file management is transferred serially from the HX-20 handheld computer.Therefore,the parallel ／serial data conversion is made by the multi-protocol serial controller μPD7201.The TF-20(exclusive use with HX-20)has file management and other intelligent functions,which are executed by CPU μPD78OC-1,64KBDRMμPD4164-3 and FDC μPD765AC.

The SD-320 mini-floppy disk drive outputs the IDX signal to determine the beginning of track,the TK00 signal to show the read／write hand in the track 00 position,and the RDY signal to identify the nomal rotation of the disk.Also,the WPT signal is output to identify the presence or absence of writing into the disk.

These four signals determine the operation of the floppy disk.The signals sent to the disk drive are the drive signal for the drivehead solenoid,the drive signal for the disk drive motor and the control signal for the head positioning VCM mechanism.

All these signals are converted to match the operation timings of the various mechamism by the custom LSI SDF 9401F on the control circuit board within the disk drive.And the mechanisms of the disk drive performs operations according to these signals.

4.2.4.1 Electrical Circuit

Fig. 2-2 shows the block diagram of the whole circuit of TF-20 (exclusive use with HX-20)

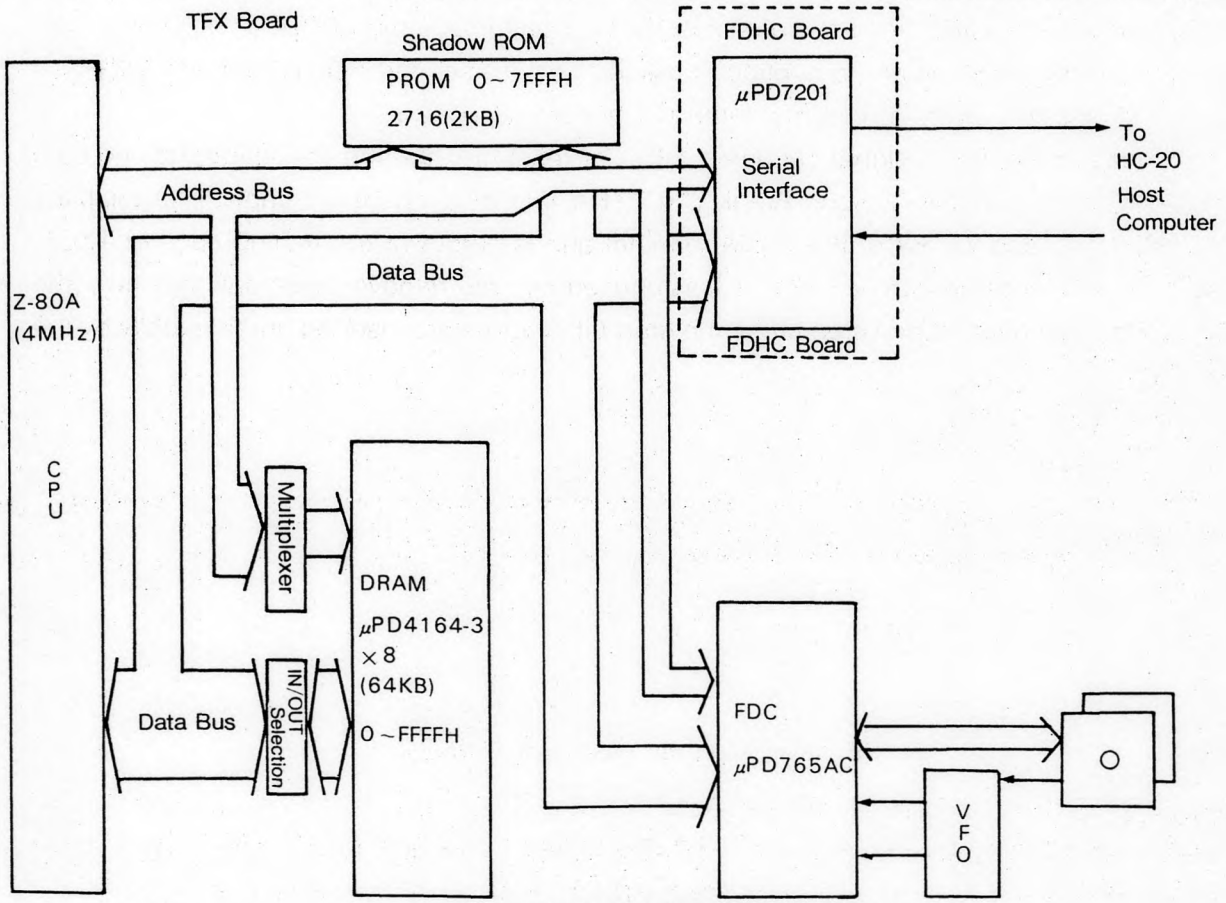


Fig. 2-2 Block Diagram of TF-20

(1) Function and role of multi-protocol serial controller

Transfer of parameter data between the HX-20 handheld computer and the TFX board requires parallel/serial data conversion. This function is performed by μPD7201 of the FDHC board. Fig. 2-3 shows the layout of components of the FDHC board,and Fig. 2-4 its circuit diagram. These are followed by an explanation on the transmission and reception operations of the multi-protocol serial controller μPD7201C.

Fig. 2-3 Component Layout of FDHC Board

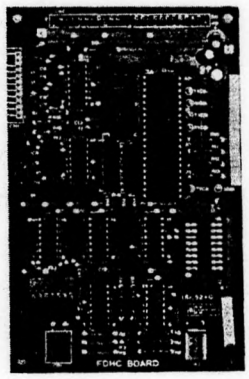
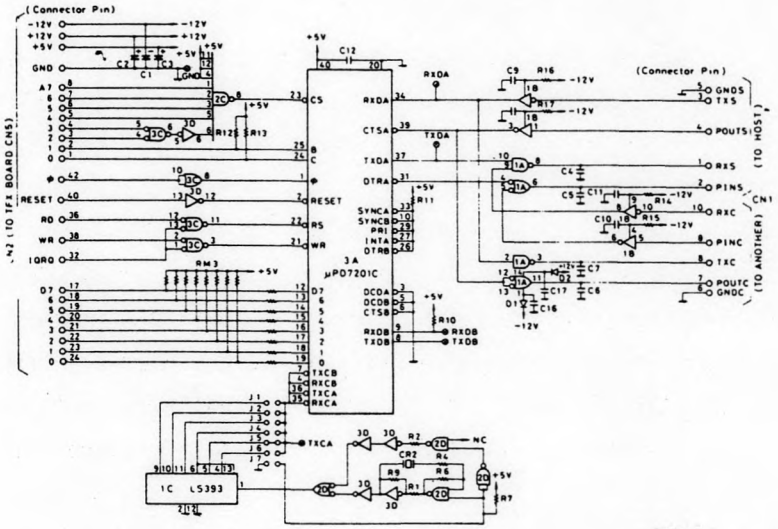


Fig. 2-4 Circuit Diagrm of FDHC Board



The μPD7201 performs data communication asynchronously.When the POUTS signal from the HX-20 reaches the "HIGH" level,the output at the $\overline{\text{CTS}}$ terminal of the μPD7201 becomes "LOW", thus making transmission and reception possible.At the same time, POUTC is made "HIGH",so that communication with an external interface becomes possible.

In transmission,the TXDA signal becomes "HIGH"at reset or when the transmitter has no data and "LOW" at the setting of Send Break.The TXDA transmission late is capable of enabling x1,x1/16,x1/32 and x1/64 of the $\overline{\text{TXCA}}$ terminal and is output at the trailing edge of TXCA. Where the character length is 7 bits or less,unused bits are removed automatically from the data string.The parity bit and stop bit by the start bit program are inserted automatically by the μPD7201.

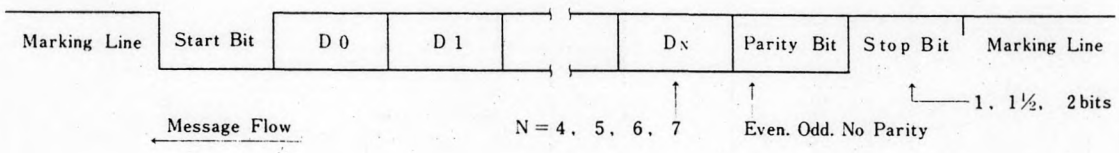


Fig. 2-5 Asynchronous Message Format

Reception becomes possible when the $\overline{\text{DCDA}}$ input is "LOW".The start bit is confirmed at the detection of "LOW" in the RXDA input and "LOW" again 1/2 bit time later.In the x1 clock mode, RXDA performs sampling at the leading edge of $\overline{\text{RXCA}}$.Where the character length is 7 bit or less,"HIGH" is inserted in unused bits.

4.2.4.2 Function and role of TFX board

The TFX board comprises the Z80 CPUμPD780C of 4MHz clock frequency,the 2KB ROM2716,the 64KB DRAM for file management and the FDC (floppy disk contmoller) μPD765AC for direct control of the floppy drive.

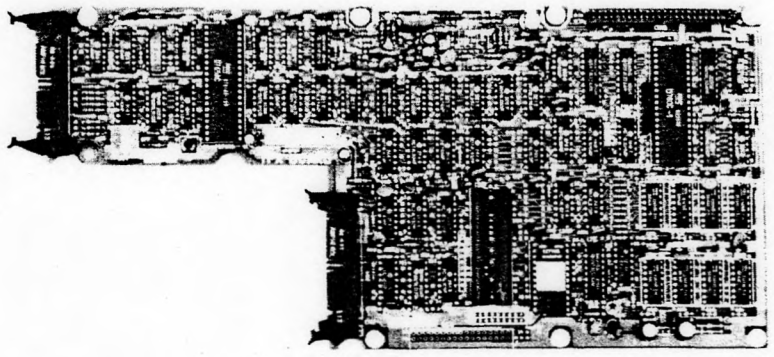


Fig. 2-6 Component Layout of TFX Board

Fig.2-6 shows the component layout of the TFX board.Fig.2-7 shows the block diagram of the circuits of the TFX board.

In the following sections,explanation is given on the operations of these circuits.

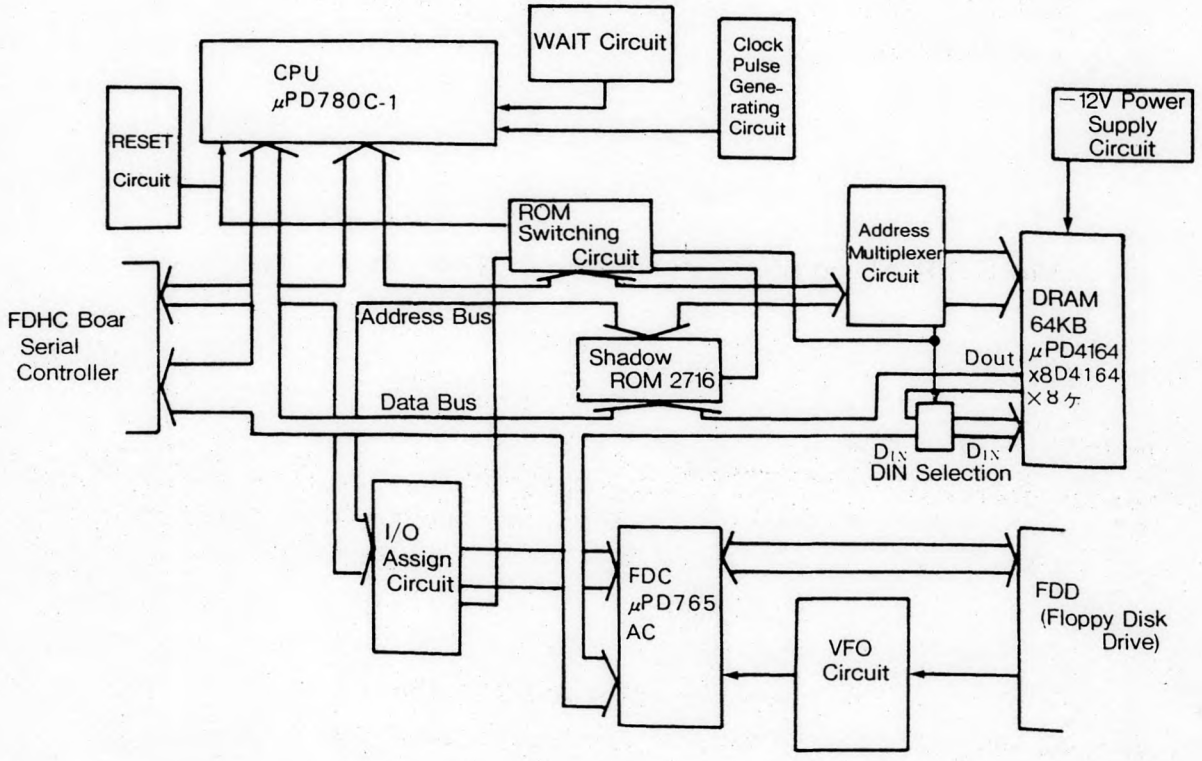


Fig. 2-7 Block Diagram of TFX Board

4.2.4.3 RESET circuit and ROM/RAM switching circuit

A maximum of 64KB memory can be accessed directly via the 16-bit address bus of A0 to 15 of CPU.

The TF-20 for exclusive use with the HX-20 is a system with all of the 64KB memory space made up of DRAM.In this memory constitution,however,DRAM is blank at the turning on of power. Accordingly,the contents of IPL (Initial Program Loader) ROM are copied on DRAM at power ON. Fig. 2-8 shows the memory map at this point. The contents of 100H to 500H of the 2BK ROM are FCooH on DRAM,and the 2KB ROM is separated.

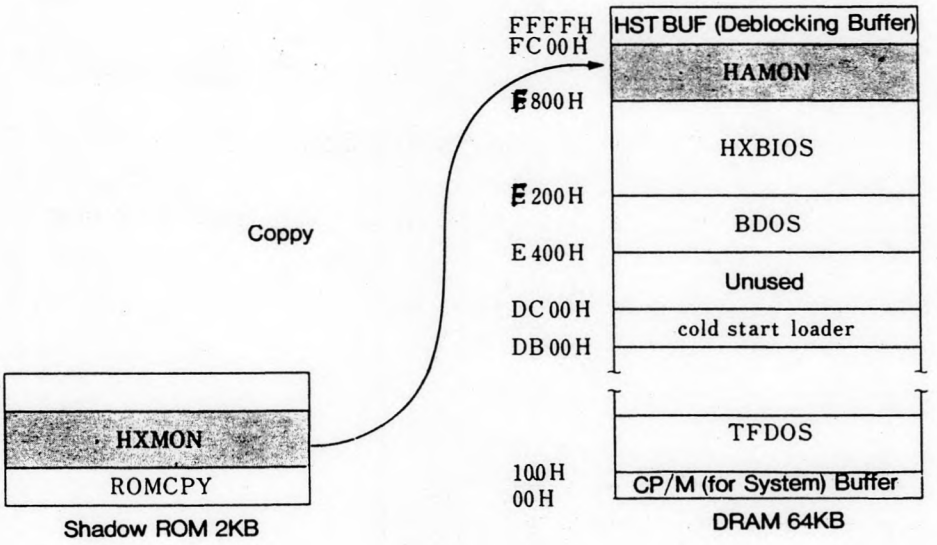


Fig. 2-8 ROM and DRAM Memory Map of TF-20 (for HX-20)

Fig. 2-9 shows the RESET circuit and the ROM/RAM switching circuit.

At power ON,TrQ1 is brought through "Cut off"⟶"ON" by R55,ZD3,R56 behind the leadind edge of the +5V line.At this timing,a Reset signal at "LOW" level is output from pin 13 of 21C.The Reset signal passes pin 3 of 22C,thus resetting 12B,and turns pin 9 of 16D to "LOW" level from pin 9.With pin 9 of 16D at "LOW" level,selection can be made by the address lines A12 to A15 for ROM to be active and for DRAM to be in the input condition.

At the completion of copying the contents of ROM into DRAM,address XXF6H is output.Since address line 0 bit and 3 bit are at "LOW" level,an output of "LOW" level is made at the Preset terminal pin 10 of 12B by LS139 of 11E and LS155 of 12D,which outputs "HIGH" level at pin 9 of 16D. Upon this,the CE terminal of ROM pin 18 of 15E is fixed at "HIGH" level and the ROM is separated. separated.

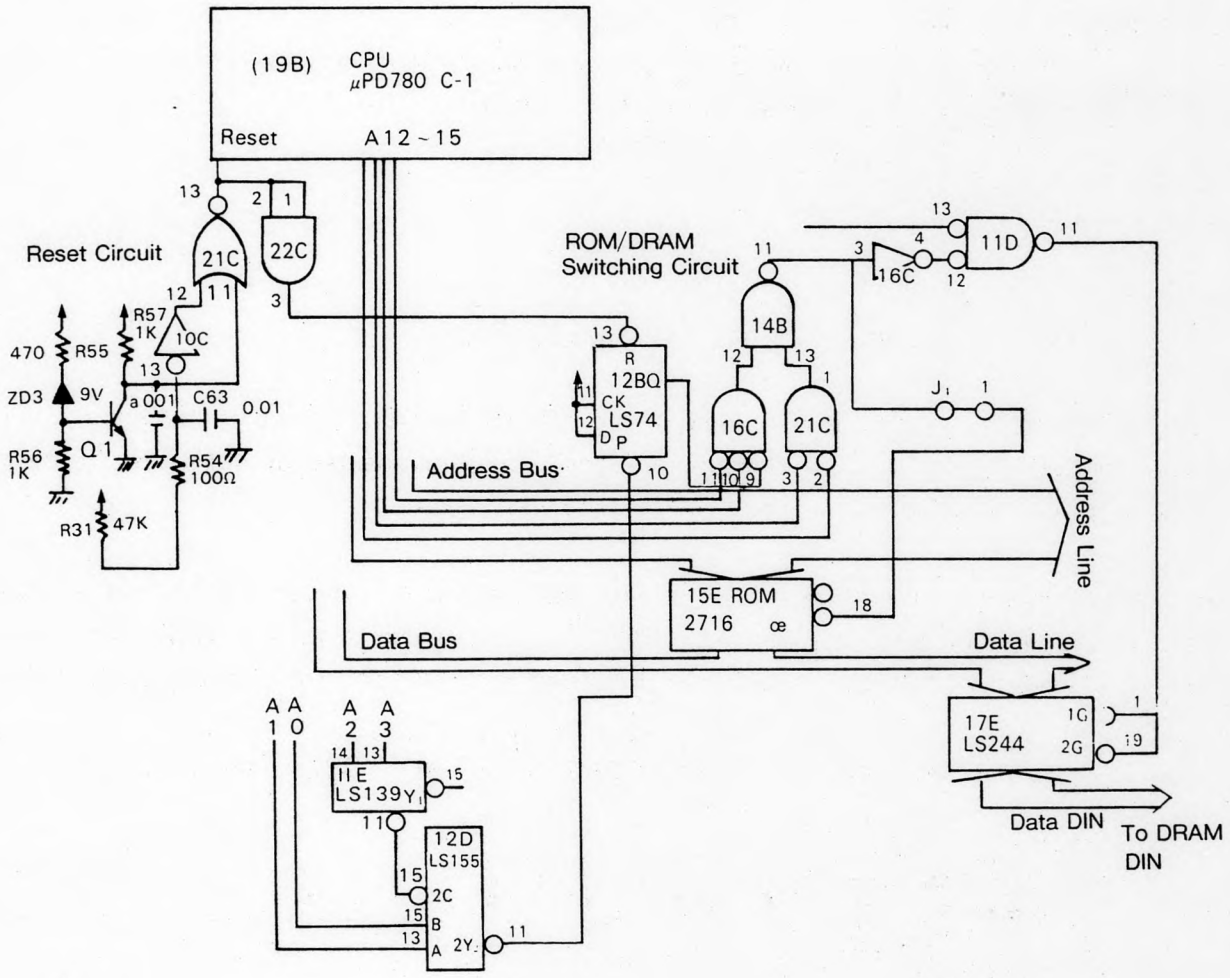


Fig. 2-9 RESET Circuit and ROM/RAM Switching Circuit

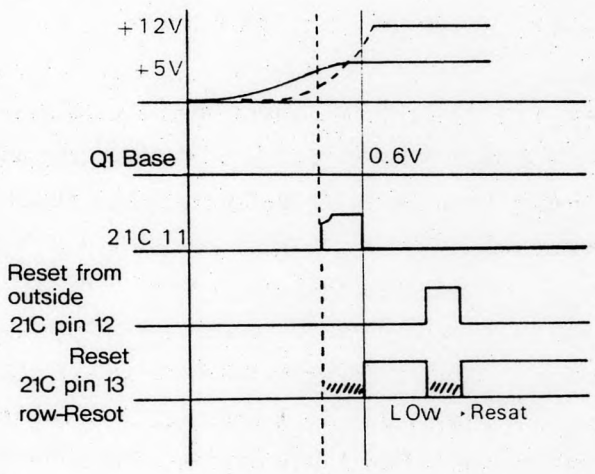


Fig. 2-10 Time Chart of Reset Circuit

4.2.4.4 Clock pulse and WAIT signal

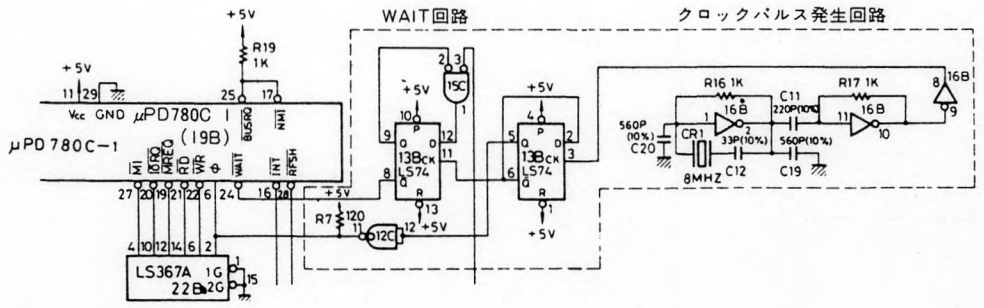
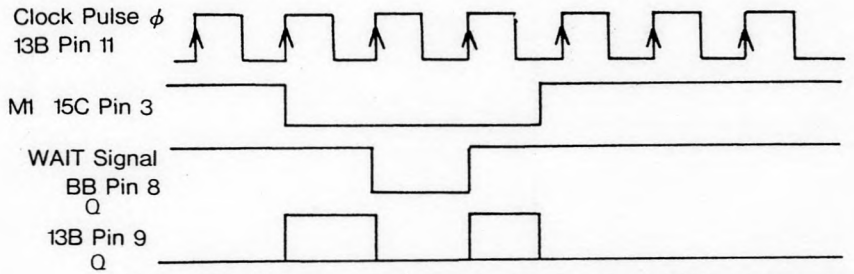


Fig. 2-11 Clock Pulse and WAIT Circuit

Data missing due to the data transfer time (1 byte／32 μS)between FDC (controller) and the floppy disk in the MFM system (double-side double-density) is compensated by 4MHz supplied to the clock pulse (ϕ) by using the Z80 high-speed CPU μPD780C-1.

As is shown in Fig.2-11,the clock pulse from the 8MHz quartz crystal oscillator circuit is input to the clock terminal of the D type flip-flop 13B (SN7474).As the truth value of SN7474 shows,it is frequency-divided at 13B,wave-shaped by the inverter of 12C and input to the clock terminal of CPU.

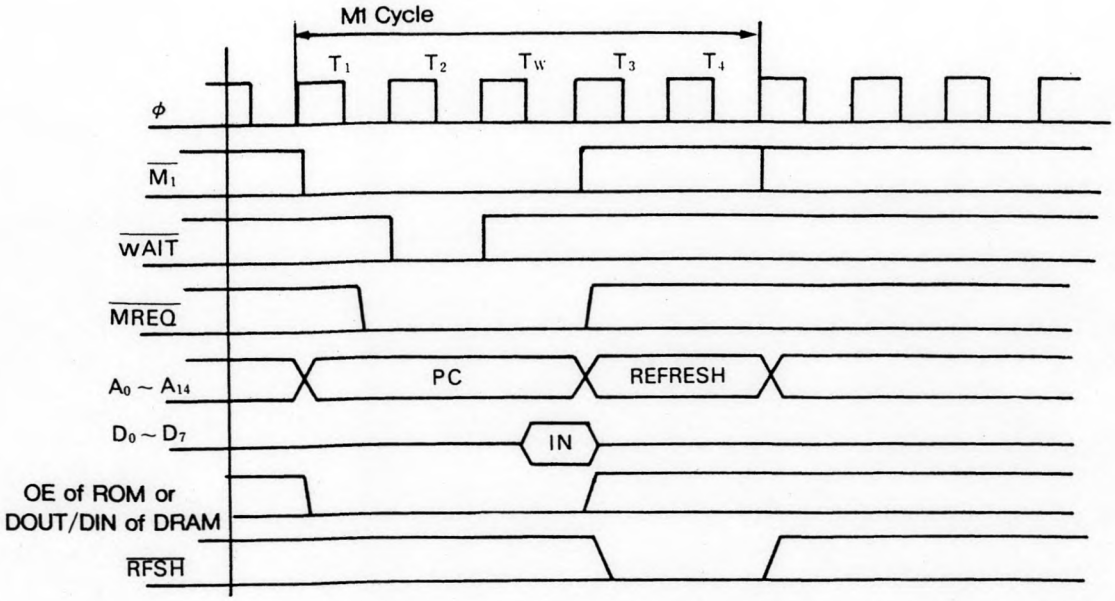
FiG.2-12 shows the timing chart of the WAIT signal circuit when CPU is disregarded.



Note : This timing chart represents the case where CPU is disregarded.

Fig. 2-12 Timings Chart of WAIT Circuit

As Fig. 2-12 shows,the WAIT signal becomes "LOW" after one clock cycle behind the "LOW" level of M1 cycle and repeats the flip-flop action as long as the M1 cycle remains at the "LOW" level. With the M1 cycle rising to the "HIGH" level,the WAIT signal becomes "HIGH",stopping the flip-flop action. Fig. 2-13 shows the actual timing chart of the M1 cycle (intruction fetch cycle). At the start of M1 cycle,the contents of the program counter (PC) are output on the address bus (A0 to A14). 1／2 clock later,the $\overline{\text{MREQ}}$ signal becomes "LOW" and simultaneously a R／W signal is output. Now the "LOW" level is selected to the $\overline{\text{OE}}$ signal for ROM or the DOUT／DIN and WE signals for DRAM,and instruction is given for data read of ROM or write／read of DRAM. Then at the trailing edge of T2 state,the WAIT signal shown in Fig. 2-12 is read and the same condition as 1 state is maintained. At Tw state,CPU and memory access time is adjusted before geing to T3 state. CPU reads D0 to D7 at the leading edge of T3 state.



Note : The M1 cycle is the basic unit in the execution of an instruction by CPU

Fig. 2-13 Timings Chart of CPU and WAITSignal

4.2.4.5 I/O assign circuit

Fig. 2-14 shows the I/O assign circuit using addresses A0 to A7 and R/W signal. Operation of the decoder/demultiplexer TTL IC of 11ELS139 and 12DLS155 enables the switching of ROM2716, reading of the DIP switch,setting of the operation mode of μPD765 and ON-OFF control of the drive motor.

Table 2-9 shows the I/O assignment table.

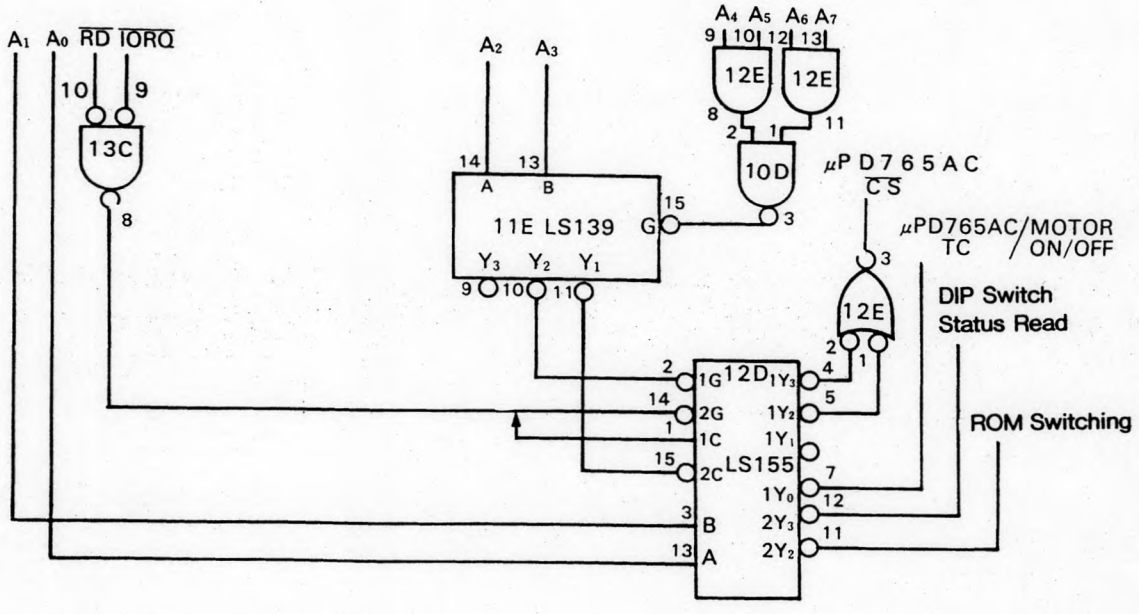
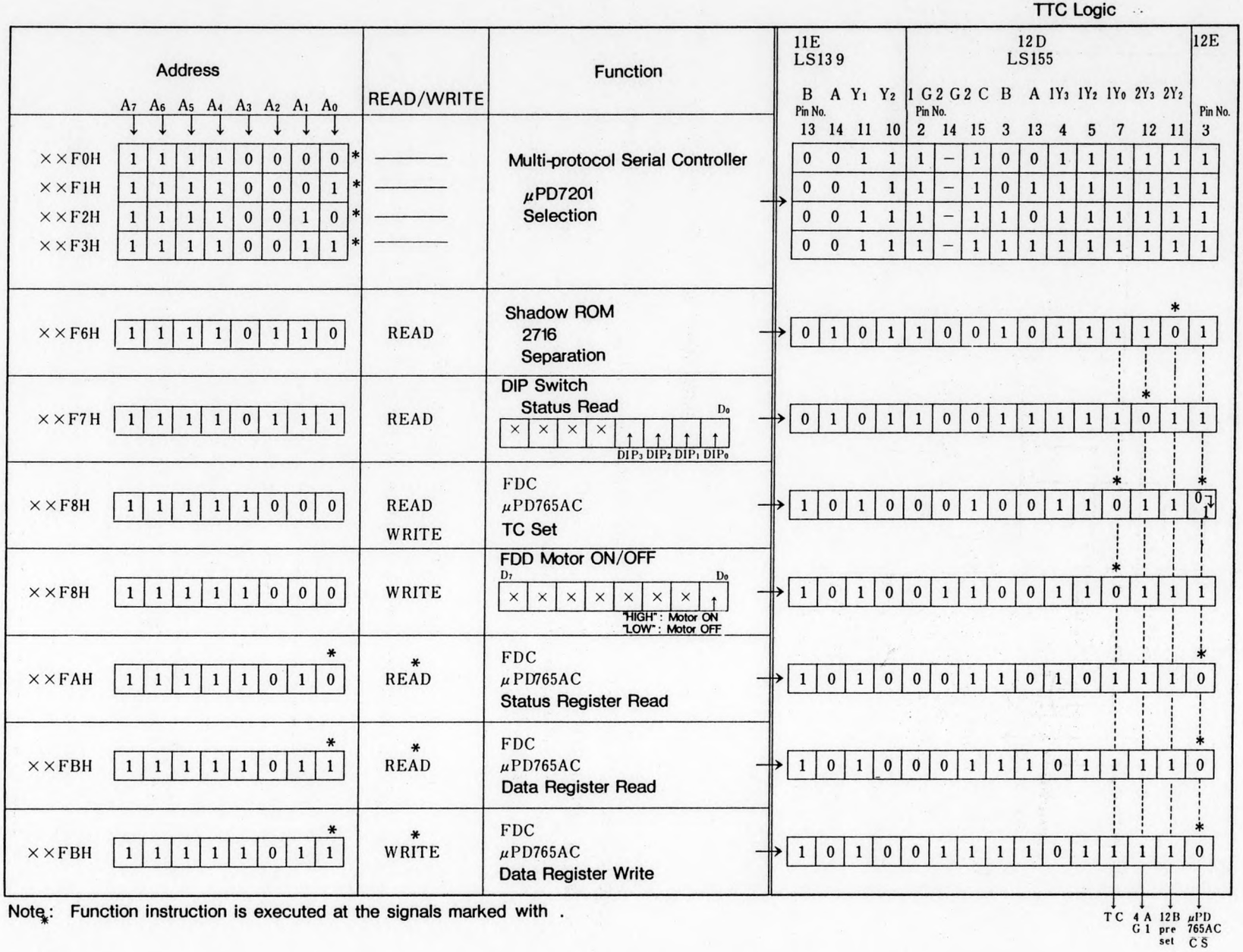


Fig. 2-14 I/O Assign Circuit



Note: * Function instruction is executed at the signals marked with .

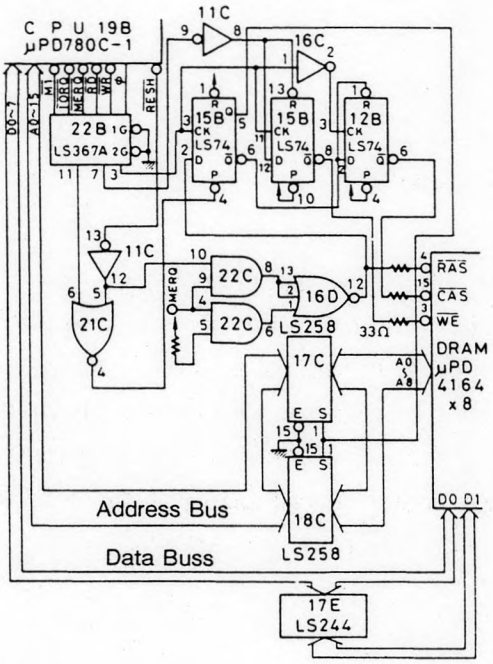
Table 2-9 I/O assignment table

4.2.4.6 Address multiplexer circuit

16 bits of addresses A0 to A15 are required to access any one byte in the 64KB DRAM. DRAM μPD4164 is set twice,8 bits at a time.The address call in DRAM consists of 256 (rows) x 256 (columns) . The low addresses A0 to 7 are taken into the low buffer by the $\overline{RAS}$ clock pulse, whereas the column addresses A8 to 15 are taken into the column butter at the trailing edge of $\overline{CAS}$ clock pulse.

Fig.2-15 shows the address multiplexer circuit of DRAM μPD4164-3.

Fig. 2-15 Address Multiplexer Circuit of TFX Board



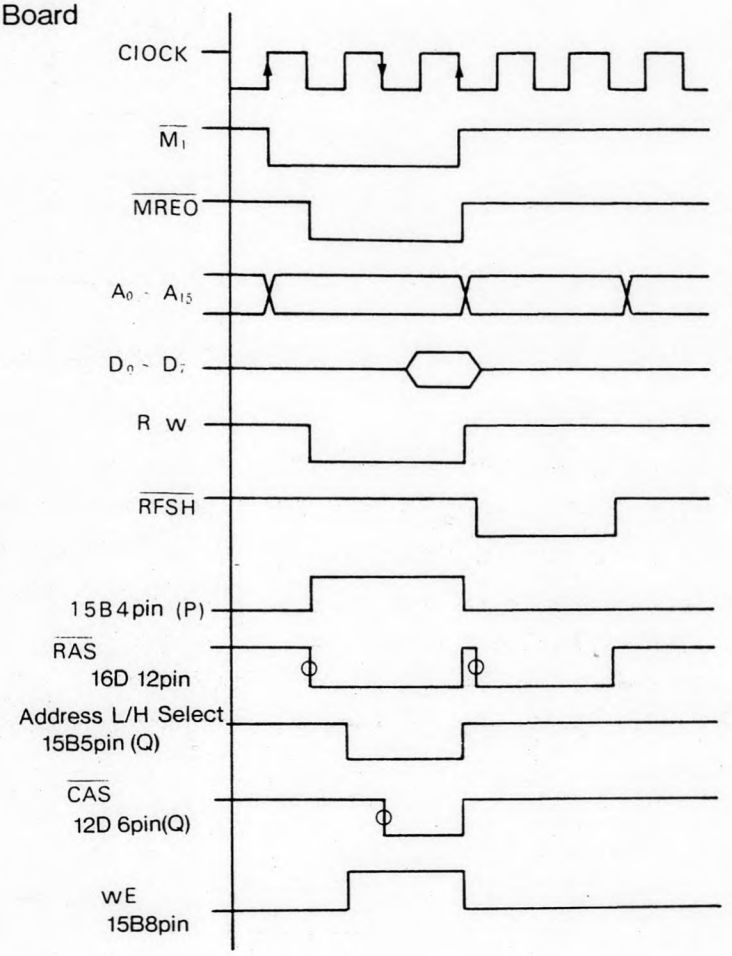


Fig. 2-16 Timing Chart of RAS and CAS Signals

The timing of the $\overline{RAS}$ and $\overline{CAS}$ signals is made mainly by the IC of LS74 of 15B and 12B.
At the output of $\overline{MERQ}$ of CPU,pin 12 (RASsignal) of 16D goes through "HIGH ⟶LOW" level change.At this point,pin 5 of 15B is at "HIGH" level and therefore 17C and 18C are in the "A Input ⟶ Y Output" state,thus causing the addresses A0 to A7 to be taken into DRAM.
At the leading edge of the next clock pulse,pin 5 of 15B goes "LOW" and 17C and 18C enter the "B Input ⟶ Y Output" state,causing the A7 to A15 address selection.
The $\overline{CAS}$ signal is output from pin 6 ($\overline{Q}$) of 12B at the trailing edge of the clock pulse after the change of address selection,and DRAM takes in A7 to 15.

At the RFSH signal of CPU,the $\overline{RAS}$ signal only is output because pin 4 (P) of 15B is preset.
Fig.2-16 shows the timing chart of the RAS and CAS signals.

4.2.4.7 −12V chopper type regulator circuit

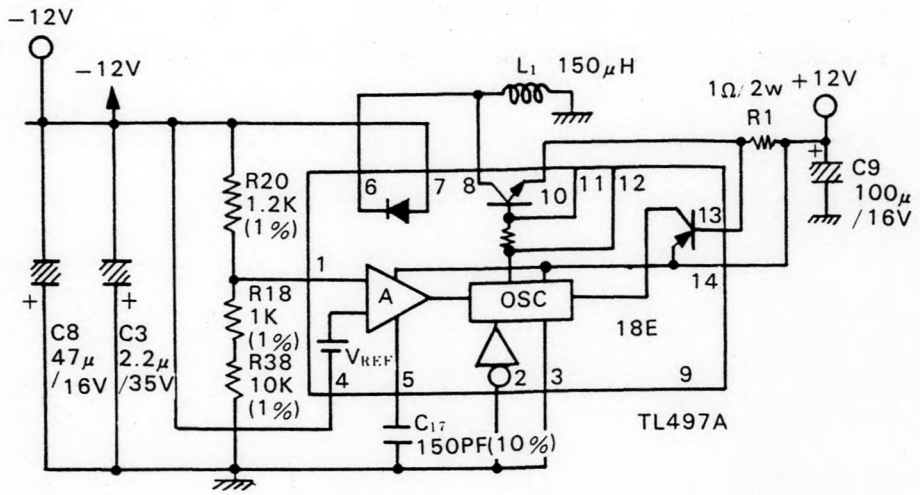


Fig. 2-17 −12V RegulatorCircuit

Fig.2-18 shows the principle of operation of the −12V chopper type regulator circuit. When Tr is on,energy is stored in inductance L for the time ton.And when Tr is off,the current flows from the load to L.Consequently,the electric potential at the top of L,or the Cathode side of diode D,turns negative and turns D on,thus charging the output capacitor C in the direction as shown in Fig.2-18.The output voltage is controlled by the time ton.In an actual circuit,the output voltage is divided by R20,R18 and R38,compared with the reference voltage VREF by OPAMP in TL49TA and made into −12V after increasing or decreasing the frequency of OSC.

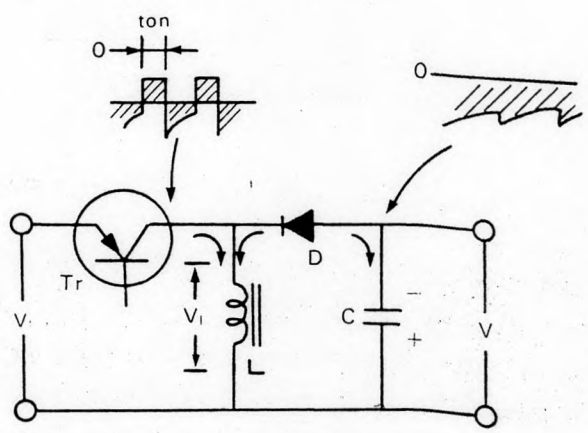


Fig. 2-18 Principle of Operation

4.2.4.8 VFO circuit

FDC μPC765AC requires the read date and clock bit window in separating date only from the read date combined with the pulse or in detecting a clock bit lost in the address mark.

The VFO circuit has a constitution as shown in Fig.2-19.

In the disk format for the TF-20 (exclusive use with HX-20) there is a Sync fild at the top of the ID field and at the top of the data field as shown in Fig. 2-20. Since this Sync field comprises "00" data,there is only a clock pulse train of epual intervals (4μS). By locking (synchronizing) with the read pulse train of this Sync field,a corret window can be obtained. Fig. 2-21 shows the relationship between the read and the clock window.

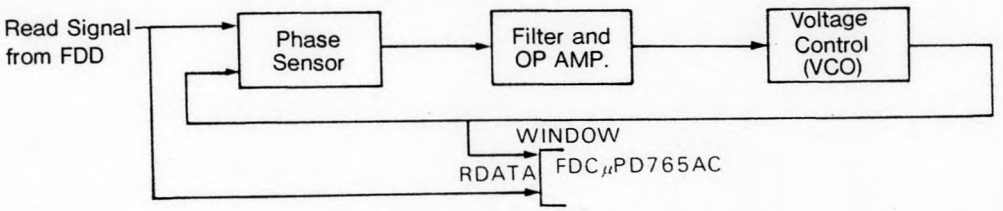


Fig. 2-19 Block Diagram

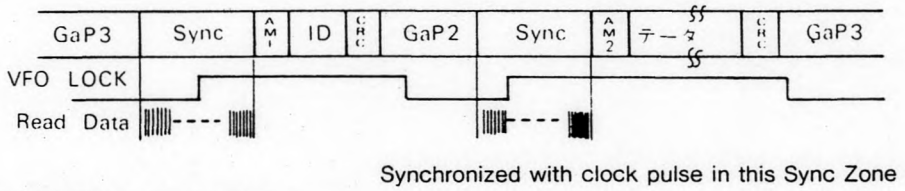


Fig. 2-20 Clock Pulse and VFO in Sync Zone

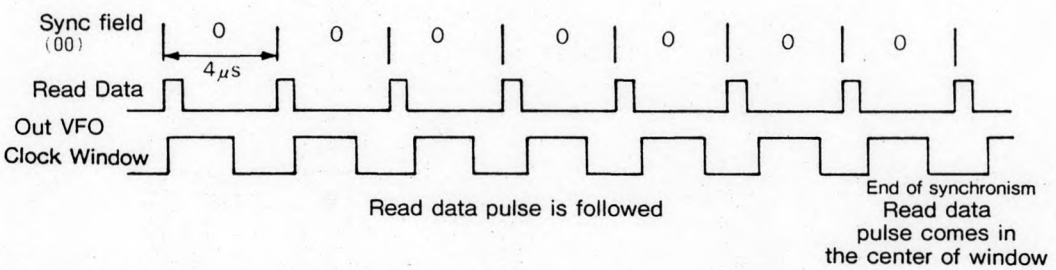


Fig. 2-21 Read Data and Clock Window

The VFO circuit on the TFX board can use either the MFM mode or the FM mode through program operation.

The instruction of MFM or FM mode to the VFO circuit is output from the pin 26 MFM terminal of FDC765C.The MFM mode is selected for "HIGH" level,and the FM mode for "LOW" level.

The VFO circuit operation in the MFM mode is explaind first in the following.

In this mode,the pin 26 MFM terminal of FDC μPD765C is at "HIGH" level and accordingly pin 1 of 9B and pin 1 of 11B become "LOW" .And pin 5 of 9B becomet "LOW" at the Reset state,and pin 11 and pin 2 of 11B are output at pin 9 and pin 4,respectively.Hence,pin 13 of 15C are fixed at "LOW" level and pin 8 of 11D at "HIGH" level.

At the output 4V～5V from pin 7 of OPAMP4558 of 12A,LS221 (multivibrator) of 10B begins to vibrate at the time constant of R35 and C13 or the time constant of R36 and C14.This pulse is frequency-divided by the synchronous binary counter LS161 of 7A.

The read data from FDD (floppy disk drive SD-320) entering pin 10 of 8A takes a pulse waveform at the leading edge.It is then output from pin 5 of 8A and enters pin 23 RDATA of FDC μPD765.

At the same time,it is again pulse-shaped by the monostable multivibrator 8A LS221 having pulse-width variable VR and output from pin 13 of 8A.

At the trailing edge of pin 14 (QA) of 7A,the output from pin 13 of 8A is output from pin 9 of 8B. It goes to pin 5 of 17D by way of pin 11 and pin 9 of 11B,and an inverted signal is input to pin 5 of 16D.

Pin 13 (QB) of 7A is connected with pin 22 WINDOW of FDC μPD765 by way of pin 2 and pin 4 of 11B.

Fig.22 shows the VFO circuit in this mode.

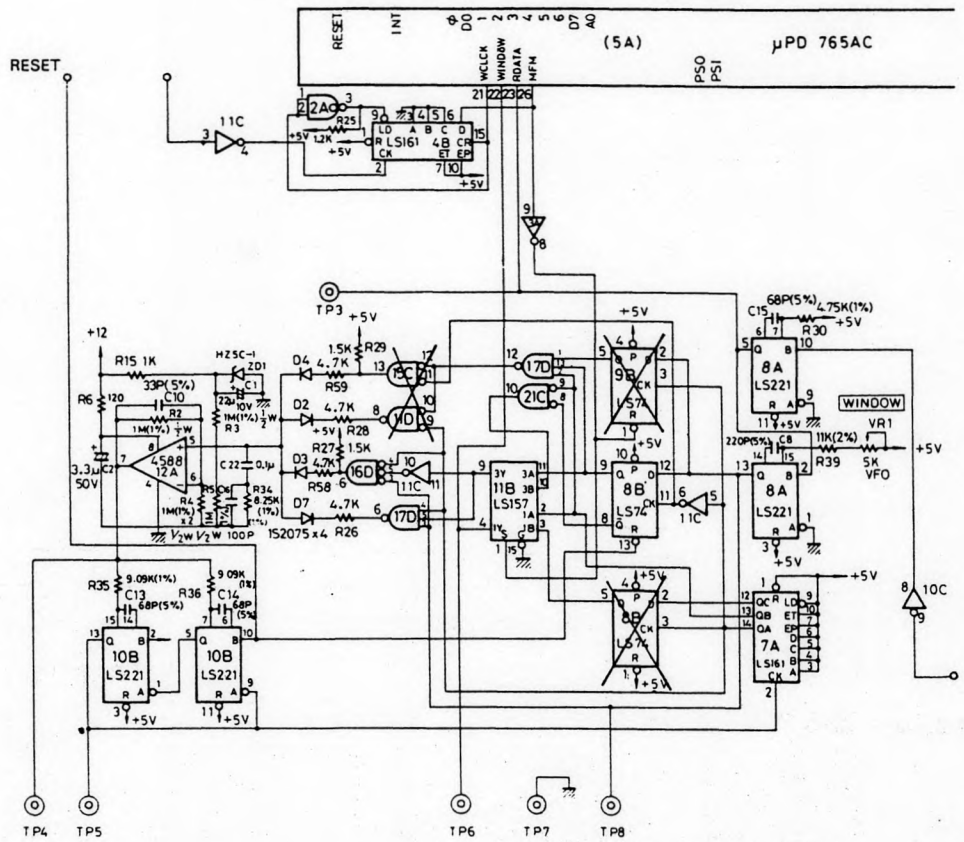


Fig. 2-22 VFO Circuit

Fig.2-23 shows the waveforms at various points.

The trailing edge timing of read data is output in pulse from pin 5 of 8A by the operation of the one-shot multivibrator.From pin 13 of 8A,one-shot pulse with 2μs pulse width from the reading edge of pin 5 of 8A is output as shown in Fig.2-23.

The multivibrator of 10B vibrates at 1MHz,and a clock output of 1μs pulse width is made from pin 14 (QA) of 7A as shown in Fig.2-23. Pin 9(Q) of 8B latches the state of pin13 of 8A at the trailing edge of QA pulse.

Pin 1 of 11B,being at "LOW" level,is connected to "A Input ⟶ Y Output".
When the trailing edge of read data coincides with the center of WINDOW,pin 6 of 16D is "LOW" and pin 6 of 17D "HIGH",and 4V~5V is output from pin 7 of 12A.

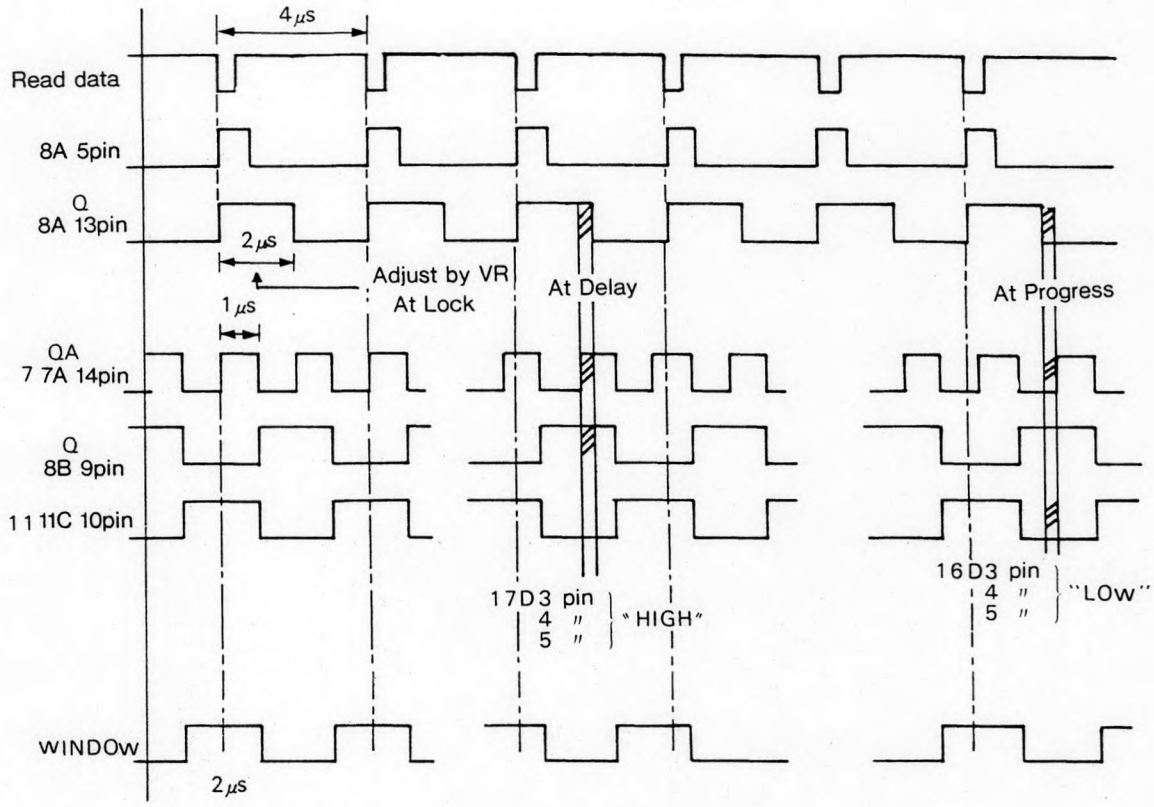


Fig. 2-23 Timing Chart of VFOCircuit on TFX Board

When the center point of WINDOW falls behind the trailing edge of read data,pins 3,4 and 5 of 17D become "HIGH","OV" is given to plus input of OPAMP of 12A,and "OV" is output from pin 7 of 12A.Then the WINDOW center is adjusted to the trailing edge of read data by enlarging the time constant of the multivibrator of 10B and lessening the clock frequency.
Also,when the trailing edge of read data has progressed before the WINDOW center,pins 3,4 and 5 of 16D become "LOW","+5V" from pin 6 is supplied to 12A and "+5V"from pin 7 of 12A is output to 10B.As a result,the clock frequency is quickened,so that the WINDOW center is adjusted to the trailing edge of read data.
The timing of WINDOW and read data is adjusted to the "2μs" pulse width of pin 13 of 8A by the semifixed resistamce VR.However,this timing,if it goes wrong,can cause R/W errors.Although the TF-20 for the HX-20 employs the MFM mode only,the VFO circuit is provided with the WINCOW pulse generating circuit for FM so that the FM mode can be activated by program change of ROM of 15E.The WINDOW pulse of 4μs pulse width is adjusted to the clock timing of read data by the clock timing of pin 14 QA and pin 13 QB of 7A.

4.2.4.9 FDC μPD765AC

FDC μPD765AC is a floppy disk control LSI incorporating the control program.Having the status register and data register inside,it performs R/W operation and Seek operation together with the floppy disk drive SD-320 at instructions from CPU.

Fig.2-24 shows a simplified flow chart of R/W Operation.

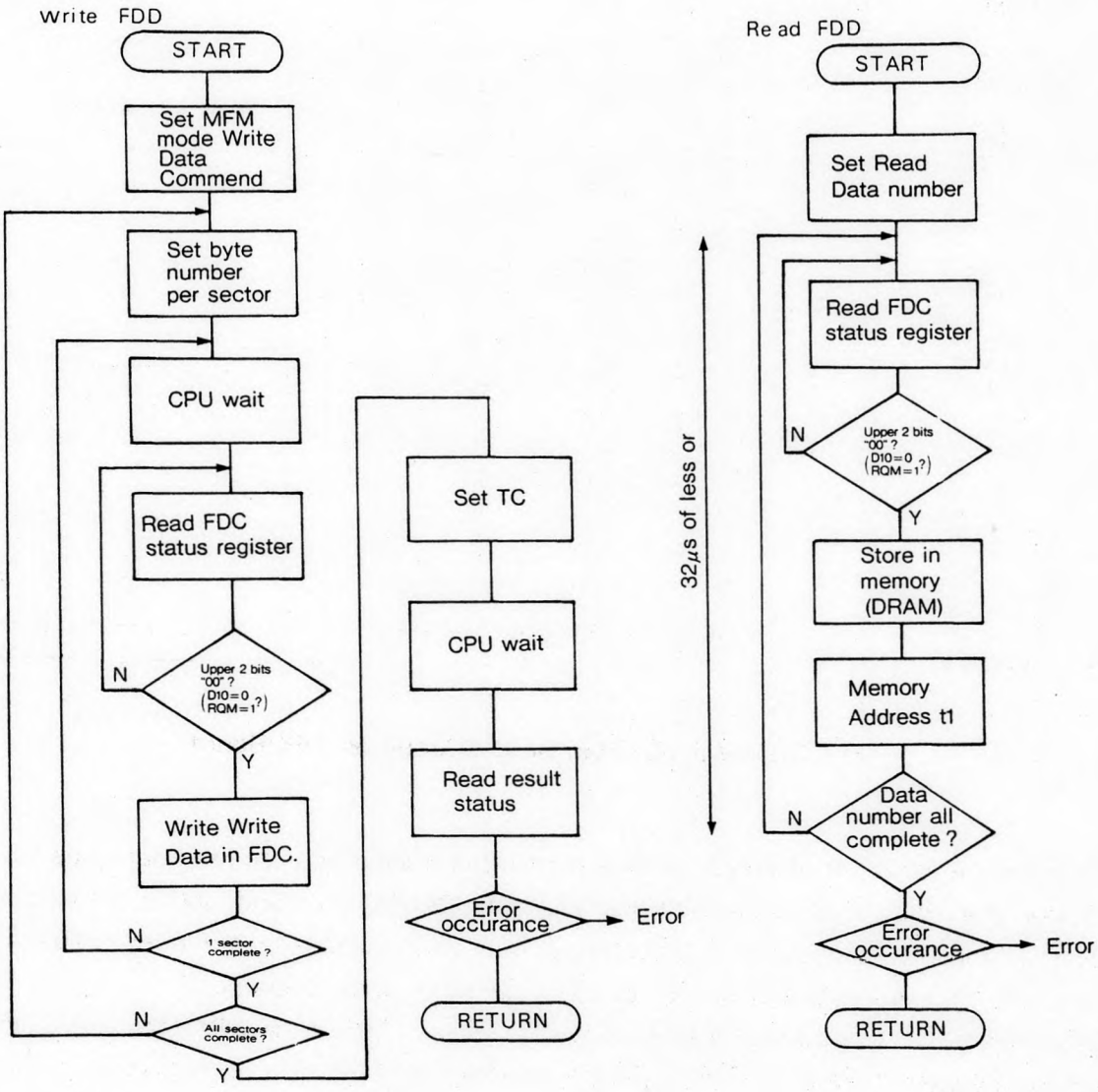


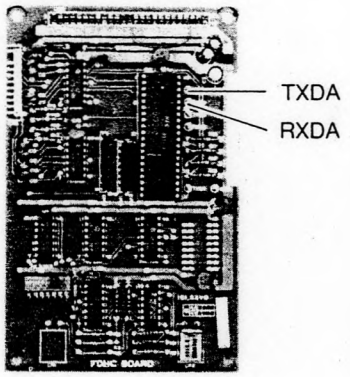
Fig. 2-24 Flow Chart of R/W Operation

The status register and data register of FDC μPD765 are selected by the Ao signal.The μPD765AC receives necessary commands (track,head,sector,etc.)from CPU.It sends interrupt signals to CPU and writes sector by sector in FDD.CPU,upon completion of sending necessary data,gives Write End signal (TC) to the μPD765AC.

The timing signal for Write data to FDD is 500KHz.Read time from the μPD765AC is a maximum of 32μsec.

4.3 Adjustments

4.3.1 Adjustment and test point



FDHC board

Test point

RXDA (serial input) == Baud rate 38.4 KHz

TXDA (serinl output) == Baud rate 38.4KHz

TFX board

Test point

TP1 (RAS signal) == ⇨

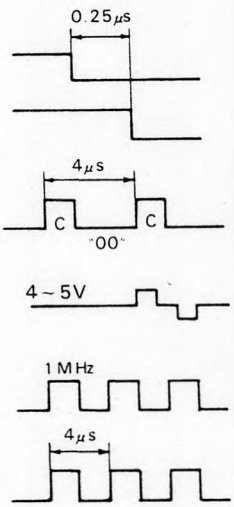
TP2 (CAS signal) == ⇨

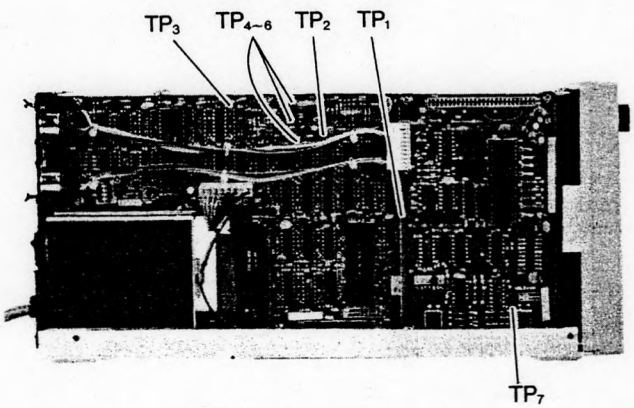
TP3 (Read Data) == ⇨

TP4 (VCO applied voltage) == ⇨

TP5 (VCO output) == ⇨

TP6 (WINDOW) == ⇨

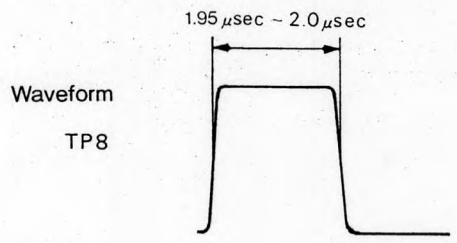




TP7 (Signal GND Level) == ⇨

Adjustment

Adjust TP8-TP7 (GND) to 1,9μsec~2,0μsec (measurement of 50% level of peak value).



Waveform

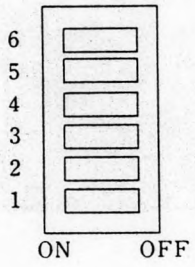
TP8

Oscilloscope
Range 0.5μsec/DIV
2V/DIV

Fig. 3-1

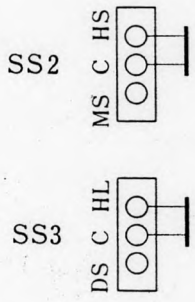
Setting of DIP and DIC switches of drive SD320

Setting of DIP Switch



	Drive A	Drive B
6	OFF	OFF
5	ON	ON
4	OFF	OFF
3	OFF	OFF
2	OFF	ON
1	ON	OFF

Setting of DIC Switch



Resistance modules (150Ω×8)

Drive B—Attach resistance module.

Drive A—Tack out resistance module.

4.3.2 Drive extention of TF-20 (HX-20 type model)

Provide the TF-20 (exclusive use with HX-20)with an extention drive as shown in Fig.3-2.

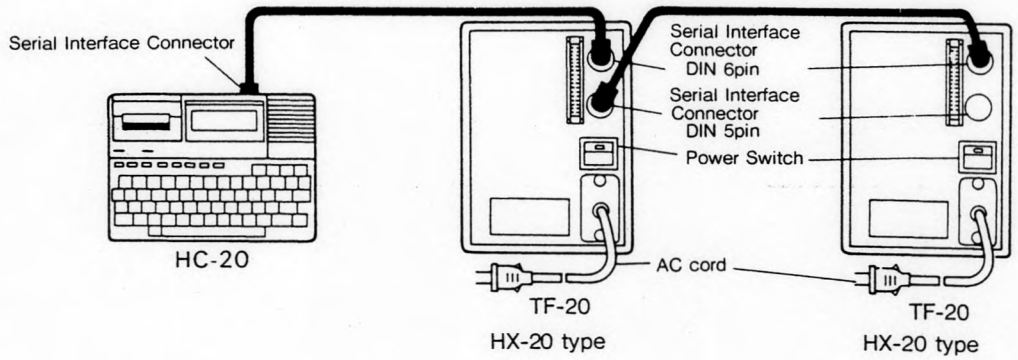


Fig. 3-2 Connection of Extension Drive

Where the TF-20 (exclusive use with HX-20) is used as an extention:

Turn off pin 4 of the DIP switch on the TFX board as shown in Fig.3-3.

Set other DIP and DIC switches the same way as with the TF-20 (exclusive use with HX-20) .

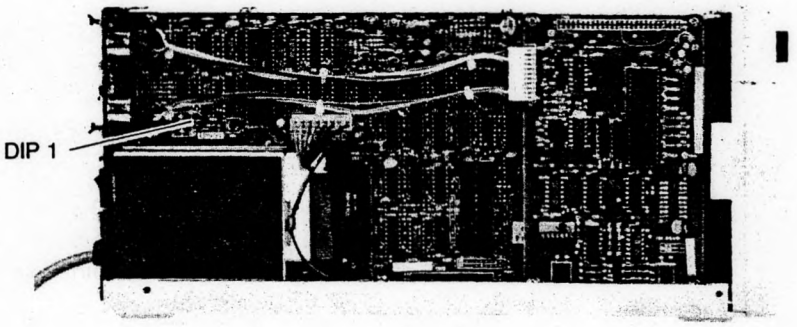
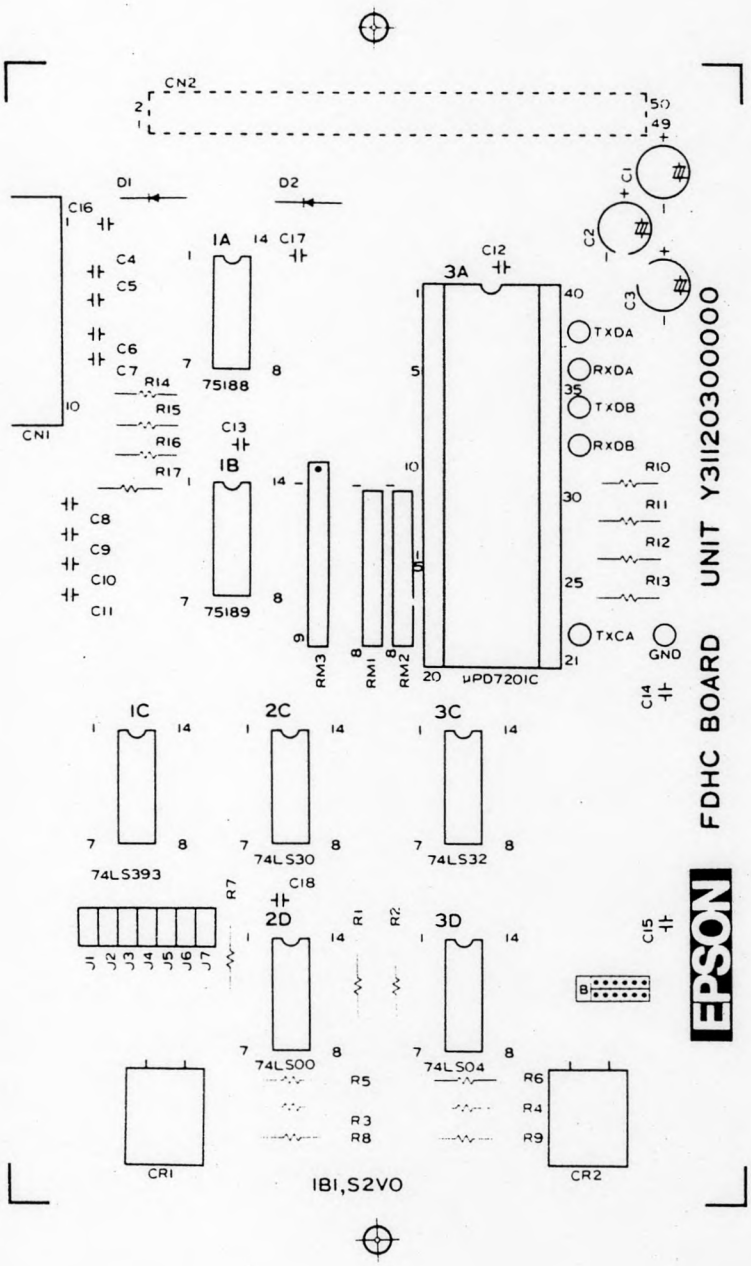
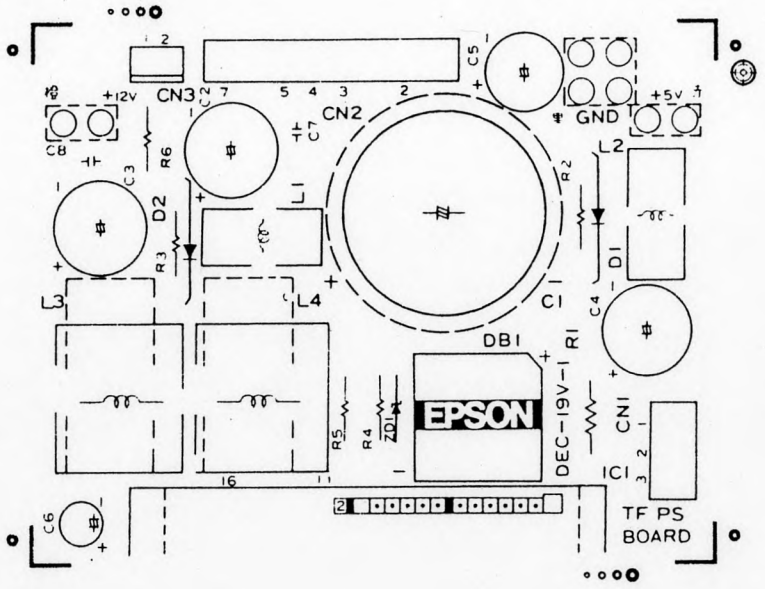
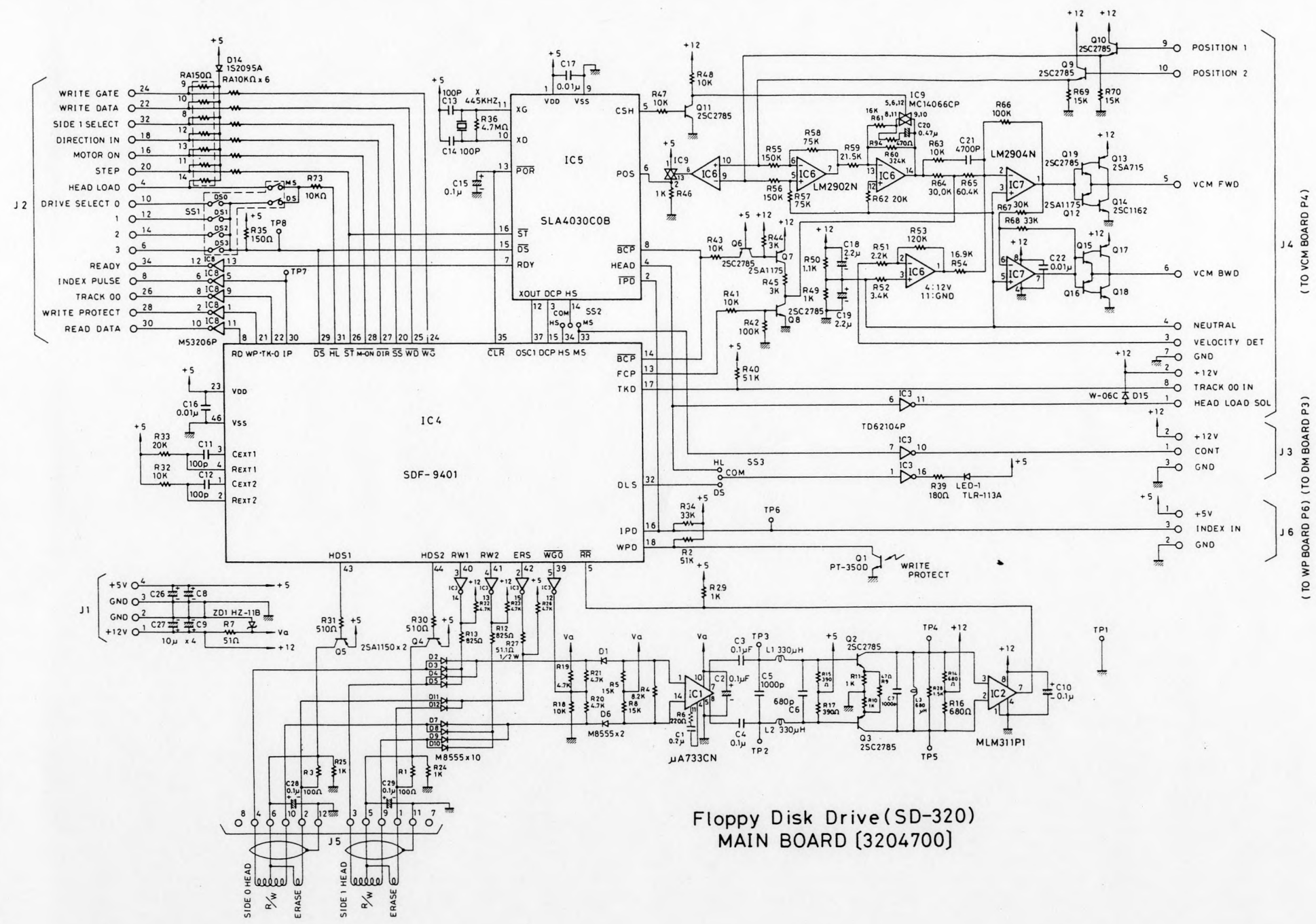


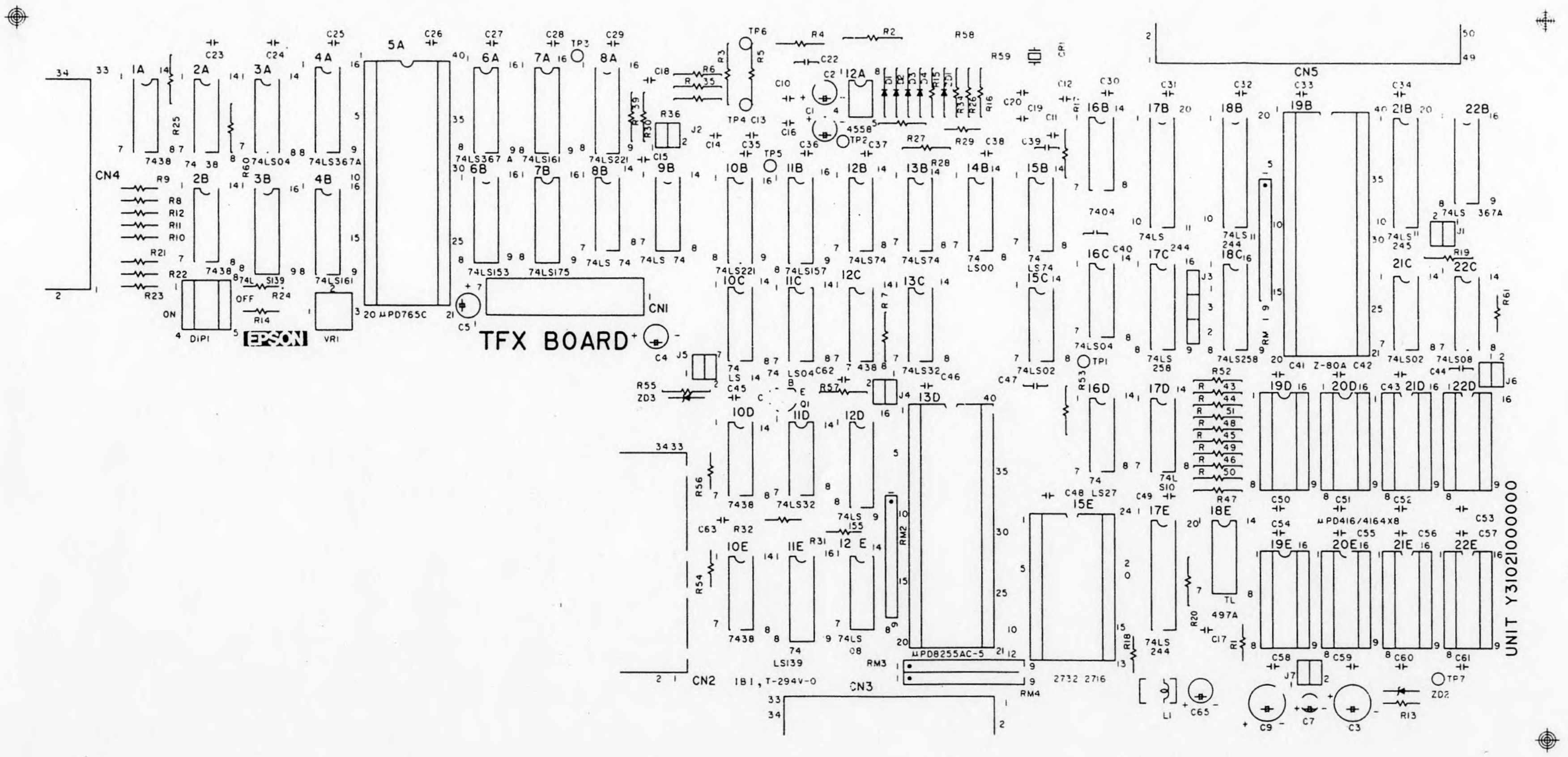
Fig. 3-3


CN2
D1
D2
C1
C2
C3
C16
C4
C5
C6
C7
R14
R15
R16
R17
C13
CN1
1A
C17
75188
1B
75189
C8
C9
C10
C11
C12
3A
μPD7201C
TXDA
RXDA
TXDB
RXDB
TXCA
GND
R10
R11
R12
R13
C14
RM3
RM1
RM2
1C
74LS393
2C
74LS30
3C
74LS32
C18
R7
2D
74LS00
R1
R2
3D
74LS04
C15
J1
J2
J3
J4
J5
J6
J7
B
R5
R3
R8
R6
R4
R9
CR1
CR2
EPSON
FDHC BOARD UNIT Y3112030000
IBI,S2VO

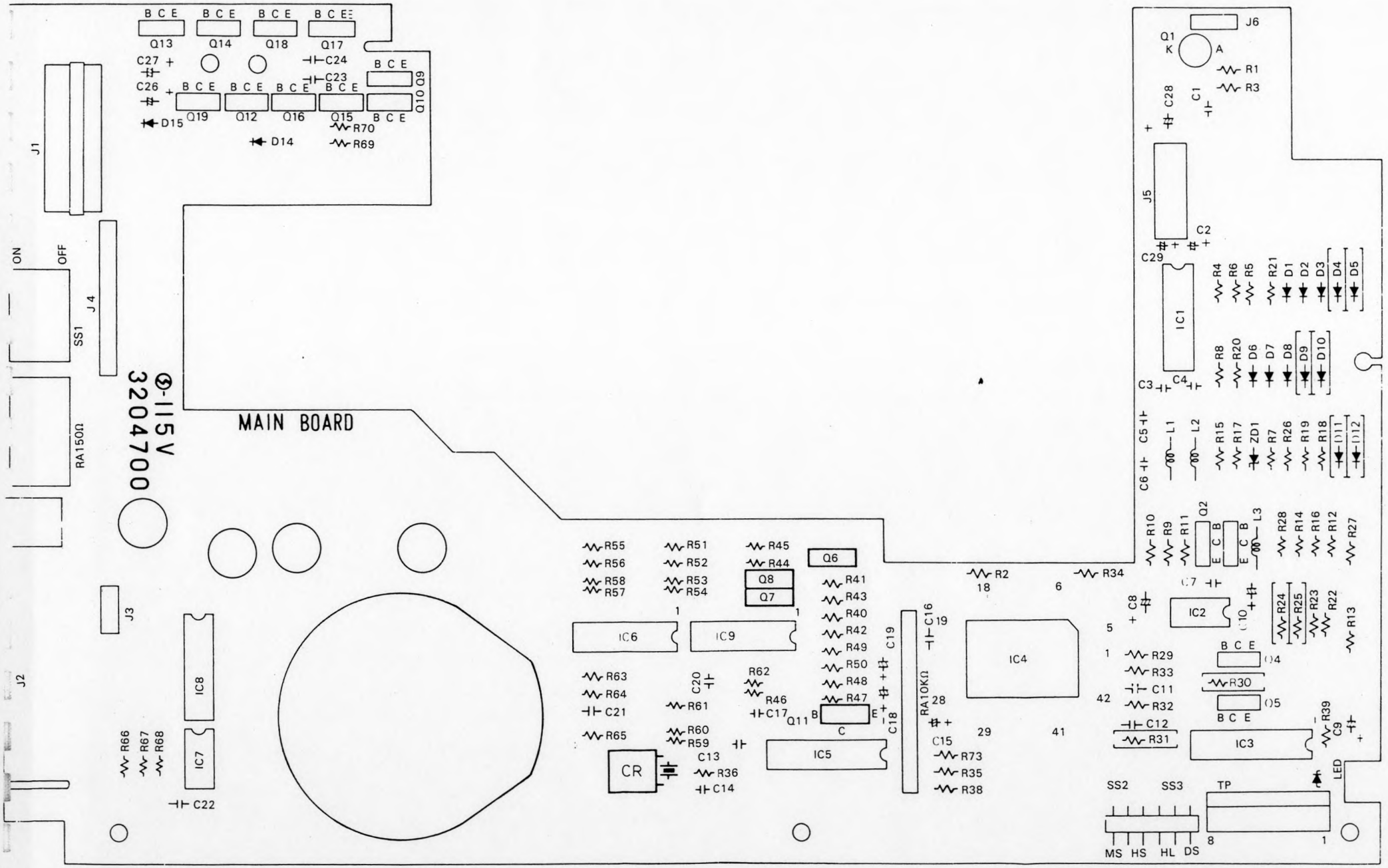

CN3
CN2
+12V
GND
+5V
C8
C3
R6
C2
C7
C5
L1
L2
D2
R3
R2
D1
L3
L4
C1
C4
DB1
R1
EPSON
DEC-19V-1
R5
R4
ZD1
CN1
IC1
C6
TF PS
BOARD



Floppy Disk Drive (SD-320)
MAIN BOARD (3204700)



TFX BOARD
EPSON
UNIT Y3102100000
CN1
CN2
CN3
CN4
CN5
DIP1
VR1
μPD765C
μPD8255AC-5
Z-80A
μPD416/4164X8
2732 2716


MAIN BOARD
Φ-115V
3204700
J1
J2
J3
J4
J5
J6
SS1
ON
OFF
RA150Ω
RA10KΩ
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
CR
LED
TP
SS2
SS3
MS
HS
HL
DS
Q1
Q2
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D14
D15
ZD1
L1
L2
L3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
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R43
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R58
R59
R60
R61
R62
R63
R64
R65
R66
R67
R68
R69
R70
R73
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
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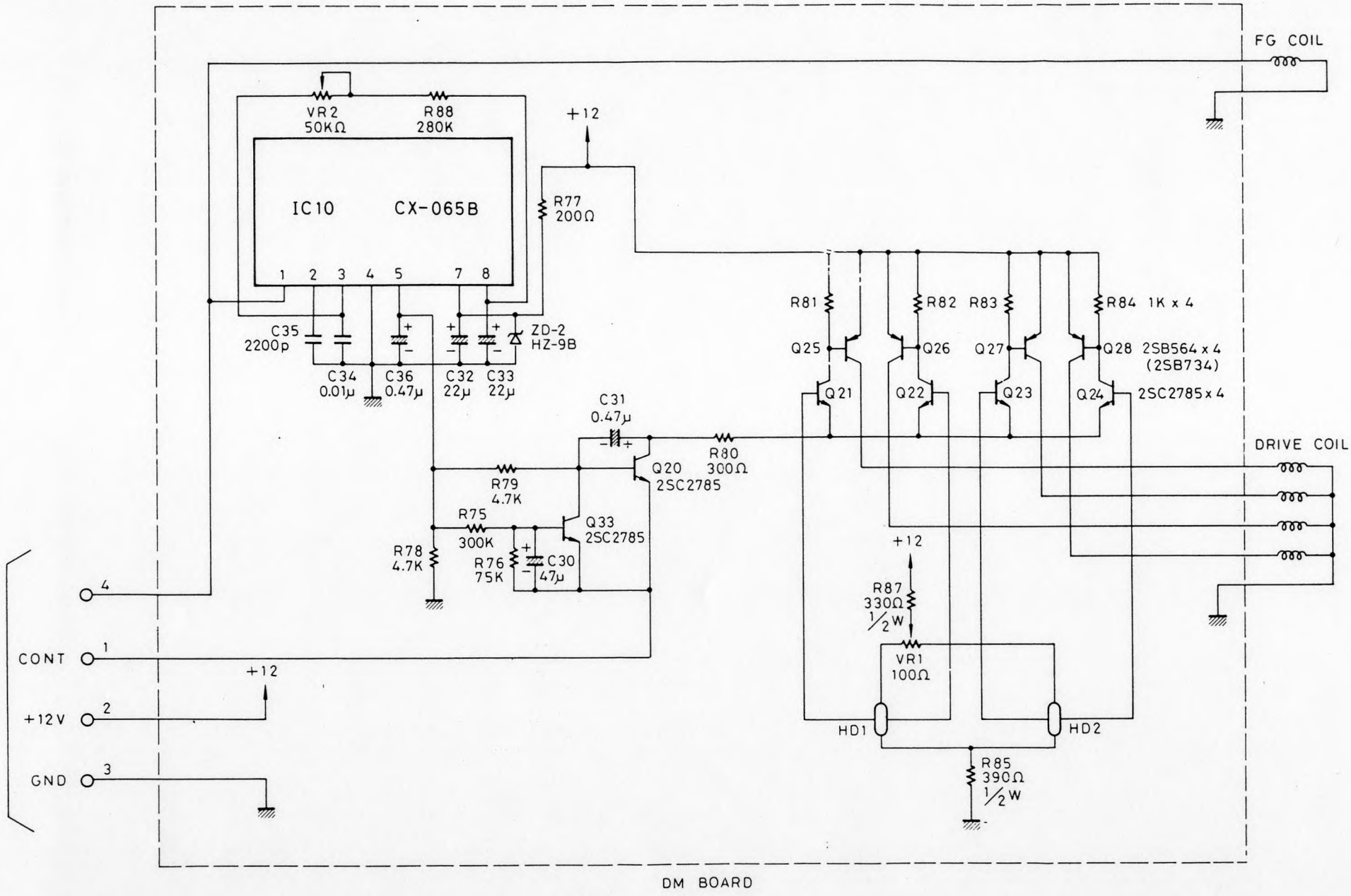
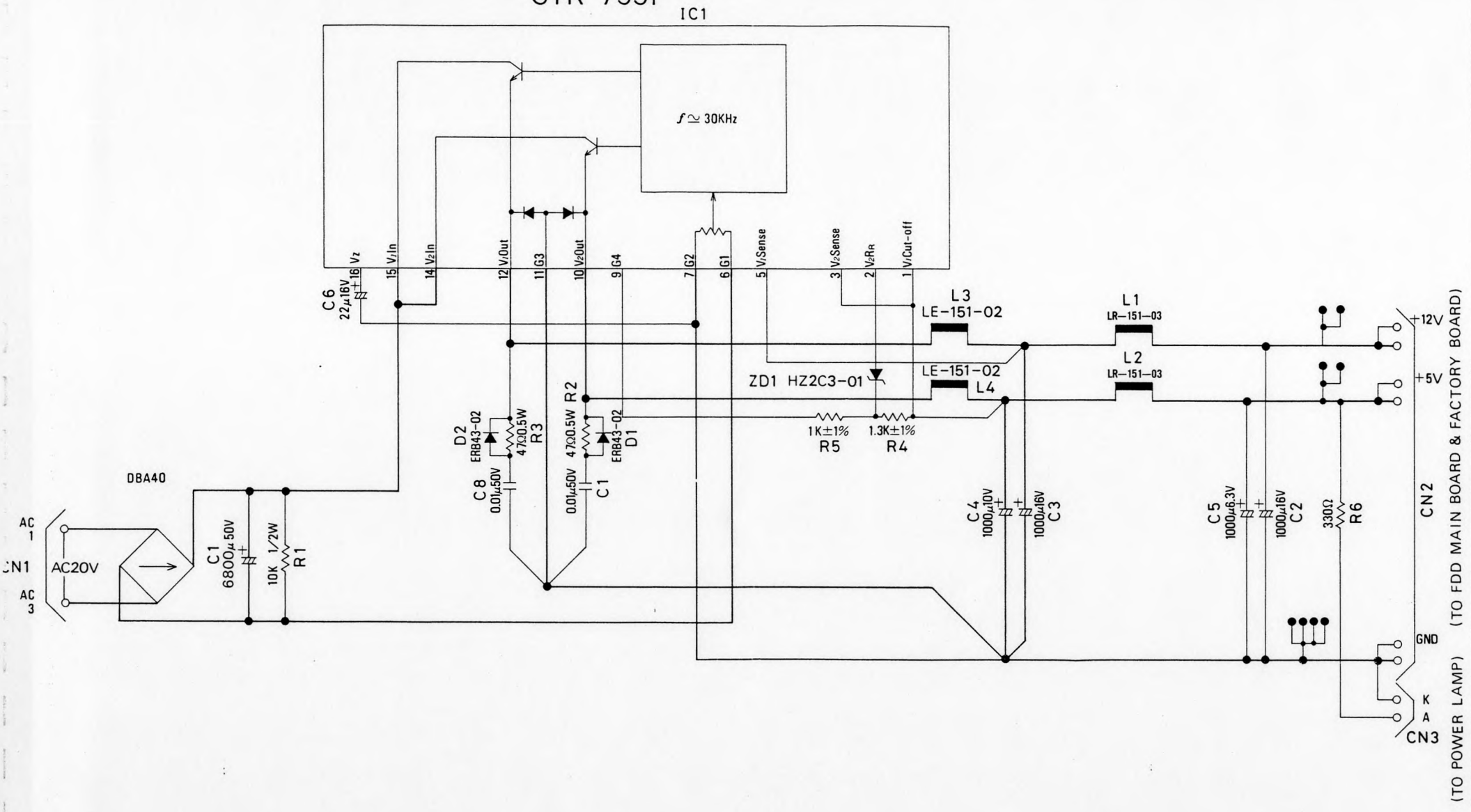
C22
C23
C24
C26
C27
C28
C29



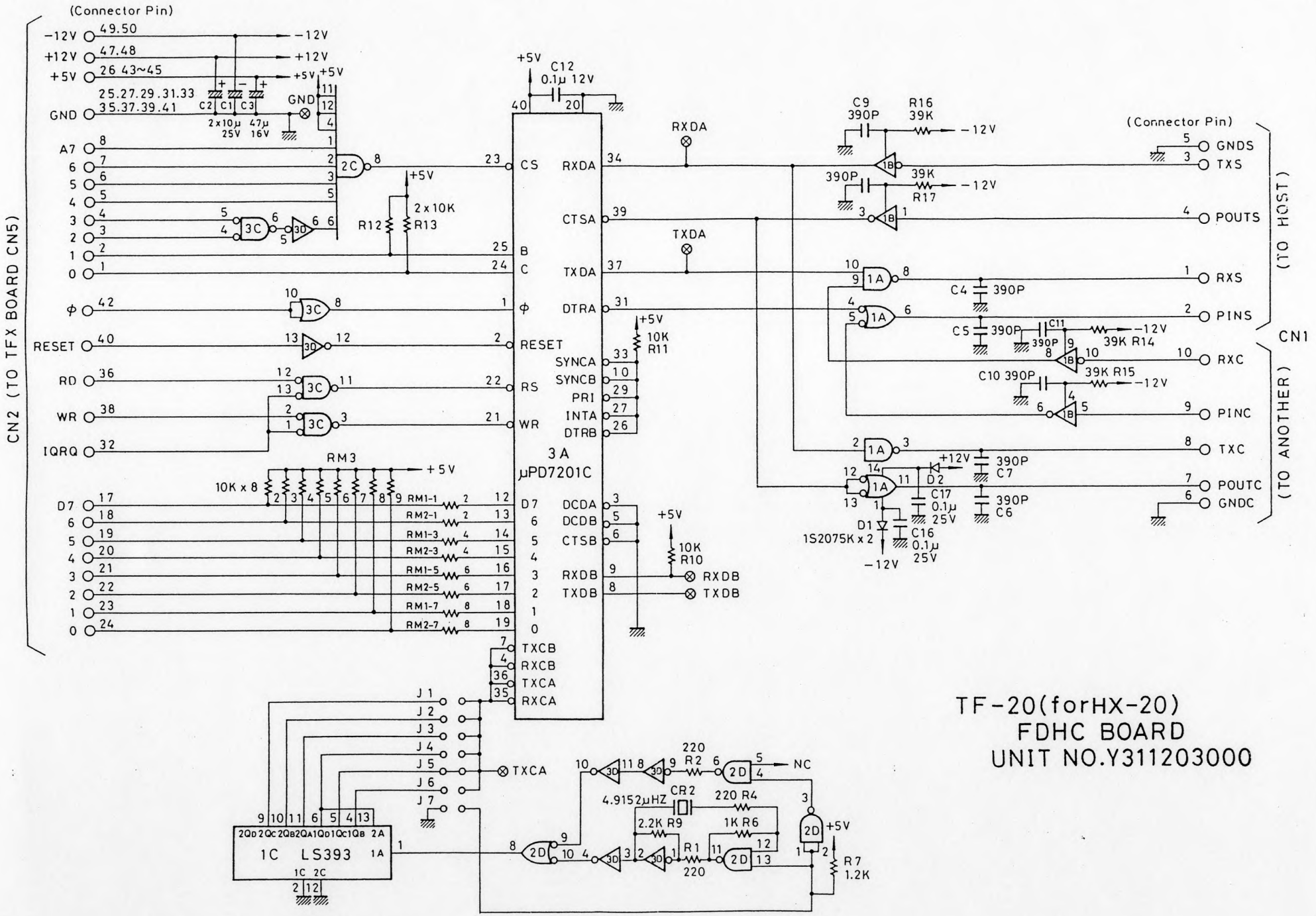
Floppy Disk Drive (SD-320/321)

DM BOARD

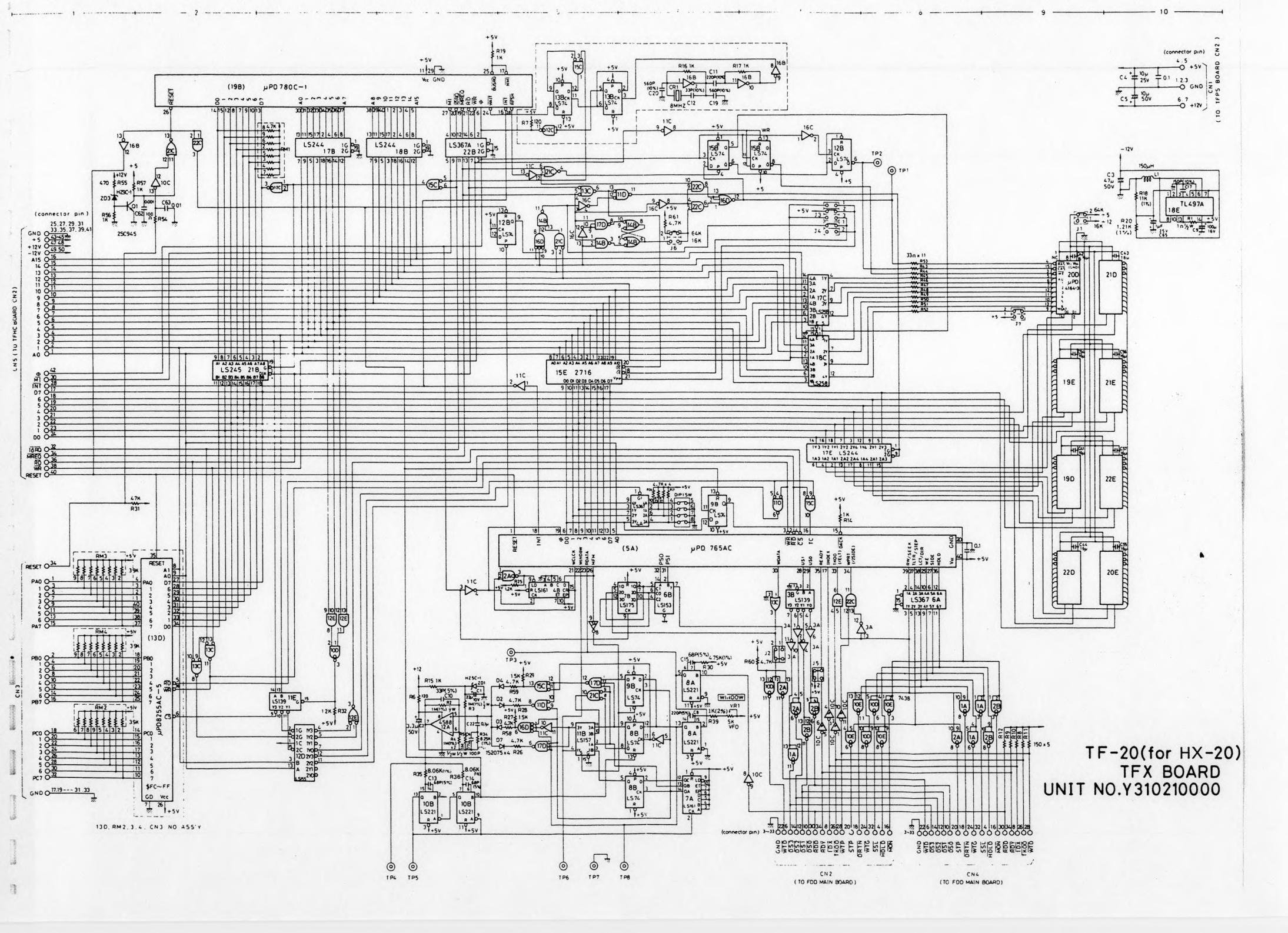
STK 7551



TF–20
TFPS BOARD
UNIT NO. Y310202100



TF-20(forHX-20)
FDHC BOARD
UNIT NO.Y311203000


TF-20(for HX-20)
TFX BOARD
UNIT NO.Y310210000
(19B) μPD780C-1
(5A) μPD 765AC
μPD8255AC-5
CN1 (TO TFPS BOARD CN2)
CN2 (TO FDD MAIN BOARD)
CN4 (TO FDD MAIN BOARD)
CN3 (TO TFHC BOARD CN2)
13D, RM2, 3, 4, CN3 NO ASS'Y
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8