From: ITT 3030 Technical Information.pdf

This manual is marked as „Vorabversion“, i.e. it is a preliminary version.

Page 52:
There are the following inputs for the screen and the keyboard:

I. Operation with a function code (Address FE9AH)
II. Character wise operation with/without control character recognition Address FE09H/FE76H)
III. Request keyboard status (Address FE12H)
IV. Wait for key (Address FE73H)

If any of these addresses seems familiar, I'll translate the corresponding section.

Page 89 has a schematic of the keyboard circuit.

Page 173 the WD1791 floppy controller gets ¼ of a 4MHz oscillator as its frequency

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Page 19:

NMI jumps to 66H on the currently active memory page and executes from there

Page 25: Processor wait cycles

Wait cycles can be programmed by writing to I/O addresses:

F0	for commands	OUT 0F0H
F1	memory access	OUT F01H
F2	I/O addressing	OUT 0F2H

Bit 0 of the data byte transmitted determines the state of the wait logic: D0=1 means on, D0=0 means off.

RAM on the Combo chip

The combo chip MK3886 has 256 bytes of RAM from 1000H … 10FFH on the internal page 8

1000H … 103FH can be write protected. This can be programmed, but at a reset of the MK3886 this portion of RAM is write protected, too.

The status of the write protection can be queried on 0E5H (IN 0E5H). Bit 5 tells the status: if D5=1 64 bytes are write protected, if D5=0, they can be written to.

Writing to 0EAH changes the write protection: OUT EAH has the following effect with those values:

66H	removes write protection
55H	writes one piece of data, then protects
all other	set write protection

Page 121: shift-lock LED on the keyboard and "horn" (beeper)
The status of the shift-lock LED and the beeper is controlled by sending D0=1 (on) or D0=0 (off) to 32H for the beeper and 33H for the LED

Page 122f

35H contains status information from the Keyboard/video interface:

Bit 7	BL	blank signal
Bit 6	VSYN	vertical sync signal
Bits 5-3	STAT5-STAT3	Keyboard status information
Bits 2-0	STAT2-STAT0	Monitor adapter information, signal QT, monitor frequency in use

Page 133f:

Adresses of the 8278 for keyboard control

Read data bus register	10H	IN A,(10H)
Read status	11H	IN A,(11H)
Output command	11H	OUT (11H),A

Command modes for the 8278

Bit 7	Bit 6	Bit 5	Command type
0	0	0	Set command mode
0	1	0	Read FIFO
1	0	1	Cancel

Format of the command byte (OUT 11H)

Bit 3:	Error treatment	0 = Error when multiple keys are pressed 1 = no error (N-key rollover)
Bit 2:	Interrupt request	0 = Request interrupt when there are characters in the FIFO and on Error (via INT0/, port 62) 1 = request no interrupt
Bit 0	key recognition	0 = normal operation, report every key once 1 = report keys on press and release

Read FIFO

Command byte: 40H

Effect: The lowest FIFO register is copied into the data bus register, the FIFO contents are moved down one place. The counter of the data register is decreased. The FIFO's contents can be read in the data bus register

Error: If the FIFO is empty, the last byte that has been read is transmitted, the counter remains at 0, no error is being reported

Clear command

Clear error flag	Command byte 0CEH
Erase FIFO	Command byte 0CFH

Page 158 "Horn" (beeper): The frequency of the beeper is ca. 770kHz

Page 167: Correlation of keys and matrix addresses

Page 195: Floppy controller addresses:

50H - 1791 Status/command register
51H - 1791 track register
52H - 1791 sector register
53H - 1791 data register
54H - card status/card command register

By issueing IN 54H, the status of the minifloppy controller card can be read by the CPU.

Bit 7	Data request (DRQ/)
Bit 6	Interrupt request (INTRQ)
Bit 5	Head load (HLD/)
Bit 4	Ready 3 (drive 3 ready)
Bit 3	Ready 2
Bit 2	Ready 1
Bit 1	Write protect (the disk in the selected drive is write protected)
Bit 0	HLT (halt signal on head down and track change)

Commands transmitted by issueing OUT 54H

Bit 7	SEL1/ - selsct drive 1
Bit 6	SEL2/
Bit 5	SEL3/
Bit 4	MOTOR/ - Motor on
Bit 3	DOOR/ - Lock drive 1 and 2 doors
Bit 2	SIDESEL/ - select disk side
Bit 1	KOMP/ - write precomp on/off
Bit 0	RG J – switch the data separator to read