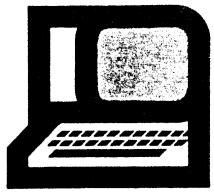

ITT
Microcomputer
Hardware

User Manual

ITT 3030

Parallel I/O

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PARALLEL INPUT/OUTPUT INTERFACE

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1. INTRODUCTION

The Parallel Input/Output Interface is a programmable digital device designed to enable the ITT 3030 microcomputer to operate with external equipment. It can be used, for example to set switches, to determine switch positions, to operate peripheral equipment or to monitor and control processes.

Parallel Input/Output means that as signals PA0 - PA7 (Port A) and PB0 - PB7 (Port B) are presented simultaneously to the input/output connections. Each channel can operate in either input or output mode. The signals presented to each channel can have one of two possible values (digital TTL values):

Logic 1 = High (5V)
Logic 0 = Low (0V)

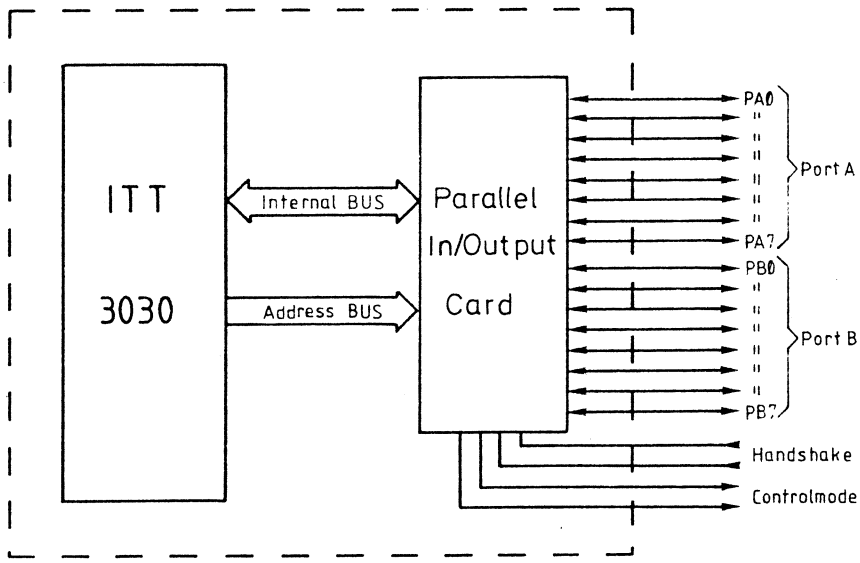


Fig.1: ITT 3030 with the Parallel Input/Output Interface

As the PIO is a programmable device using the ITT 3030, it is possible to change the signal direction i.e. input or output and the value of the output signals. It is also possible for the CPU to read the state of the channels. The major design characteristics of the PIO can be summarised as follows:

1. Two independent peripheral interface ports with "handshake" data transfer control.

2. Interrupt driven "handshake" for fast response.

3. Four distinct modes of operation.

4. Daisy chain priority interrupt logic included for automatic interrupt vectoring without external logic.

5. All inputs and outputs are fully TTL compatible.

These features are described below.

2. GENERAL DESCRIPTION

The Parallel Input/Output Interface consists of 16 "channels" that can be either transmitted or received by the ITT 3030. The 16 channels (bits) are combined into two 8-bit groups called Port A and Port B. Each port can be individually interrogated and programmed. As a result, four distinct modes of operation are available:

Mode 0 - Transmission of data
Mode 1 - Reception of data
Mode 2 - Bidirectional data bus operation
(Port A only, Port B cannot be used)
Mode 3 - Single bit input/output

These modes can be programmed using special control words or instructions either in BASIC or ASSEMBLER. Operation is also possible under full interrupt control (see section 3.3).

BASIC Instructions : INP, OUT, WAIT
ASSEMBLER Instructions : IN , OUT

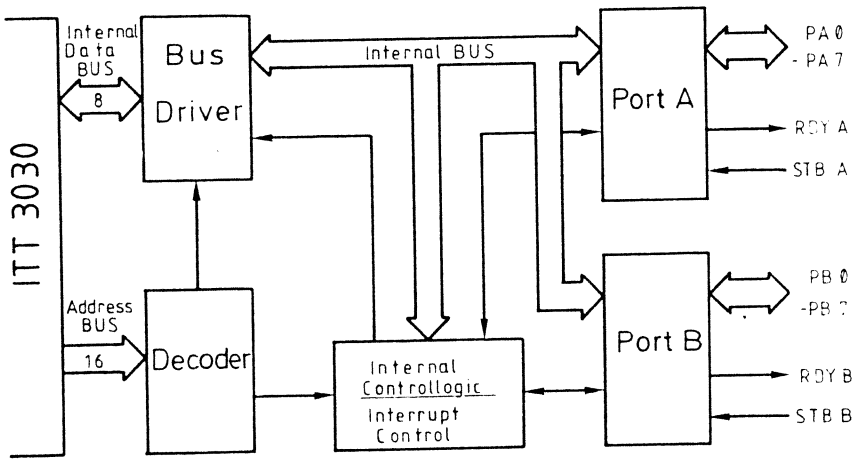


Fig.2: Block Diagram of the Parallel Input/Output Interface

All input/output gates are fully TTL-compatible and the 8 outputs forming Port B can also be used to drive Darlington transistors.

3. INSTALLATION INSTRUCTIONS

Instructions for the assembly and dismantling of the ITT 3030 are contained in the User's handbook, but the following instructions for the insertion of PCB's are given for the sake of completeness:

1. Switch the equipment OFF and remove the power cables from the mains sockets.

2. Remove the top cover (see the ITT 3030 User's handbook).

3. As required, remove the Floppy Disc Drives (this assumes that this operation is not the first installation of the system).

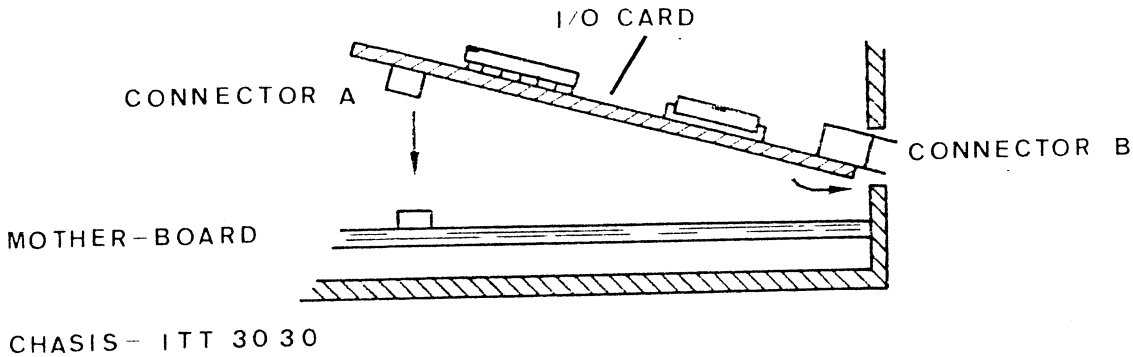
4. Release the Floppy Disc Drives retaining plate and remove. To achieve this, remove the black AMP connector from the right hand side of the retaining plate. Release the locking device on the underside of the left hand side of the retaining plate by turning it to the left. The retaining plate is now free and can be removed.

5. Select the required connector position on the rear of the unit and remove the protective cover from the slot. If the computer is to be used for interrupt operation, the selection of the appropriate connector must follow the interrupt priority that is fixed by the hardware. The priority is fixed via a daisy chain and in this instance is as follows:

   Viewed from the front:
   1. Left hand connector (highest priority)
   2. Middle connector
   3. Right hand connector (lowest priority)

   The daisy chain must not be interrupted and it may be necessary to re-arrange already installed PCBs in order to achieve the required priority sequence. The addresses for these PCBs will not be changed by this process.

6. The required PCB can now be installed into the slot and the connector for the internal data bus pressed into place on the adjacent circuit board.



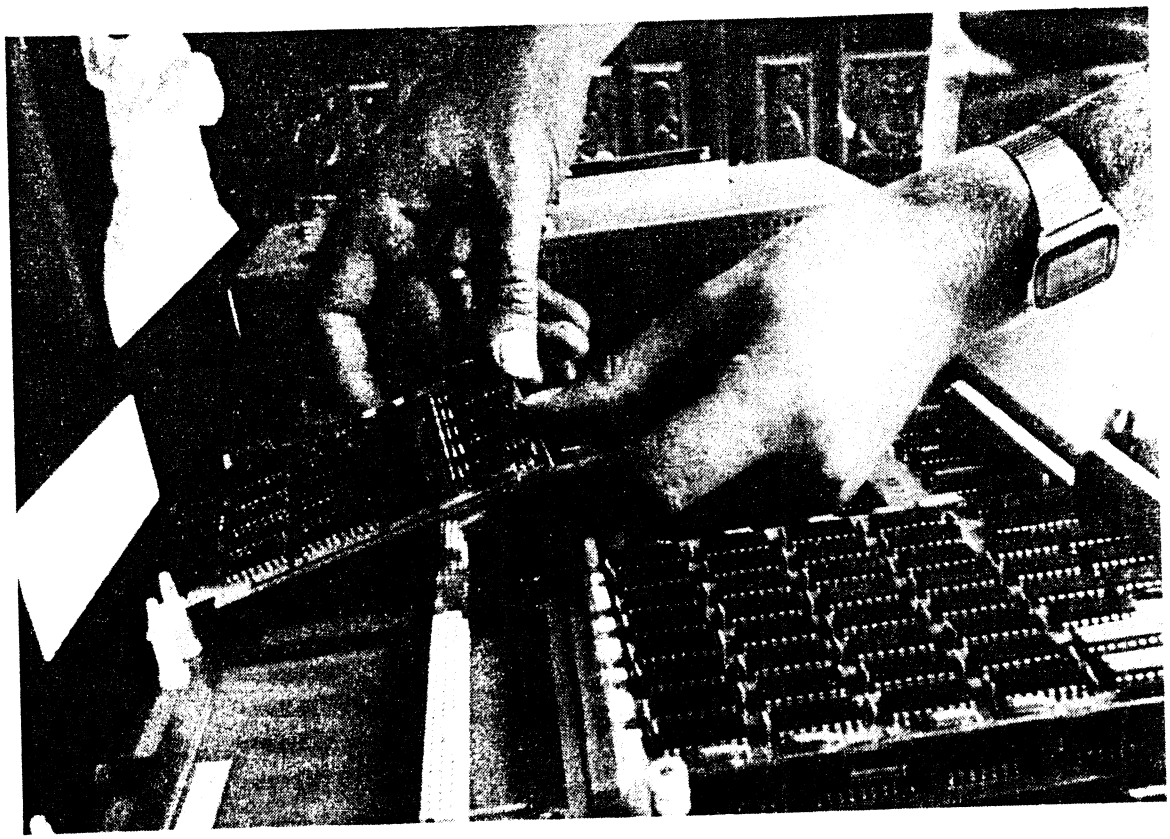
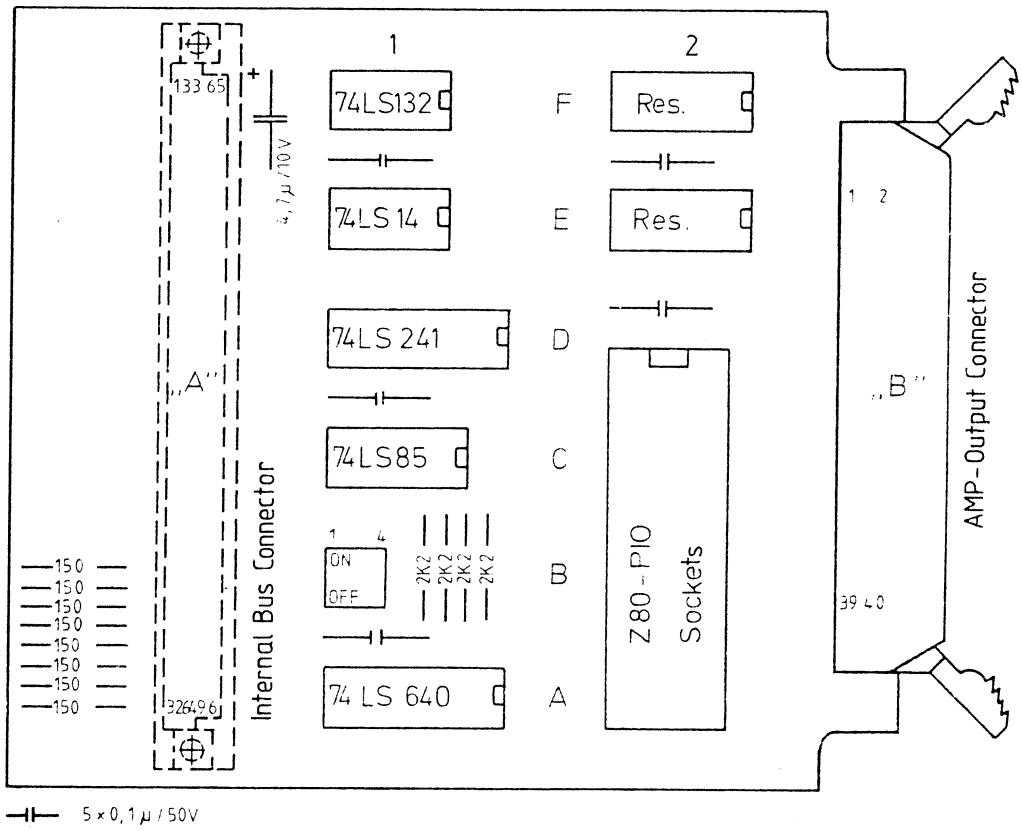
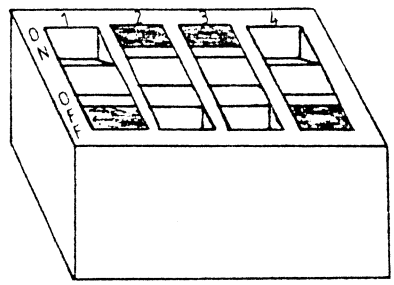


Fig.3: Installation of the PIO PCB

7. *Addressing*

Every PCB must, at installation, be given an individual address that can be used by the program to uniquely identify the card. No two interfaces (including other types such as RS 232 and IEEE Bus Interfaces) may have identical addresses.





Address Switches
(4Bit-Baseaddress)

Fig.4: PIO Layout with Addressing Microswitch

The address is selected using the microswitch on the PCB in accordance with the following table:

Address		Switch			
Dec	Hex	S4	S3	S2	S1
0	00	0	0	0	0
16	10	0	0	0	1
32	20	0	0	1	0
48	30	0	0	1	1
64	40	0	1	0	0
80	50	0	1	0	1
96	60	0	1	1	0
112	70	0	1	1	1
128	80	1	0	0	0
144	90	1	0	0	1
160	A0	1	0	1	0
176	B0	1	0	1	1
192	C0	1	1	0	0
208	D0	1	1	0	1
224	E0	1	1	1	0
240	F0	1	1	1	1

0 = Switch position OFF
1 = Switch position ON

A few addresses have already been allocated and must not be used. These are:

00, 10, 20, 30, 50, 60, E0 and F0 (hexadecimal)

The PIO Interface will be delivered with address 90H preset by the manufacturer.

8. Reassembly

Reassembly is in the reverse order in accordance with the User handbook. (For initial installation of the system, follow the assembly instructions in the User documentation.)

4. SOFTWARE CONTROL AND PROGRAMMING

4.1 SELECTING AN OPERATING MODE

It is necessary to define the operating mode for the Parallel Input/Output Interface using control words before undertaking any data transfers. The PIO will decode the lower 8 bits of the address word to determine whether the following information is to be interpreted as an instruction or as data. They also define which port is to be used.

These 8 bits have the following format:

Address Bits								Decode Information
A7	A6	A5	A4	A3	A2	A1	A0	
				X	0	0	0	Instructions Port B
				X	0	0	1	Data Port B
				X	0	1	0	Instructions Port A
				X	0	1	1	Data Port A
				X	1	0	0	Reset after Interrupt
PCB Address (set by microswitch)								

X= not used

The PIO PCB must be identified (addressed) within the micro-computer system itself. The address is set when the PIO PCB is first installed into the system using the in-built microswitches. It is usually specified in hexadecimal based on the calculated values of bits A4-A7 and assuming that bits A0-A3=0. When, for example bits A4 and A7 are set using microswitch positions S1 and S4, this PCB address is 90H, where the H stands for hexadecimal.

The Control Word for mode selection has the following format:

Data Bits								Mode
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	X	X	1	1	1	1	0=Byte Output
0	1	X	X	1	1	1	1	1=Byte Input
1	0	X	X	1	1	1	1	2=Bidirectional Bus
1	1	X	X	1	1	1	1	3=Bit Input/Output

X = not used
Byte= 8 bits

Bits D3-D0 must all be set to "1" to indicate that a new mode is to be set.

4.2 DESCRIPTION OF THE OPERATING MODES

MODE 0 - BYTE OUTPUT

When Mode 0 is selected, the 8 data bits will be sent via the internal data bus connecting the PIO with the CPU to the output data bus for the required Port. The contents of the output register can be changed at any time simply by sending a new data word from the CPU to the PIO. Also, the contents of the output register can be read back to the CPU using an input instruction.

When data for the CPU has been written to the selected port, the READY line (1=high) for the required port will be activated,(notifying the peripheral that data is available. This signal will remain active until a "received" signal is sent from the receiving peripheral. This "received" signal is in the form of a STROBE pulse whose rising edge generates an interrupt (if enabled by the appropriate control word, see also section 4.3) and resets the READY line to low. This very simple handshake system is common to many peripheral devices.

MODE 1 - BYTE INPUT

When Mode 1 is selected, the required port will be set to input data from the peripheral. To start the handshake routine, the CPU performs an input read operation from the port. This activates the READY line to the peripheral to indicate that data should be loaded into the empty input register. The peripheral then loads the data into the input register using the STROBE signal. Again, the rising edge of the strobe causes an interrupt request (if enabled) and resets the READY line.

MODE 2 - BIDIRECTIONAL DATA TRANSFER

This operating mode allows a two directional exchange of information between the ITT 3030 and peripheral devices such as printers or other computers that must operate using a parallel interface. As this mode requires the use of all four handshake lines, only Port A can be used. Port B must be set to Mode 3 and its signals (PB0-PB7) suppressed using an appropriate mask (see section 4.3). The handshake signals for Port A are used for output control and those for Port B are used for input control. The only difference between Mode 2 output operation and Mode 0 is that data from the Port A output register is allowed onto the port data bus only when STROBE A is active.

MODE 3 - BIT OPERATION

Mode 3 operation is intended for status and control applications and does not utilise the handshake signals (see the example in section 4.4). When Mode 3 is selected, the next word sent to the PIO must be a control word and must define which of the port data bus lines are to be inputs and which are to be outputs.

The control word has the following format:

D7	D6	D5	D4	D3	D2	D1	D0
I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

If any bit is set to "1" then the corresponding data bus line will be used as an input. Conversely, if the bit is reset ie "0", the line will be used as an output. During Mode 3 operation the strobe signal is ignored and the READY line remains inactive. Data may be written to a port or read from a port by the CPU at any time during Mode 3 operation. When reading a port, the data returned to the CPU will be composed of input data from the port data bus lines assigned as inputs plus port output register data from those lines assigned as outputs.
Additionally, this mode offers the possibility to generate interrupts on reaching specified conditions at the input lines. This option frees the processor from status checking (polling) and is explained further in the following chapter.

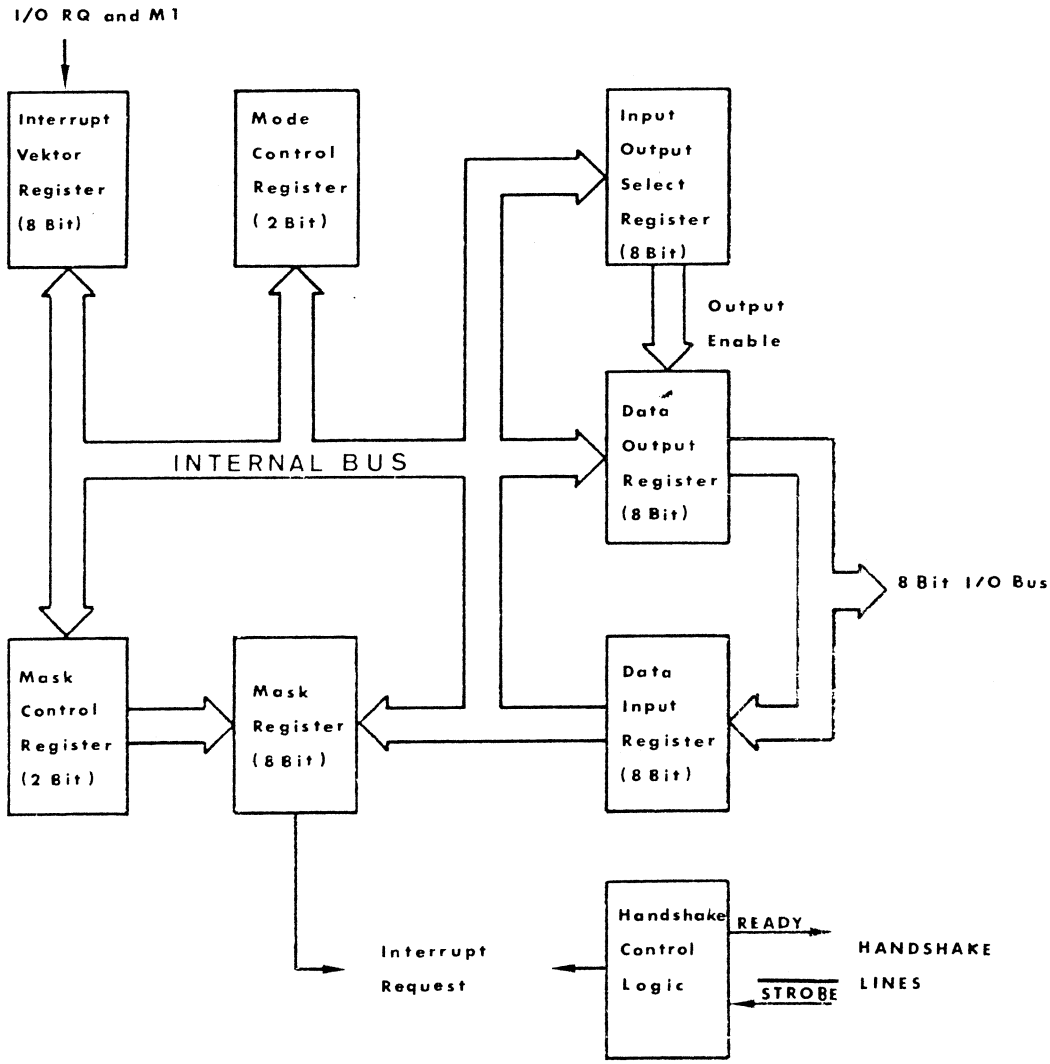


Fig.5: Detailled Block Diagram of an Input/Output Port

3.3 INTERRUPT CONTROL

As stated in the previous section, the Parallel Input/Output interface can operate under full interrupt control. A description of this follows the description of the mode of operation of the Z80 CPU interrupt.

The PIO has been developed to operate with the Z80 CPU in Interrupt Mode 2. This operating mode requires the CPU to receive an interrupt address (vector) from the peripheral requesting the interrupt. This interrupt will cause the CPU to suspend the sequencing of the program in progress and, in this case, force the CPU to service the PIO port requesting the interrupt (e.g. a real time input of new data)

The interrupt vector will be placed on the internal data bus by the interrupting port with the highest priority (Port A before Port B) and will point to a table in the memory. This table forms a series of pointers to the locations where the service routines for the appropriate interrupts are to be found.
The interrupt vector is loaded into the PIO by writing a control word to the desired port of the PIO using the following format:

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	0

The data bit D0 is used as a flag bit and signifies that this control word is an interrupt vector and must be loaded into the vector register. At interrupt acknowledge time, the vector of the interrupting port will appear on the Z80 data bus exactly as shown in the format above.

It is necessary to have an interrupt control word for each port in addition to the interrupt vector. This control word will allow the interrupt to be processed or supressed as required, and in Mode 3 operation informs the PIO that the next control word to be received is a mask.

The interrupt control word has the following format:

D7	D6	D5	D4	D3	D2	D1	D0
IE	AO	HL	MA	0	1	1	1

signifies interrupt control word

IE = Interrupt Enable (permits interrupts)
AO = AND/OR (AND=1, OR=0)
HL = HIGH/LOW (HIGH=1, LOW=0)
MA = Mask (Mask follows = 1)

Bits D4, D5 and D6 are only used in Mode 3 operation and will be ignored in all other modes. These three bits are used to allow for interrupt operation in Mode 3 when any group of the input/output lines adopts certain defined states.
However, setting bit D4 of the interrupt control word during any mode of operation will cause any pending interrupt to be reset.

Bit D6 (AND/OR) defines the logical operation to be performed in port monitoring. If bit D6=1, an AND function is selected and all specified bits must adopt a defined state before an interrupt is generated, while the OR function will generate an interrupt if any specified bit goes to the active state.

D5 defines the active polarity of the port data bus. If bit D5=1, the port data lines are monitored for a high state while, if D5=0 they will be monitored for a low state.

When bit D4=1 in Mode 3 the next control word sent to the PIO must define a mask as follows:

D7	D6	D5	D4	D3	D2	D1	D0
MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

Only those port lines whose mask bit is zero will be monitored for generating an interrupt.

This particular interrupt operation (i.e. one that reacts automatically to set external conditions) results in a considerable saving in computer time that would otherwise be used in determining the status of the peripheral devices.

An example using interrupt routines is given in section 4.4.

Interrupt Priority (Daisy Chain)

The interrupt control logic section handles all CPU interrupt protocols for nested priority structures. The priority of any device is determined by its physical location in a "daisy chain" configuration. Two lines are provided in each PIO to form this daisy chain. The device closest to the CPU has the highest priority. In this case, the system has been hardware configured so that the left connector (viewed from the front) has the highest priority after the combo chip on the CPU PCB. Within the PIO itself, Port A interrupts have a higher priority than those of Port B. The PIO provides for complete control of nested interrupts. That is, lower priority devices may not interrupt higher priority devices that have not had their interrupt service routine completed by the CPU. Higher priority devices may interrupt the servicing of lower priority devices.

Interrupt Service Routines

When writing the interrupt service routine, it is imperative to take note of a peculiarity in its operation. Normally, the interrupting device will be reset using the instruction RETI (Return from Interrupt). The PIO interface requires an additional instruction in order to reset the interrupting port. Therefore, the final two instructions of the interrupt servicing routine must be in the form:

```
OUT   PCB address + 4  (i.e. Address bit A2=1)
RETI
```

Note:

This instruction resets both PIO ports (hardware reset). Therefore both ports must be re-initialized following each interrupt.

4.4 PROGRAMMING EXAMPLE

Central Heating Control.

A typical example for the use of single-bit Mode 3 operation is the control of a central heating system. In this example the individual bits for the control and status words have the following definition:

Bit	Signal	Input/Output
D0	Equipment "ON"switch	PA0
D1	Heating "ON"	PA1
D2	not used	PA2
D3	Temperature Alarm	PA3
D4	Excess Pressure Alarm	PA4
D5	Emergency "OFF" switch	PA5
D6	Alarm signal "ON"	PA6
D7	not used	PA7

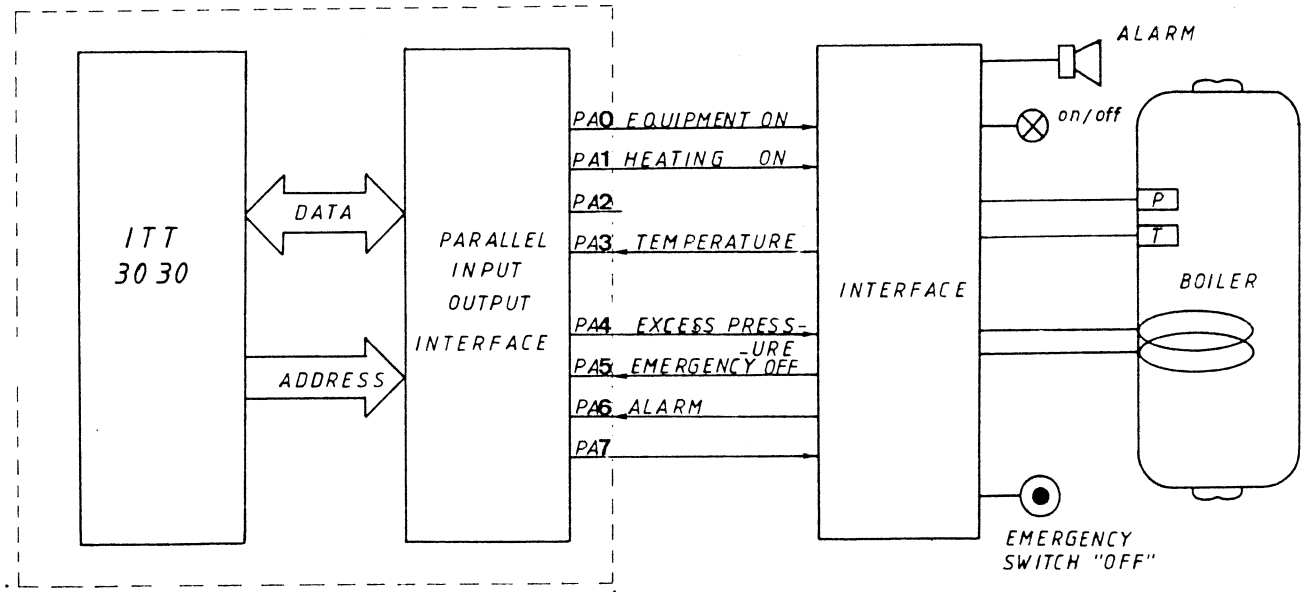


Fig.6: Practical Example of the Use of the PIO

The PIO must now be programmed. The PCB itself has been given address 90H using the microswitch and Port A has been selected as the interface port . Initially, the Port must be configured to operate in Mode 3 using the following control word:

Address 92H	Data 0CFH
10010010 PCB Address 90H	11001111 Mode 3 Bit operation
Instructions Port A	Input/Output

This will be coded in Assembler as follows:

```
LD   A,0CFH          ;Load data into accumulator
OUT  92H,A           ;Output accumulator to Port A
                      via PCB Address 90H
```

After selection of Mode 3, it is necessary that the next word defines the inputs and outputs.

Address 92H	Data 38H 00111000 (D5,D4,D3 = inputs)

Next, the required interrupt vector must be loaded

Address 92H	Data (defined by program) xxxxxxx0

The interrupt control word will then be sent to the Port. In this example, D7 = Interrupt Enable, D6 = OR (logical), D5 = Active (high), D4 = Mask follows.

Address 92H	Data 0B7H 10110111

The mask word that follows this instruction will define that an interrupt should be generated on a change of state of bits D5,D4,D3.

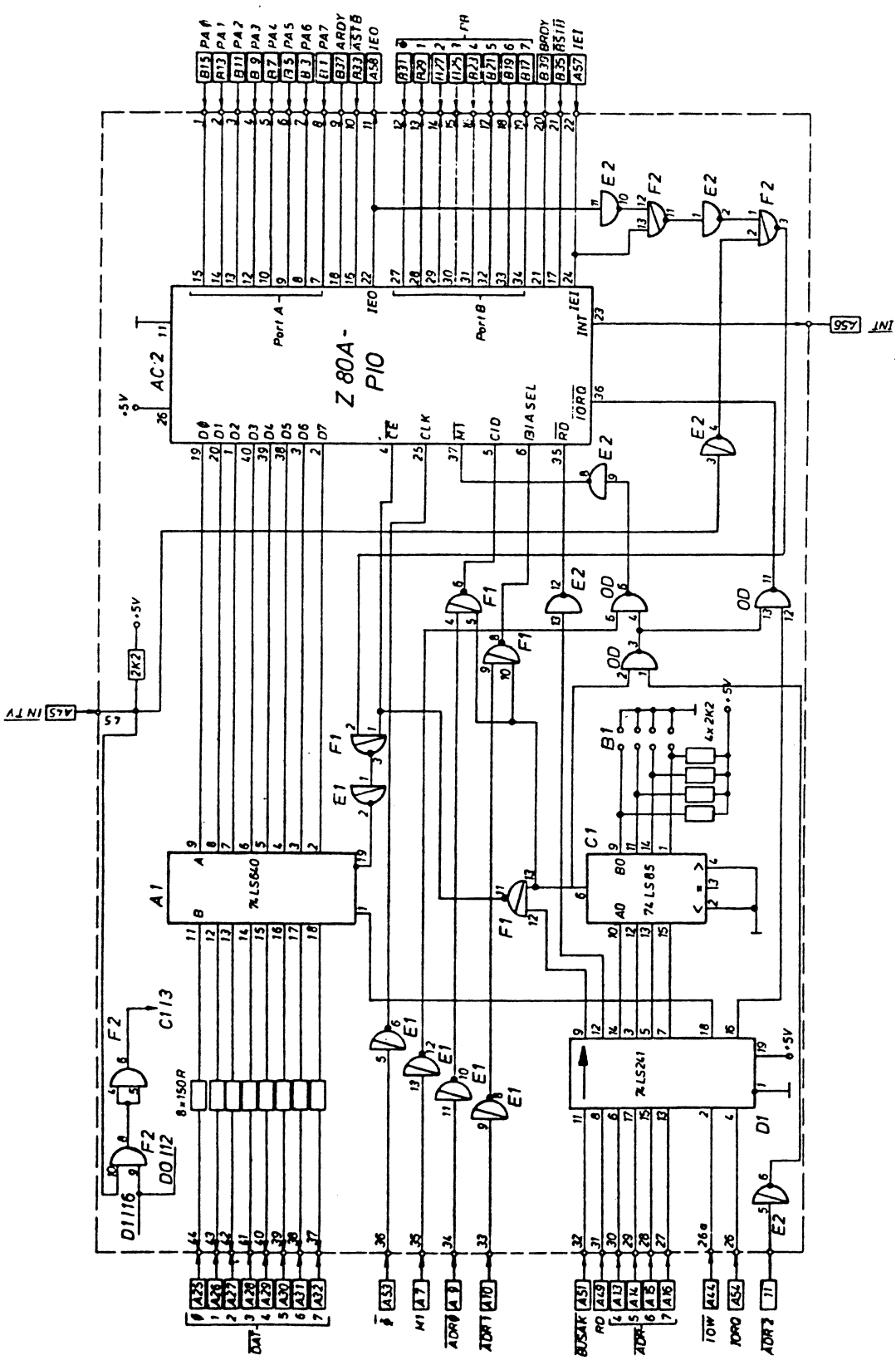
Address 92H	Data 0C7H 11000111

Now, whenever via the sensors or the emergency switch a high signal is received as an input to the PIO over those connections joined to PIO inputs D5, D4 or D3, the Port will immediately generate an interrupt forcing the CPU to go to and perform the appropriate service routine indicated by the previously loaded interrupt vector. In this case, the course of action will be to eventually shut down the heating system and trigger an audible alarm.

Address 93H	Data 40H
10100011 PCB Address 90 Data Port A	01000000 set bit 6 = ² Alarm Signal ON reset bit 1 = ² Heating OFF

To reset the Interrupt line, the interrupt procedure must be closed as described in Chapter 3.3

5. CIRCUIT DIAGRAM



6. TECHNICAL DATA

Internal voltage requirements for the computer :

Vcc = 5V+-5%, Icc = 150mA

Absolute Maximum Ratings :

Storage Temperature	-25 C to +65 C rel. humidity of the air 10-80%
Working Temperature	+10 C to +35 C rel. humidity of the air 20-80%
Voltage on any pin with respect to ground	-0.3V to +7 V
Power dissipation	0.6W

Input/Output Channel Characteristics :

16 parallel input/output channels configured as two 8-bit ports Ports A and B.

All channels fully TTL-compatible

The outputs from Port B (PB0-PB7) can drive Darlington transistors.

Priority : defined by card position (leftmost position - highest priority)
Port A has priority over Port B.

D.C. Characteristics

Specification		Parameter	Min	Typ	Dim
Input Voltage Low (0)	V		-0.3	0.8	V
Input Voltage High(1)	V		2	Vcc	V
Output Voltage Low (0)	V	I = 2mA		0.4	V
Output Voltage High(1)	V	I =-250uA	2.4		V
Input Leakage Current	I	V =0-5V		10	uA
Tristate Output Leakage Current (High)	I	V =2.4-5V		10	uA
Tristate Output Leakage Current (Low)	I	V =0.4V		-10	uA
Darlington Drive Current	I	V =1.5V R =390 only Port B	-1.5	3.8	mA

. CONNECTOR DESCRIPTION

The Output connector (B) for the PIO Interface has the following identifier:

AMP Latch 826/40 Pin

The connector has the following pin allocations:

Pin	Identifier	Diagram	Remarks
1	PA7		Port A output 7
2	Ground		
3	PA6		Port A output 6
4	Ground		
5	PA5		Port A output 5
6	Ground		
7	PA4		Port A output 4
8	Ground		
9	PA3		Port A output 3
10	Ground		
11	PA2		Port A output 2
12	Ground		
13	PA1		Port A output 1
14	Ground		
15	PA0		Port A output 0
16	Ground		
17	PB7		Port B output 7
18	Ground		
19	PB6		Port B output 6
20	Ground		
21	PB5		Port B output 5
22	Ground		
23	PB4		Port B output 4
24	Ground		
25	PB3		Port B output 3
26	Ground		
27	PB2		Port B output 2
28	Ground		
29	PB1		Port B output 1
30	Groun		
31	PB0		Port B output 0
32	Ground		
33	ASTB		Port A Strobe
34	Ground		
35	BSTB		Port B Strobe
36	Ground		
37	ARDY		Port A READY
38	Ground		
39	BRDY		Port B READY
40	Ground		

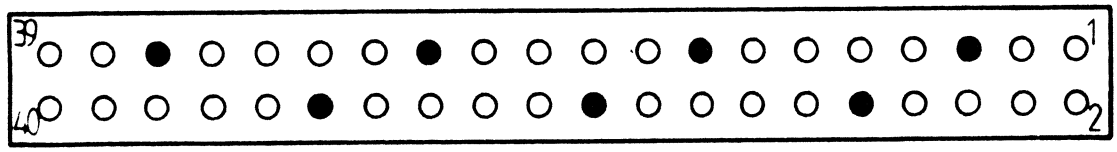


Fig.8: View of the Input/Output Connector (B)

8. ORDERING INSTRUCTIONS

Description	Part Number	Remarks
ITT 3030 Parallel Input/Output PCB	59712142	16 inputs/outputs 2 Ports
Interface Connector		Male for I/O Connector (B)

Standard Elektrik Lorenz AG
Gruppenbereich
Private Kommunikationssysteme
Produktbereich Microcomputer
Postfach 1570
D-7530 Pforzheim

Radiofabrik Ingelen, Figer & Co.
Schottenfeldgasse 13-15
A-1070 Wien

Standard Telephon & Radio AG
Brandschenkestraße 178
CH-8027 Zürich

ITT Consumer Products (UK) Ltd.
Chester Hall Lane
Basildon
Essex SS14 3BW
Great Britain

Order No. 7950128002 GB