

- NOTES**
- - OFF PAGE REFERENCE
 - △ - BUSS ORIENTATION
 - - - - - BUSSED SIGNALS

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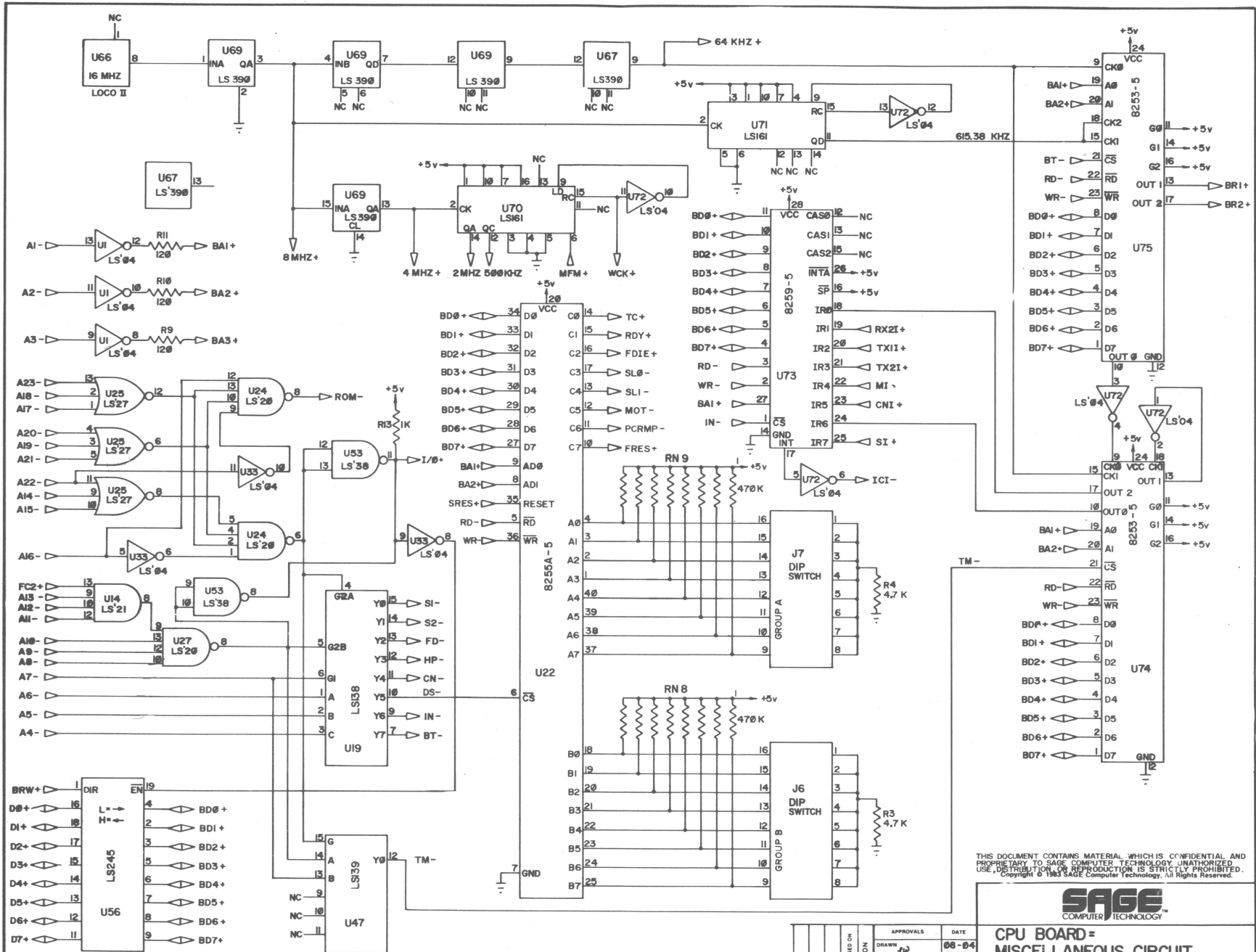


CPU BOARD PROCESSOR CIRCUIT

APPROVALS	DATE
DRAWN: [Signature]	08-01 1983
CHECKED:	
REVISED:	
APPLICATION	
NET AS ST	USEG-2K

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. BREAK OUTSIDE CORNERS. DO NOT SCALE DRAWING. TOLERANCES ARE DECIMALS ANGLES PART # **CB0002** REV. **PAGE 1** OF **9**

REV	BY	ECO #	DATE	APPR.



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CPU BOARD = MISCELLANEOUS CIRCUIT

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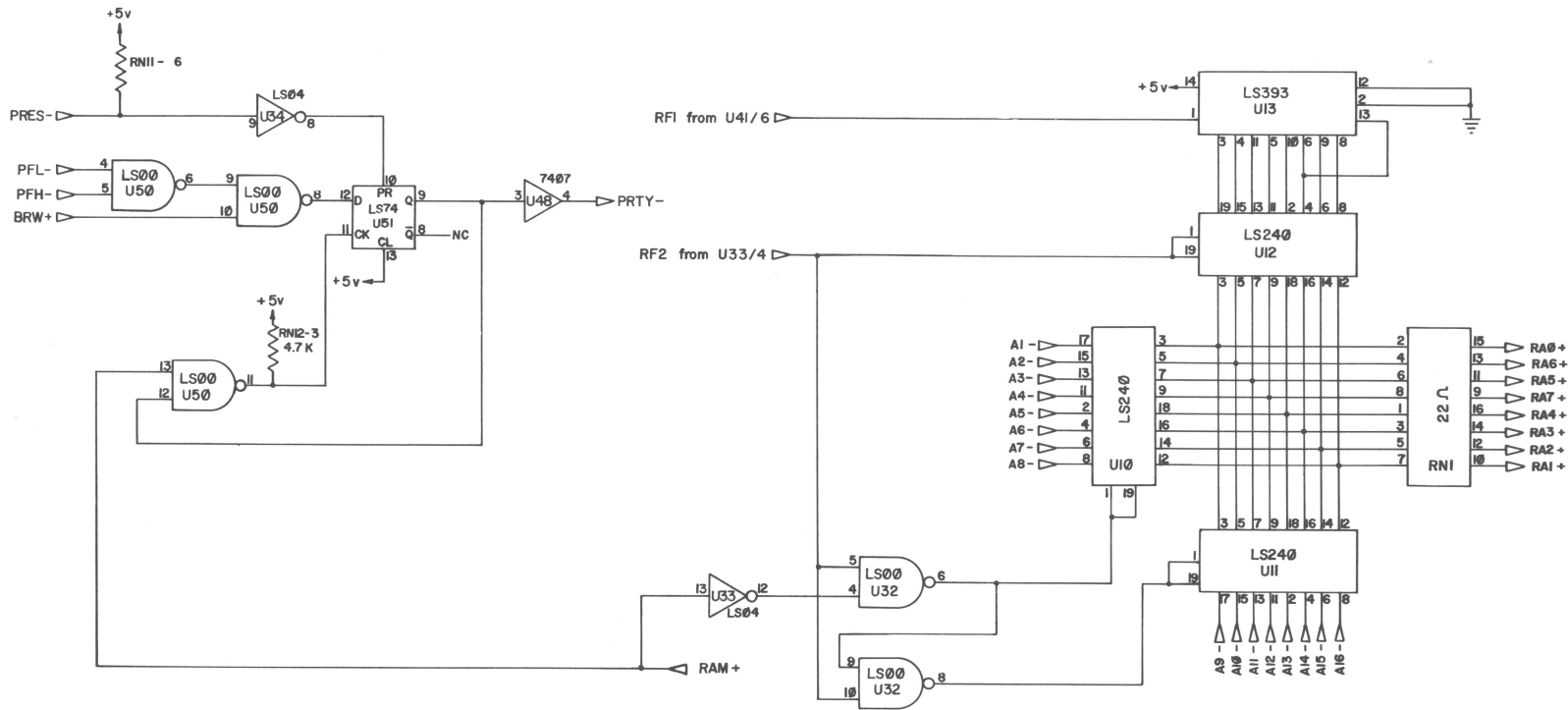
APPROVALS DATE
 DRAWN 06-04 1983
 CHECKED
 ISSUED

PART # CB0002

PAGE 2 OF 9

REV	BY	ECO #	DATE	APPR

REV	BY	ECO #	DATE	APPR



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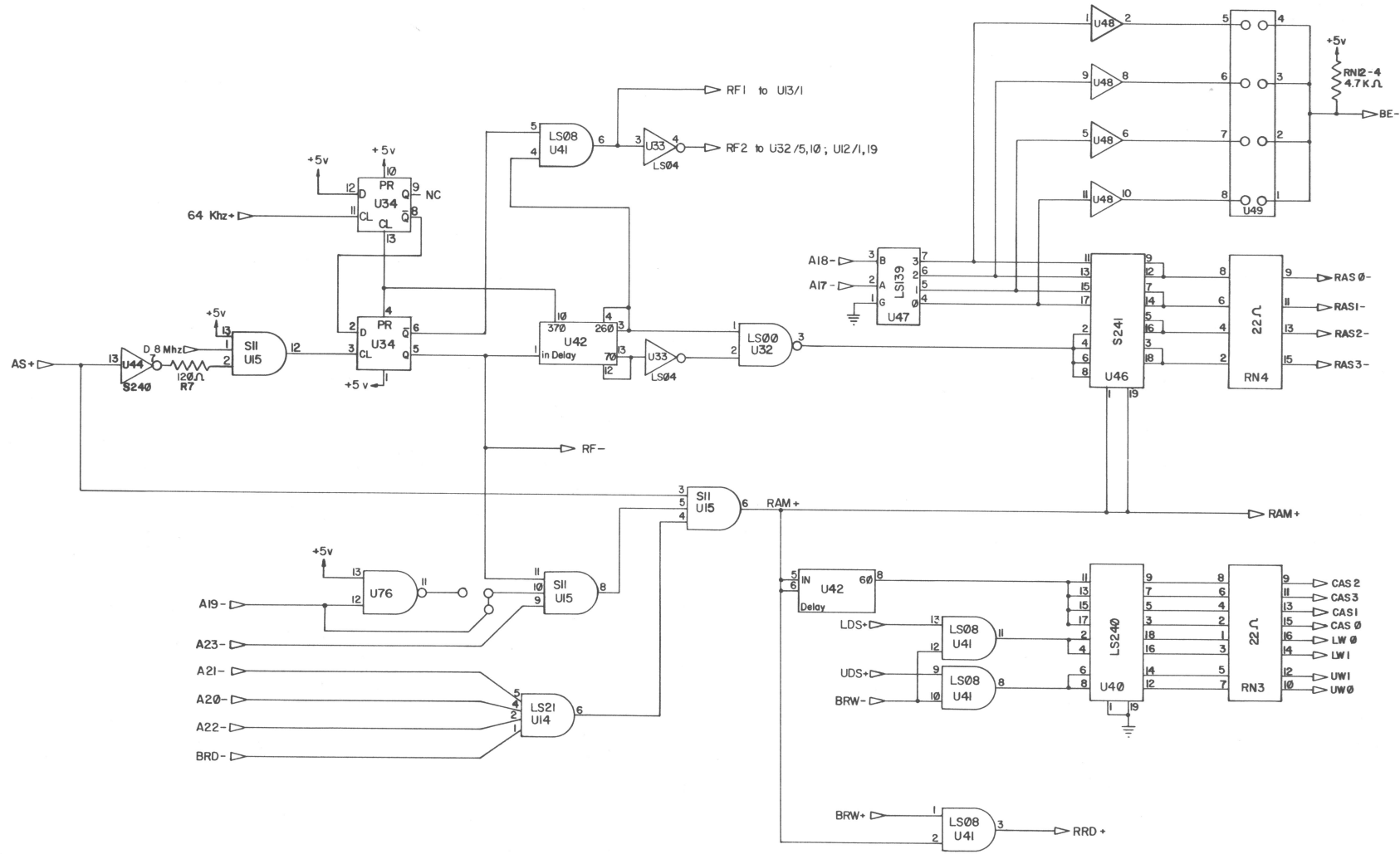
CPU BOARD = RAS/CAS GENERATION, PAGE 1 of 2

DESIGN	APPROVALS	DATE
APPLICATION	2/0	07-26-83
CHECKED		
DESIGNED		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. REFERENCE TO DIMENSIONS ARE TO DIMENSION LINES.
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DIMENSIONS ARE IN INCHES. REFERENCE TO DIMENSIONS ARE TO DIMENSION LINES.

PART # **BD0002.B** REV
PAGE 3 OF 9

REV	BY	ECO #	DATE	APPR



U42 (Delay line)	IN	70	90	250	260	370	375	IN	60
DDU-7-8087-1	1	13		3	3	12	12	5	8
DDU-7-8087	1		13				12	5	8
DDU-4-8150	1	12			4	10		5	8
ESC 98-61	1		12				10	6	8

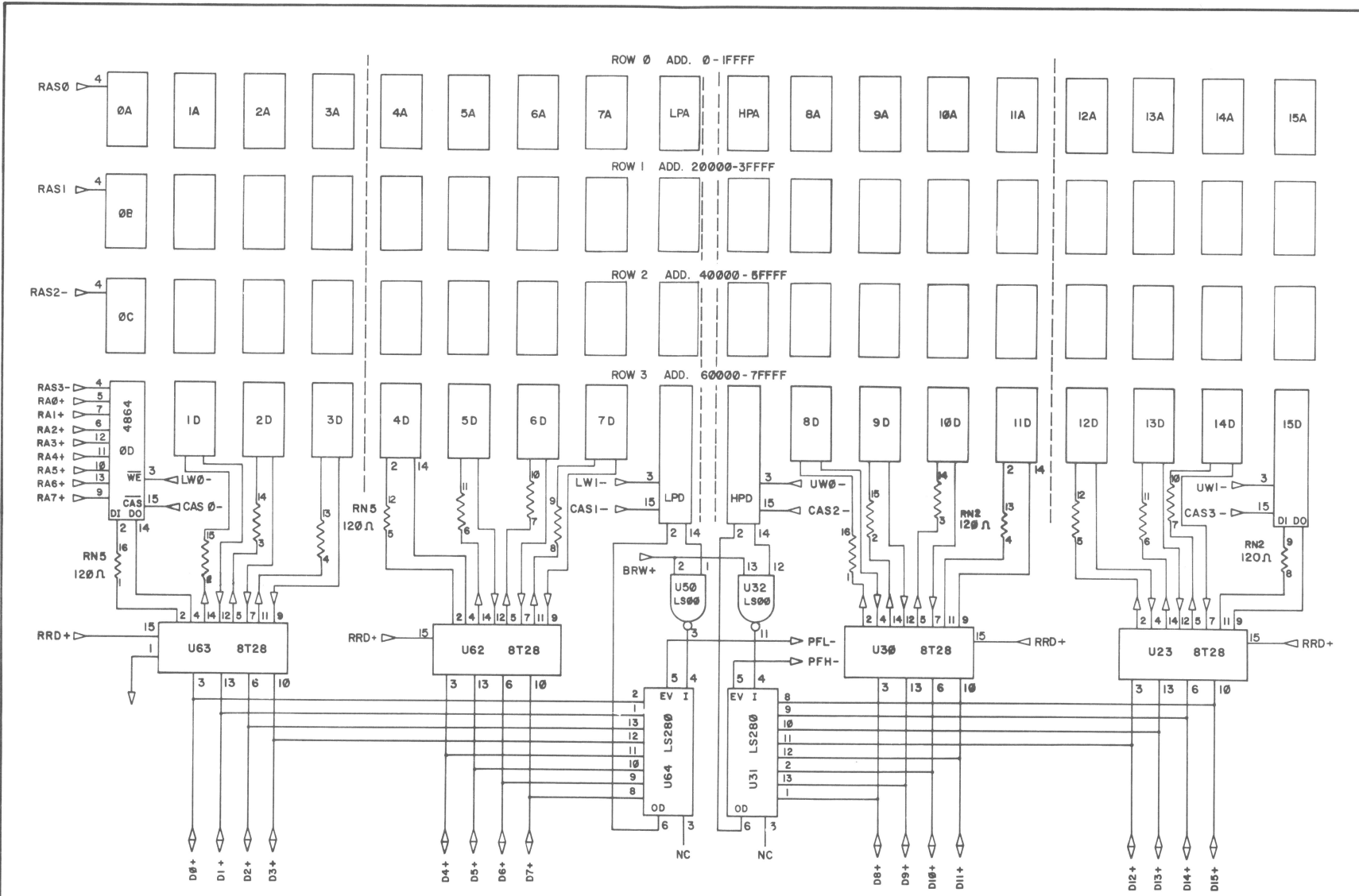
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CPU BOARD= RAS/CAS GENERATION,
GENERATION, PAGE 2 of 2

PART # **BD0002:B**
 REV. **4**
 PAGE **4** OF **9**

APPROVALS	DATE
DRAWN <i>[Signature]</i>	07-25-83
CHECKED	
INFORMED	



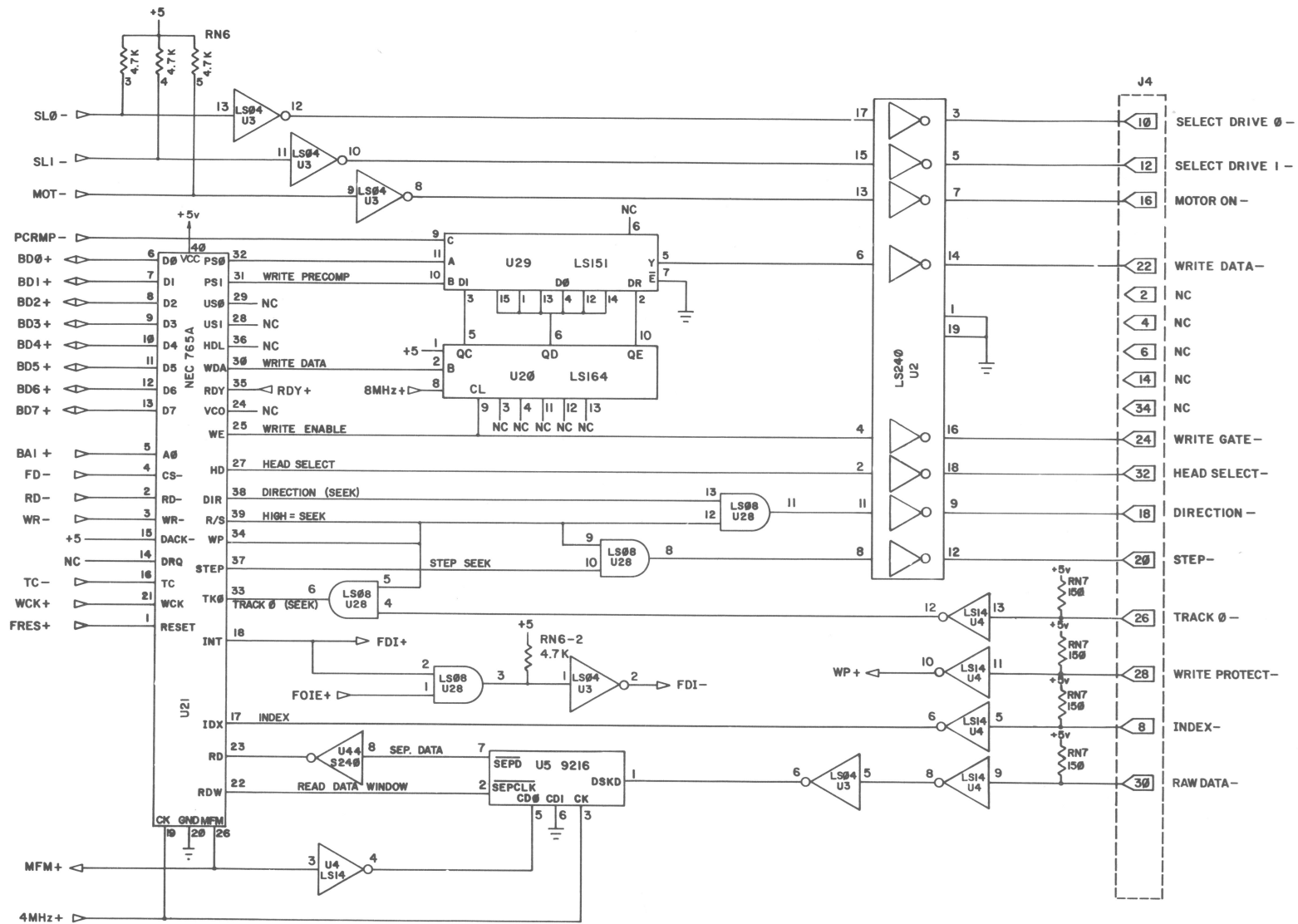
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APPROVALS		DATE
DRAWN		
CHECKED		
ISSUED		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES BREAK OUTS - CORNERS TO RANGES ARE DECIMALS ANGLES 1:2		PART # BD0002.B
CPU BOARD = RAM ARRAY		REV PAGE 5 OF 9

REV	BY	ECO	DATE	APPR

REV	BY	ECO	DATE	APPR



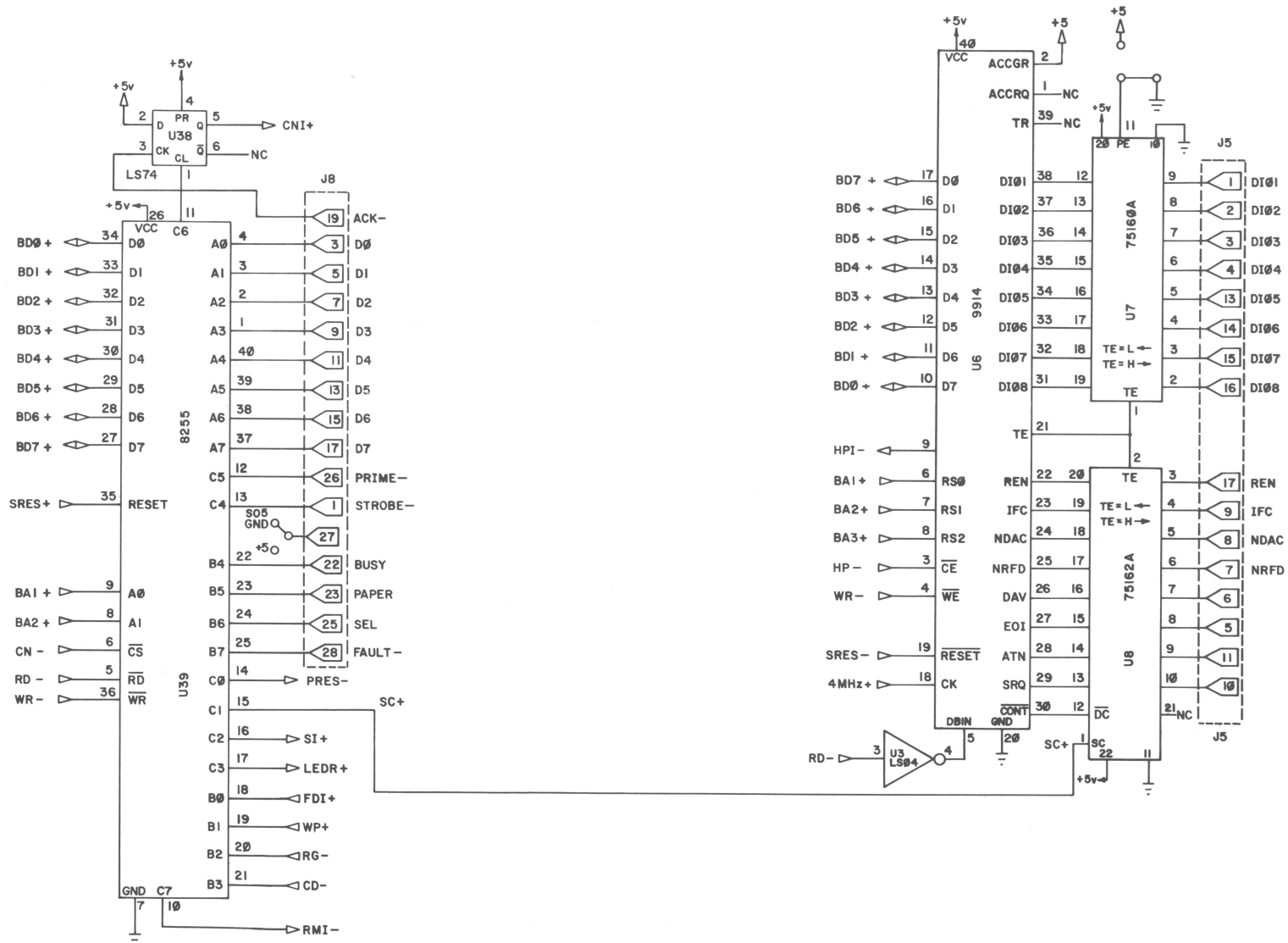
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APPROVALS		DATE	CPU BOARD- FLOPPY DISK CIRCUIT UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. BREAK OUTSIDE CORNERS DO NOT SCALE DRAWING TOLERANCES ARE: DECIMALS .005 ANGLES .2°	PART #	REV.
DRAWN				BD0002:B	
CHECKED					
ISSUED					

USED ON	NET ASSEMBLY	APPLICATION

REV	BY	ECO #	DATE	APPR



REV	BY	ECO #	DATE	APPR.

APPROVALS	DATE

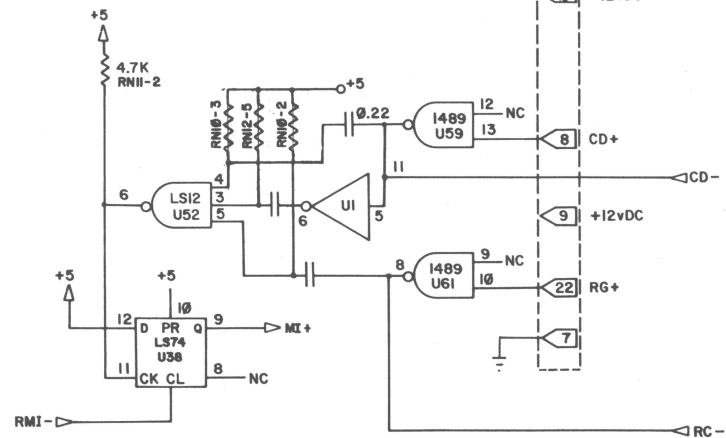
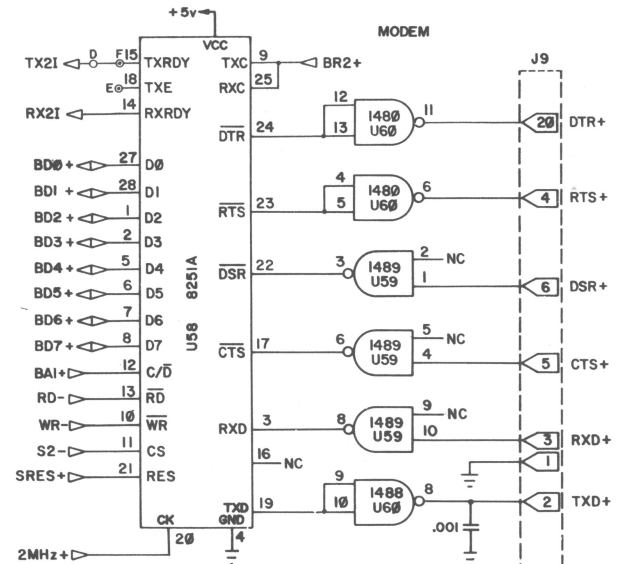
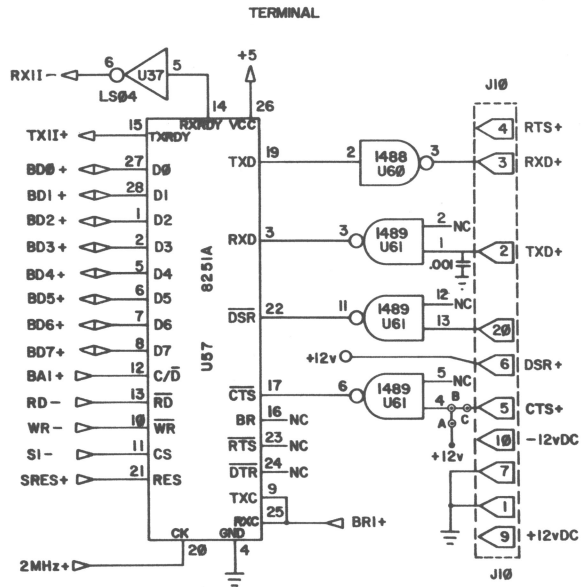
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CPU BOARD - COMMUNICATIONS CIRCUIT, Pg.1 of 2

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING
TOLERANCES ARE:
.10 ± .02
ANGLES
± 3°

PART # **BD0002B** REV.
PAGE 7 OF 9



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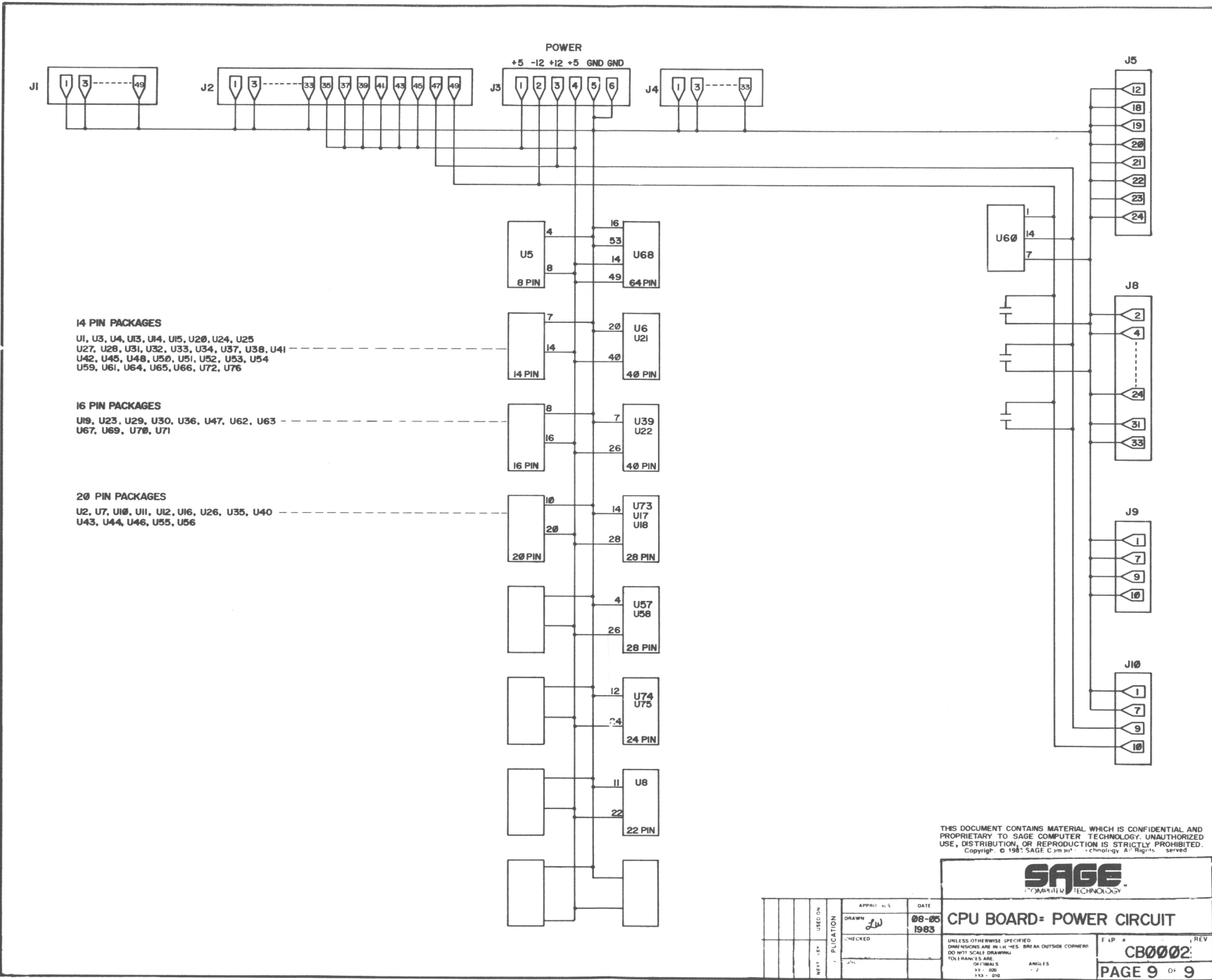
CPU BOARD COMMUNICATIONS CIRCUIT Pg. 2 of 2

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES - BREAK OUTSIDE CORNERS
DO NOT SCALE DRAWING
TOLERANCES ARE:
DECIMALS .01 ± .005
FRACTIONS 1/16 ± .005

PART #
BD0002:B
REV.
1
PAGE 8 OF 9

REV	BY	ECO #	DATE	APPR.

NET ASBY	USED ON	APPLICATION	APPROVALS	DATE

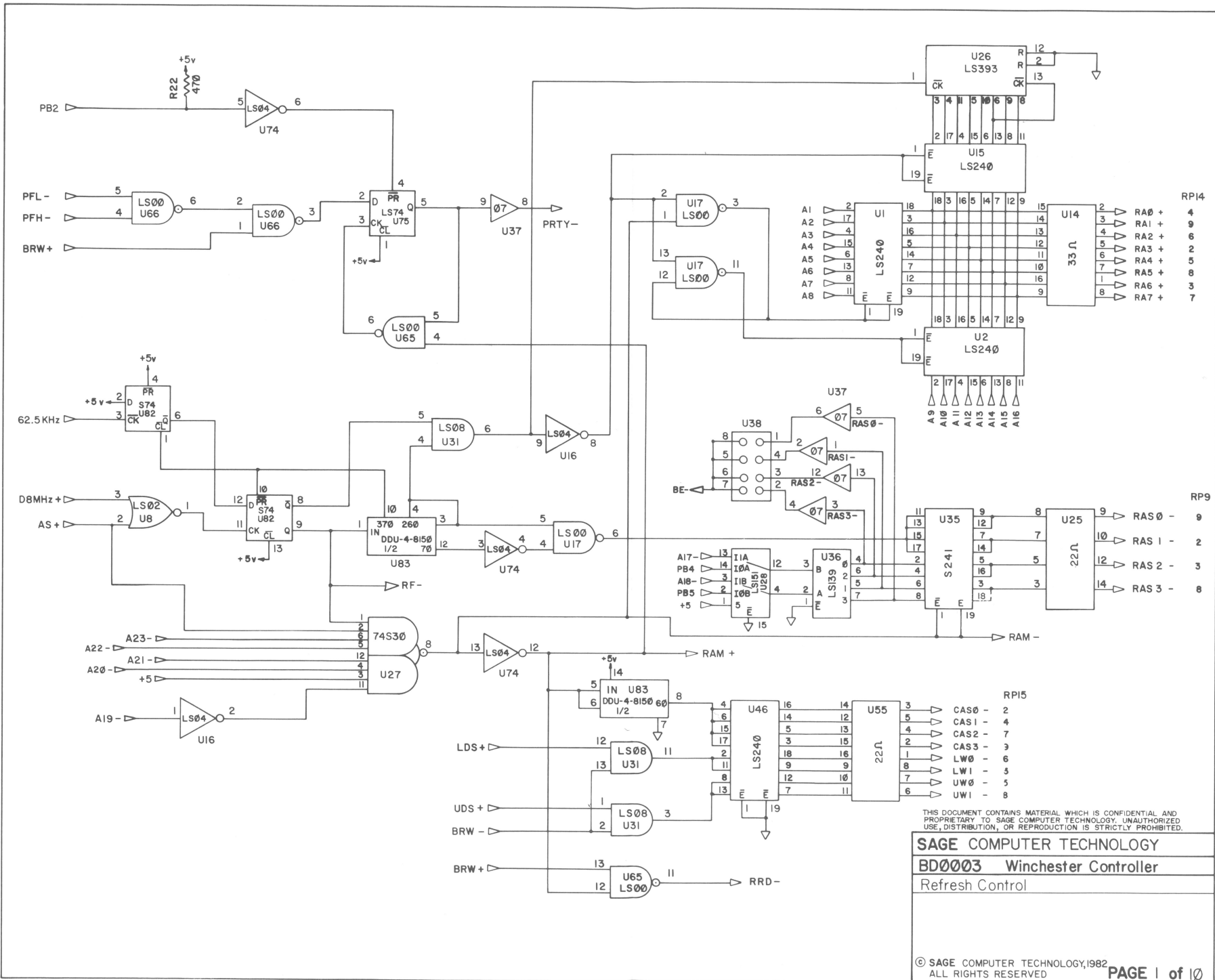


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CPU BOARD- POWER CIRCUIT

REV	BY	ECO #	DATE	APPR.	APPROVALS	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES - BREAK OUTSIDE CORNERS DO NOT SCALE DRAWING TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX .000 .001 .005	F.P.#	REV
					DRAWN	08-05 1983			
					CHECKED				
					RELEASED				

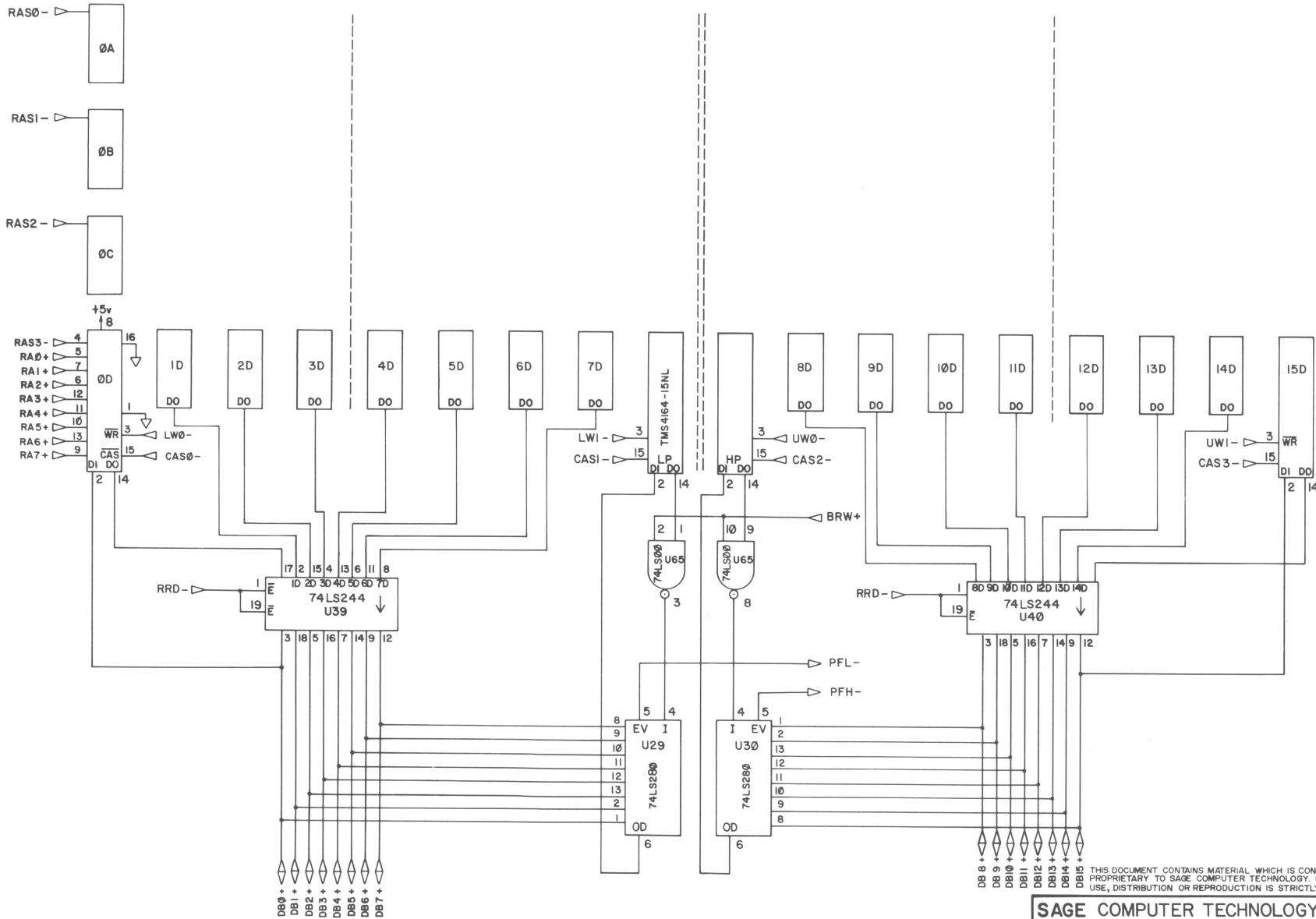


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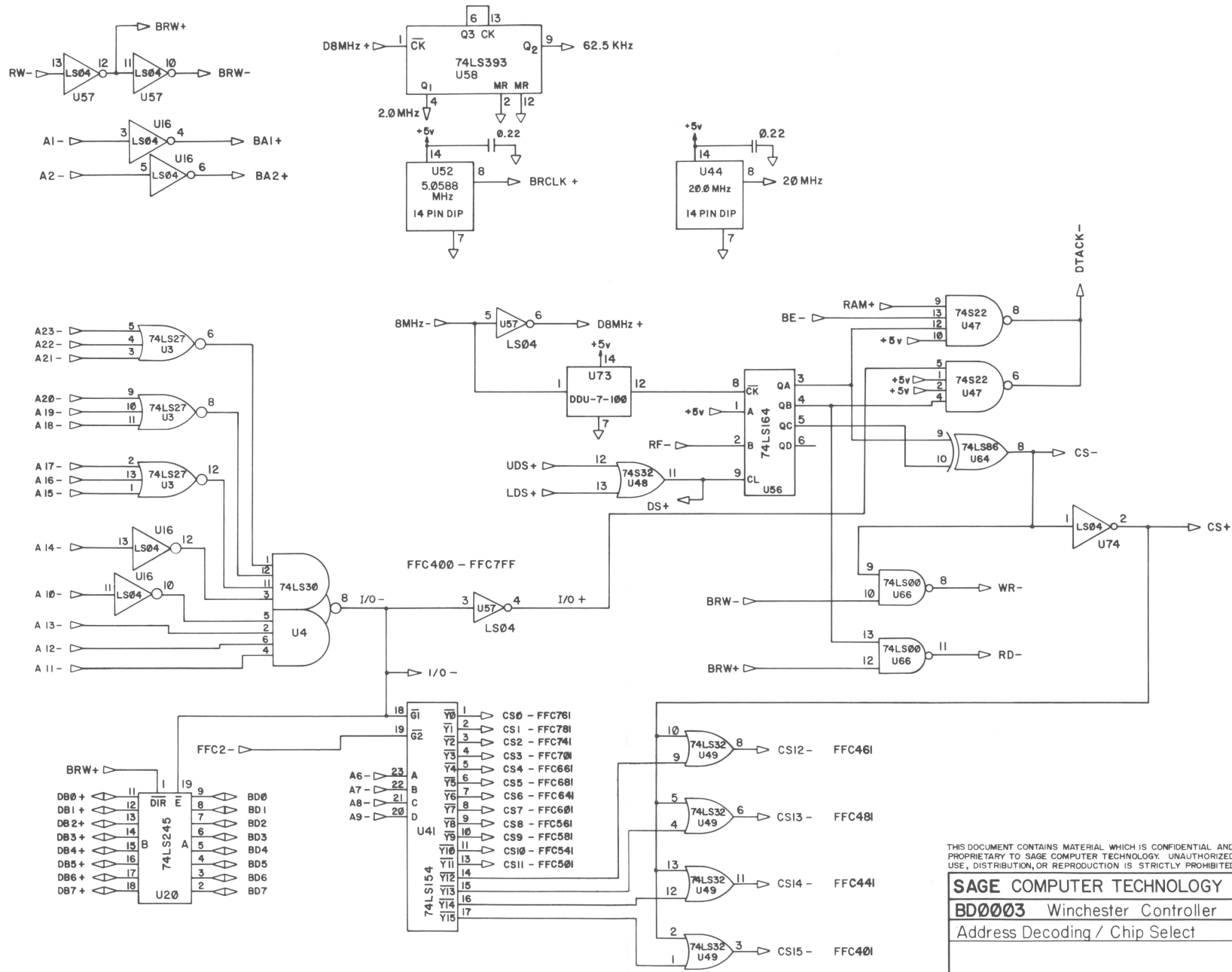
BD0003 Winchester Controller

Refresh Control



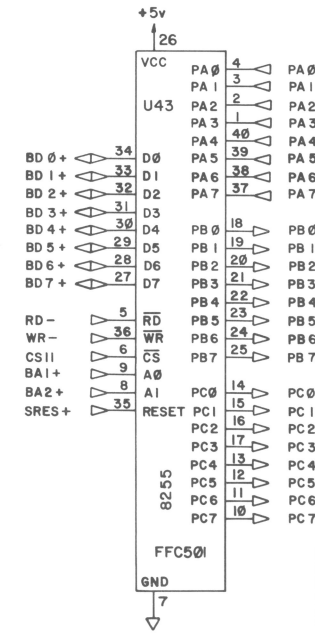
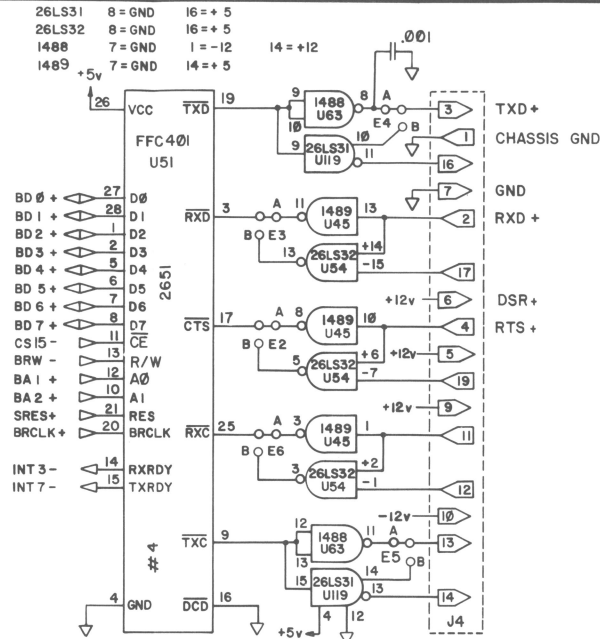
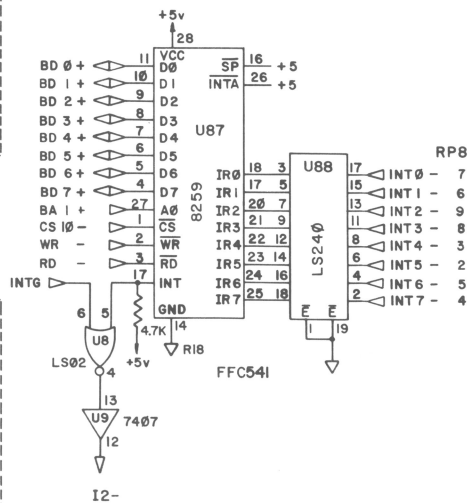
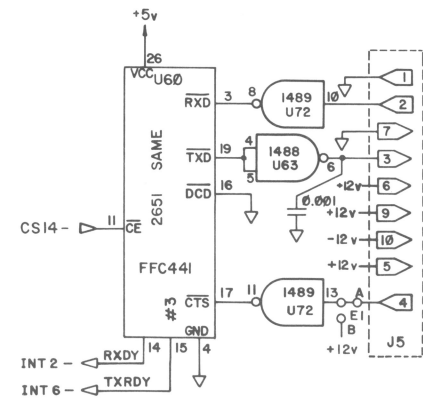
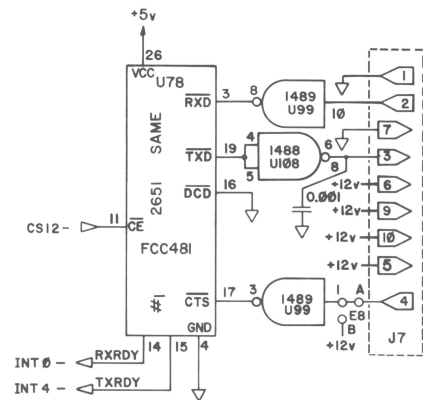
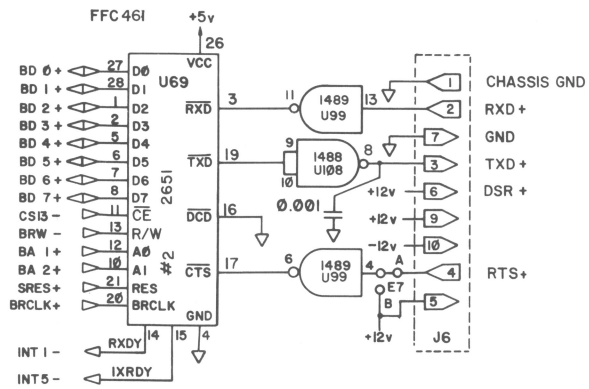
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BD0003 Winchester Controller
 Memory Array



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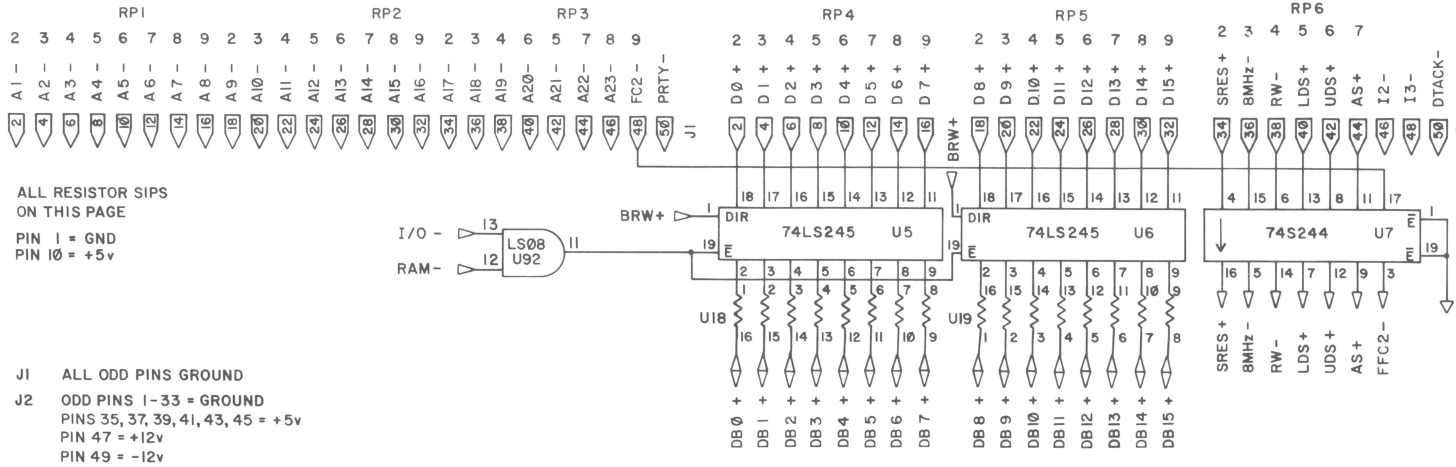
SAGE COMPUTER TECHNOLOGY
BD0003 Winchester Controller
 Address Decoding / Chip Select



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SAGE COMPUTER TECHNOLOGY
BD0003 Winchester Controller
 Serial I/O

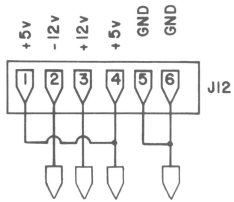
2/3
ALL THIS
PAGE



ALL RESISTOR SIPS
ON THIS PAGE

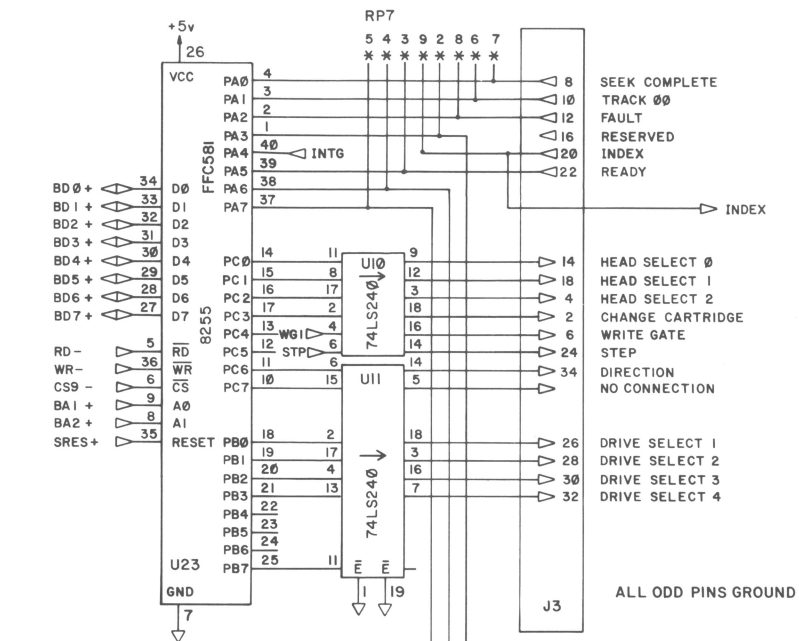
PIN 1 = GND
PIN 10 = +5v

J1 ALL ODD PINS GROUND
J2 ODD PINS 1-33 = GROUND
PINS 35, 37, 39, 41, 43, 45 = +5v
PIN 47 = +12v
PIN 49 = -12v

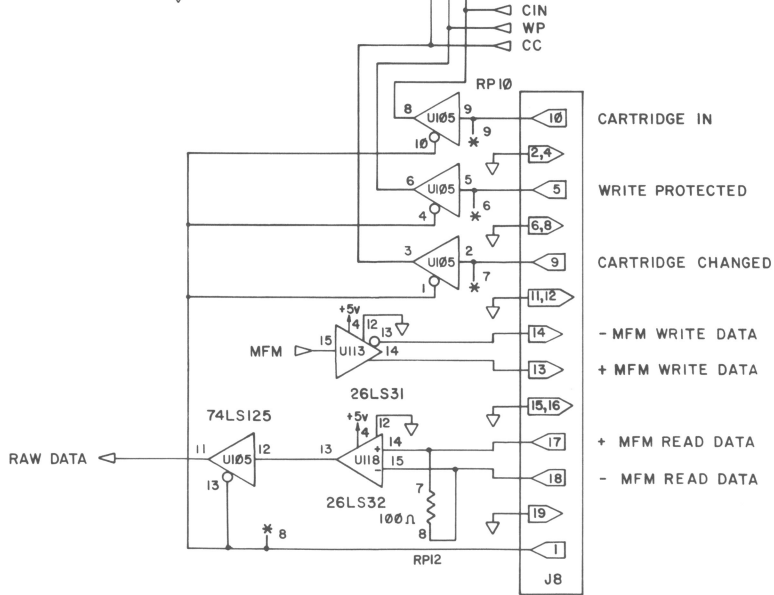


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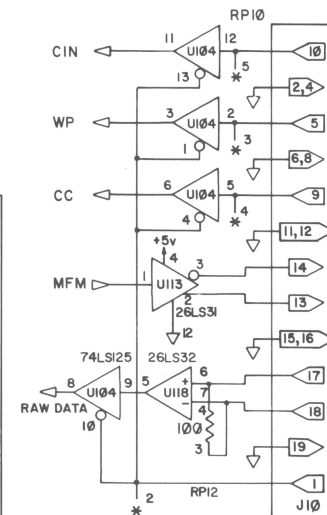
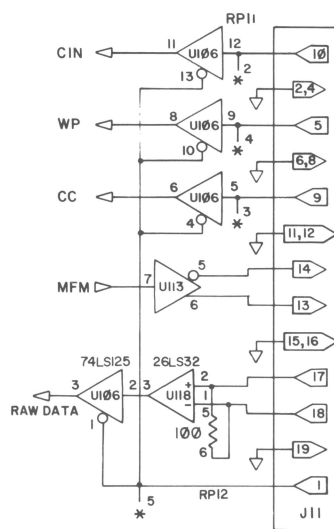
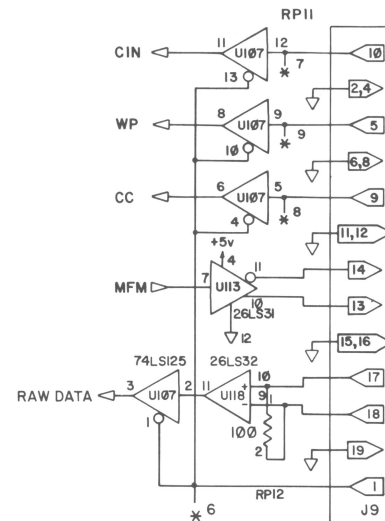
SAGE COMPUTER TECHNOLOGY
BD0003 Winchester Controller
Buss Connectors / Buffers



ALL ODD PINS GROUND

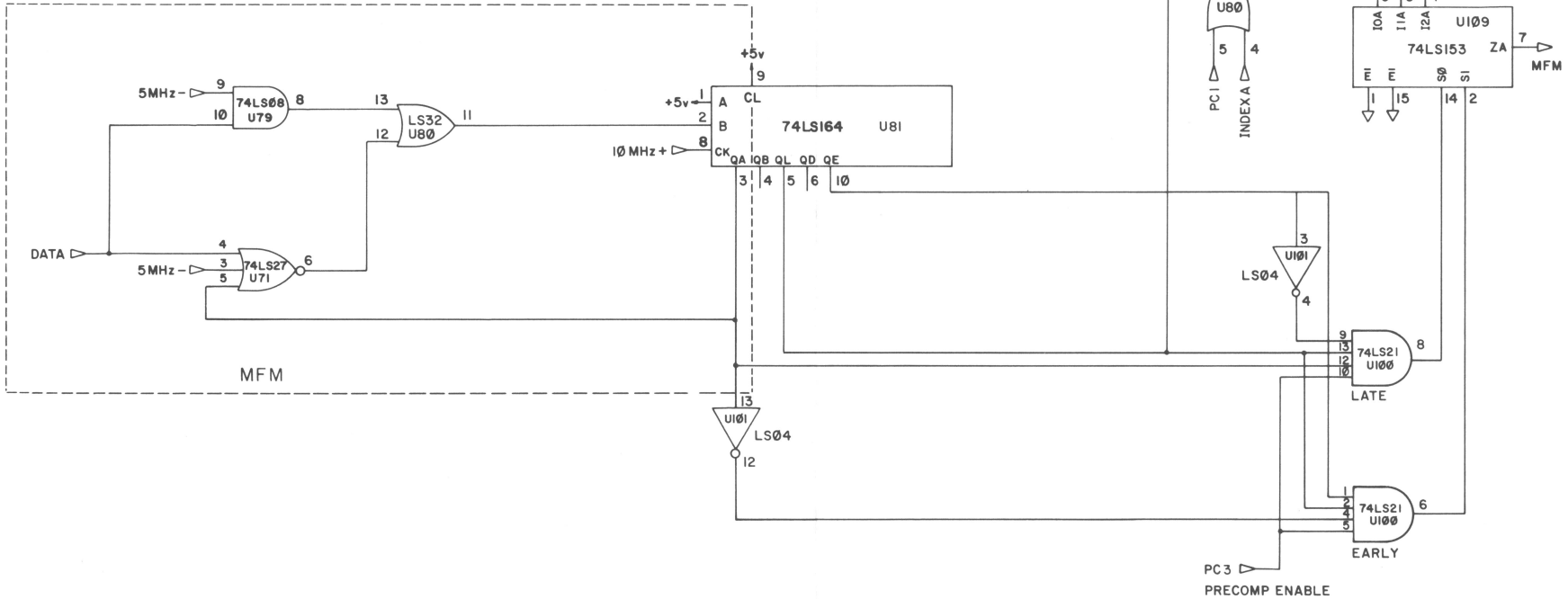
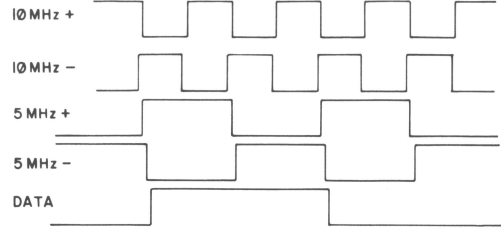


4 - 20 PIN CONNECTORS TOTAL



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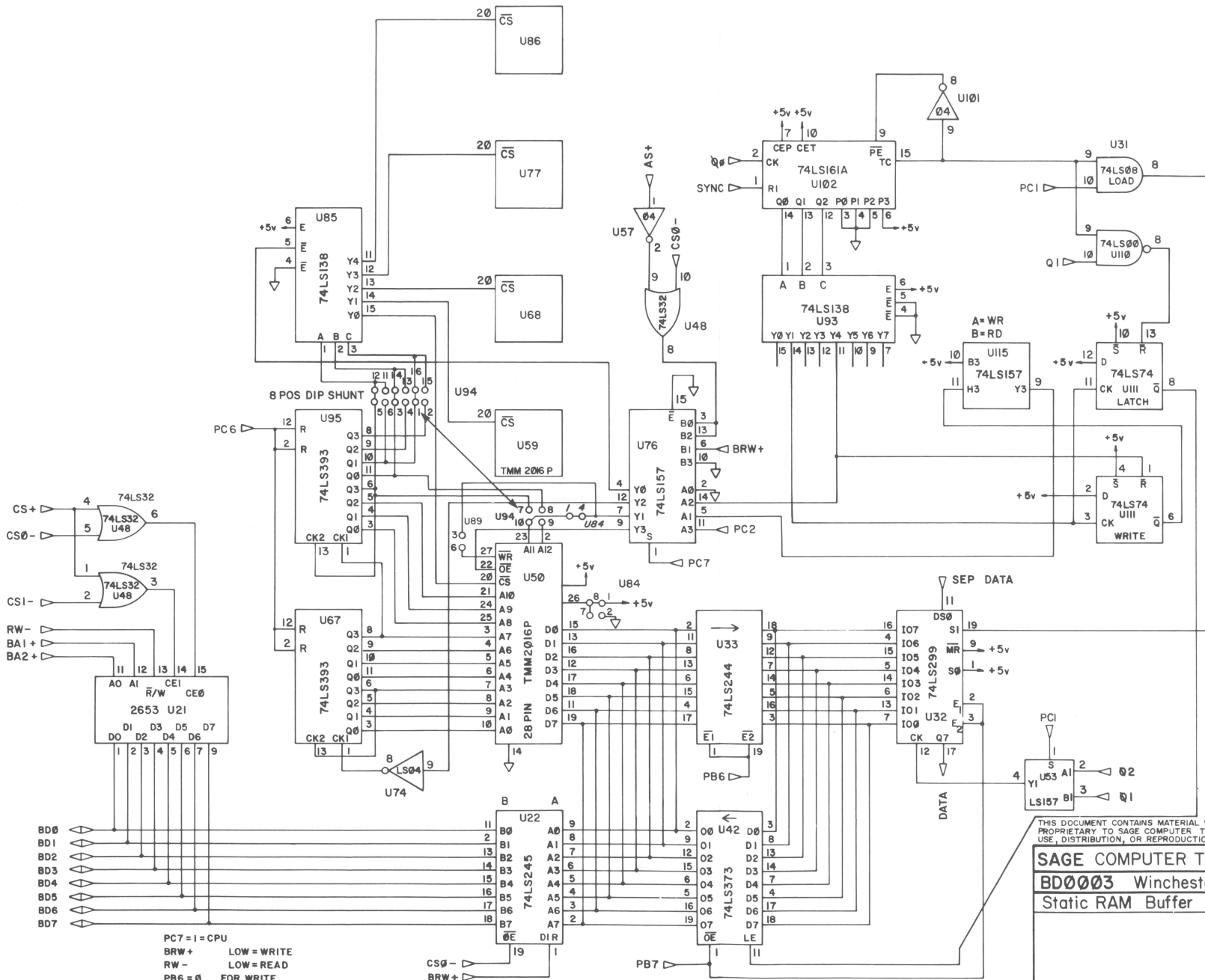
SAGE COMPUTER TECHNOLOGY
BD0003 Winchester Controller
 Winchester Connectors/ Buffers



PC1 = LOW = READ
 PC3 = LOW = PRECOMP DISABLED

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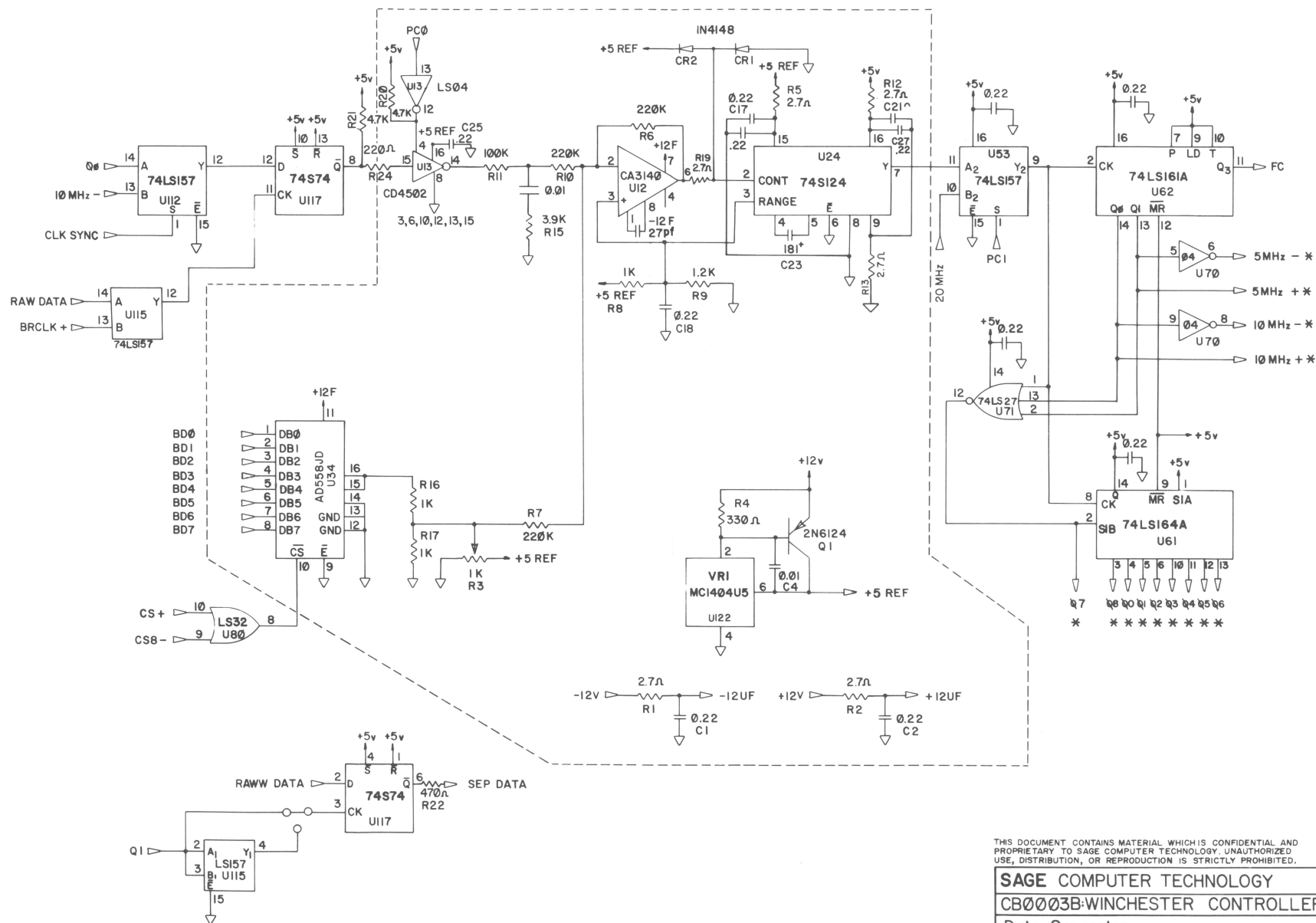
SAGE COMPUTER TECHNOLOGY
 BD0003 Winchester Controller
 MFM / Write Precomp



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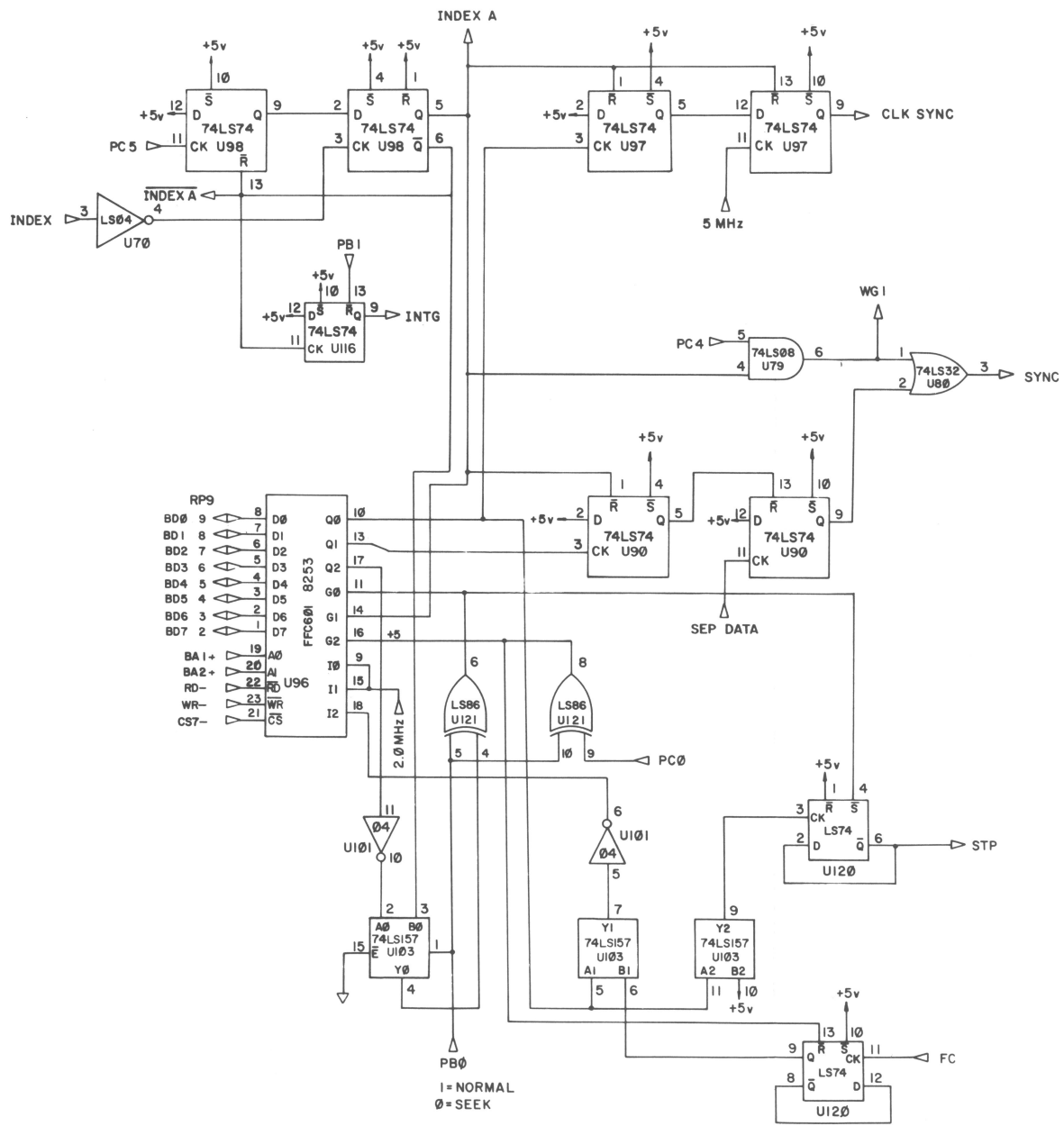
SAGE COMPUTER TECHNOLOGY
BD0003 Winchester Controller
Static RAM Buffer

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SAGE COMPUTER TECHNOLOGY
CB0003B:WINCHESTER CONTROLLER
Data Separator



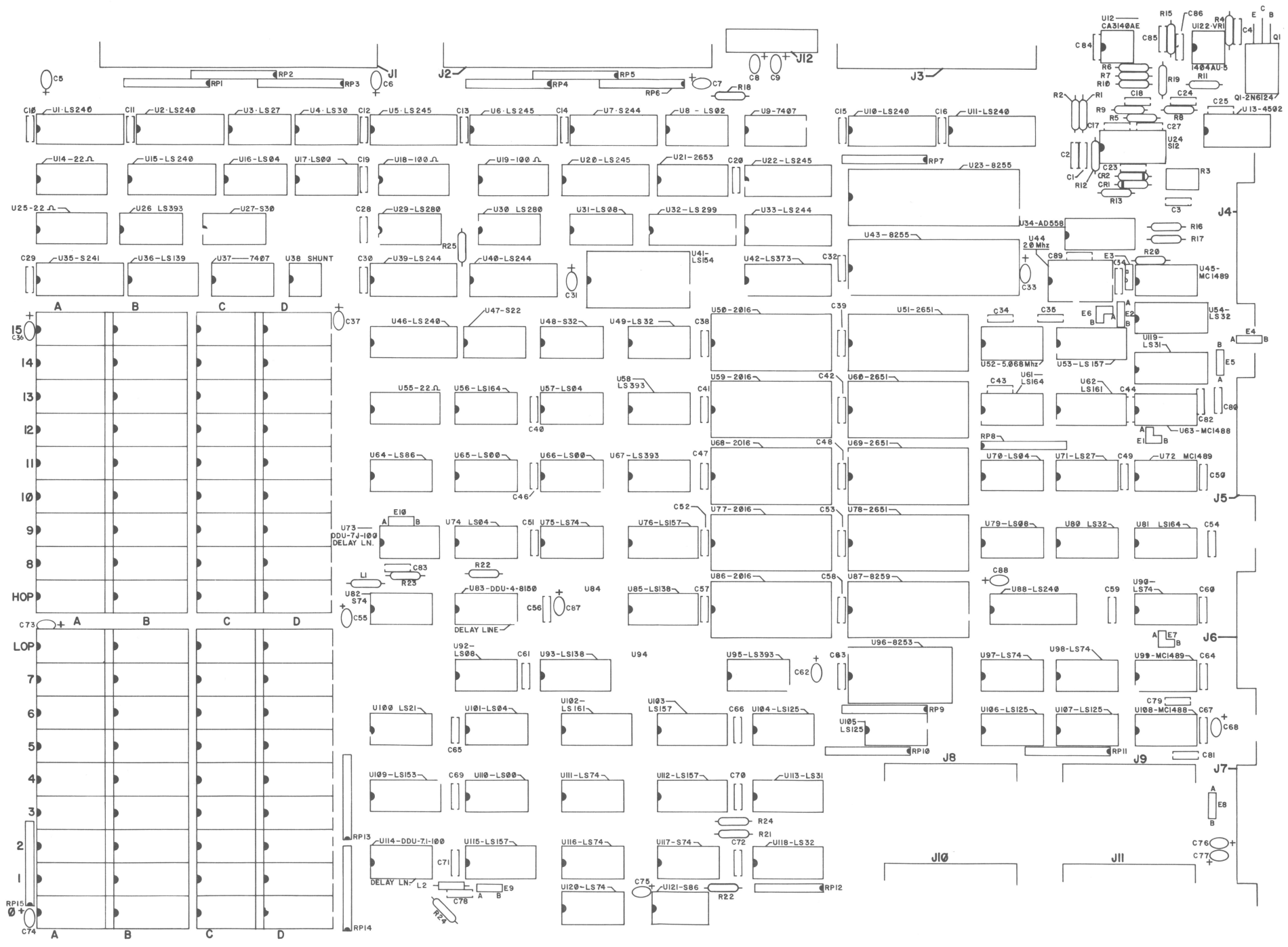
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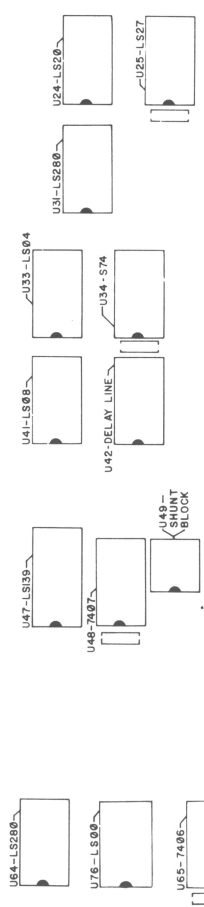
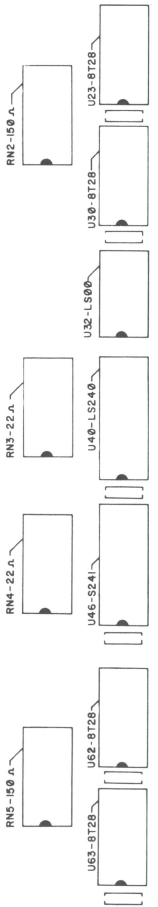
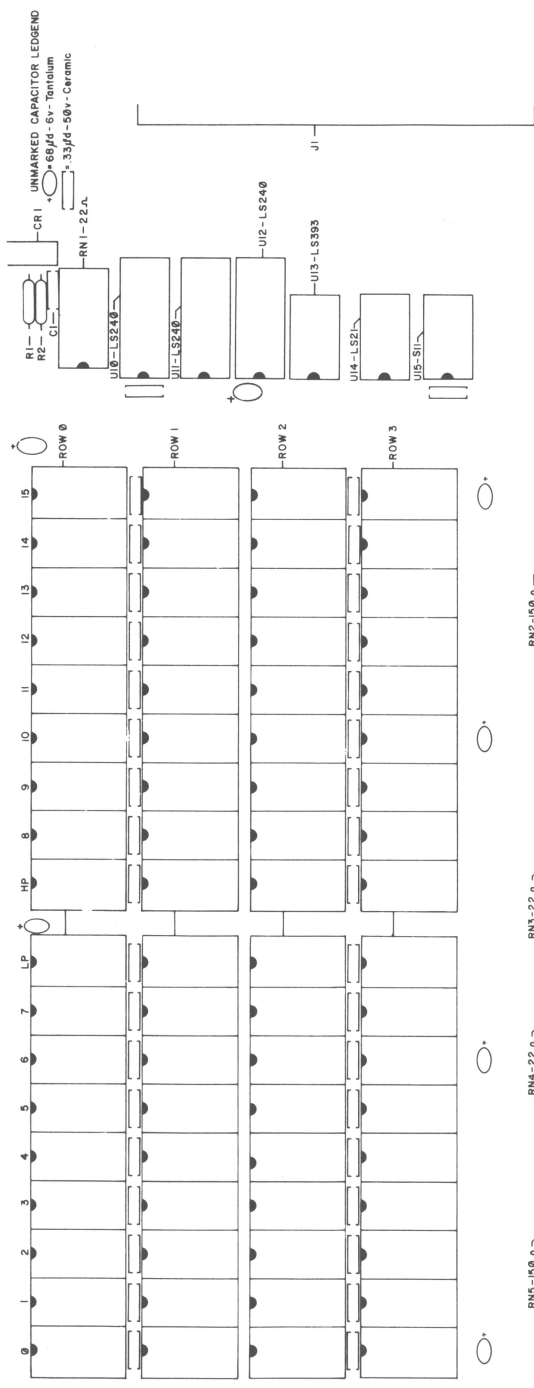
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CB0003 Winchester Controller
Buffered Seek Logic

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