INDUSTRIAL MICRO SYSTEMS

MODELS 450 & 440

Z80 PROCESSOR & I/O BOARDS

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GENERAL

The Model 450 Processor and the 440 I/O Boards are the Central Processing Unit (CPU) of the Industrial Micro Systems Series 5000 and 8000 Computer Systems. The Model 450 provides control and the 440 provides timing, and I/O interfacing for the system.

Control is accomplished by the NEC Z-80 LSI (Large Scale Integration) Micro Processor device. This is a fully Parallel, 8-bit, Bi-Directional, Bus Oriented Processing Unit with a 16-bit address capability, allowing up to 64 Kbytes of directly addressable memory. the Z-80 has a 1 μSEC instruction cycle time.

Timing is provided by the 8253 Programmable Interval Timer (PIT). The PIT is a Timer/Counter and functions as a general-purpose, multi-mode timing element that generates accurate time delays under software control.

The 6402 Universal Asynchronous Receiver/Transmitter (UART) interfaces the Z-80 Microprocessor to an Asynchronous Serial Data Channel. The UART converts input serial data to parallel data to be acted upon by the system. Output data is converted from parallel to serial to be placed on the RS-232 PORT.

The 8255 Programmable Peripheral Interface Circuit interfaces to Z-80 Microprocessor to three 8-bit parallel ports. These are located at the 50 pin I/O connector at the top of the 440 card. Each line is TTL buffered and has provision for termination network.

The Model 450 processor consists of a single Printed Circuit Board that nominally occupies the first slot (Slot 0) of 12 slots in the Series 5000 or 8000 Computer Systems. It interfaces with the rest of the system through the address, data, and control lines of the S-100 Bus System.

The 450 Processor board consists of the following functional divisions (See Figure 1).

- 8-bit Microprocessor Device (CPU)
- Priority Vectored Interrupt Circuitry

The 440 I/O Board consists of the following functions:

- 1024 by 8-bit ultraviolet Erasable Programmable Read-Only-Memory
- Programmable Interval Timer/Real Time Clock
- Two Universal Asynchronous Receiver/Transmitters (UART's)
- RS-232 Interface Logic
- Three 8-bit parallel ports

SPECIFICATIONS

. Word Size: Address 16 bits	
Data 8 bits	
. On-Board ROM:	1 Kbyte
. Directly Addressable Memory:	64Kbytes
. Clock Frequency:	4 MHz
. I/O Ports (Serial):	2
. 8 Bit Parallel Ports:	3
. Baud Rate:	75 to 9600 Baud
. PCB Dimensions:	5.25" x 10"
	(13.3 cm x 25.4 cm)
. Power Requirements:	440 +16 @ 60 ma
	+8 @ 500 ma
	-16 @ 40 ma
	450 +8 @ 700 ma

Z-80 MICROPROCESSOR

The Z-80 Processor is a Bi-Directional, Bus-Oriented, 8-bit Parallel LSI device with a 16-bit address capability, allowing up to 64 Kbytes of directly addressable memory. The Z-80 contains six 8-bit, general purpose working registers and an accumlator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The Z-80 has an external stack feature wherein any portion of memory may be used as a last-in/first-out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the six general-purpose registers. The 16-bit stack pointer contains the address of the next available location in the external memory. The program counter is a 16-bit register that contains the program address. The flag register contains six bits of condition code information which indicate the results of the ALU (Arithmetic Logic Unit) operation; Negative (N), Zero (Z), Overflow (V), Carry from Bit 7 (C), and Half-Carry from Bit 3 (H). These are used as testable conditions for the conditional branch instructions. This stack feature allows the ability to provide priority vectored interrupts.

The minimum instruction time for the Z-80 Microprocessor is 1 usec. Separate 16-bit address and 8-bit bi-directional data lines are used to facilitate easy interface to memory and I/O.

Memory and I/O interface control signals may be used to suspend processor operation and force the address and data lines to a high impedance state (Tri-State allowing Direct Memory Access (DMA) and multi-processor operation.

The Z-80 provides 158 variable length instructions (see Z-80 instruction set). In addition to performing basic processing functions, the processor is capable of responding to Real-Time Program Interrupts, Automatic Restart in response to the RESET/Power-On RESET signals, and Direct Memory Access operations.

FIGURE 1 - Z80 CPU BLOCK DIAGRAM

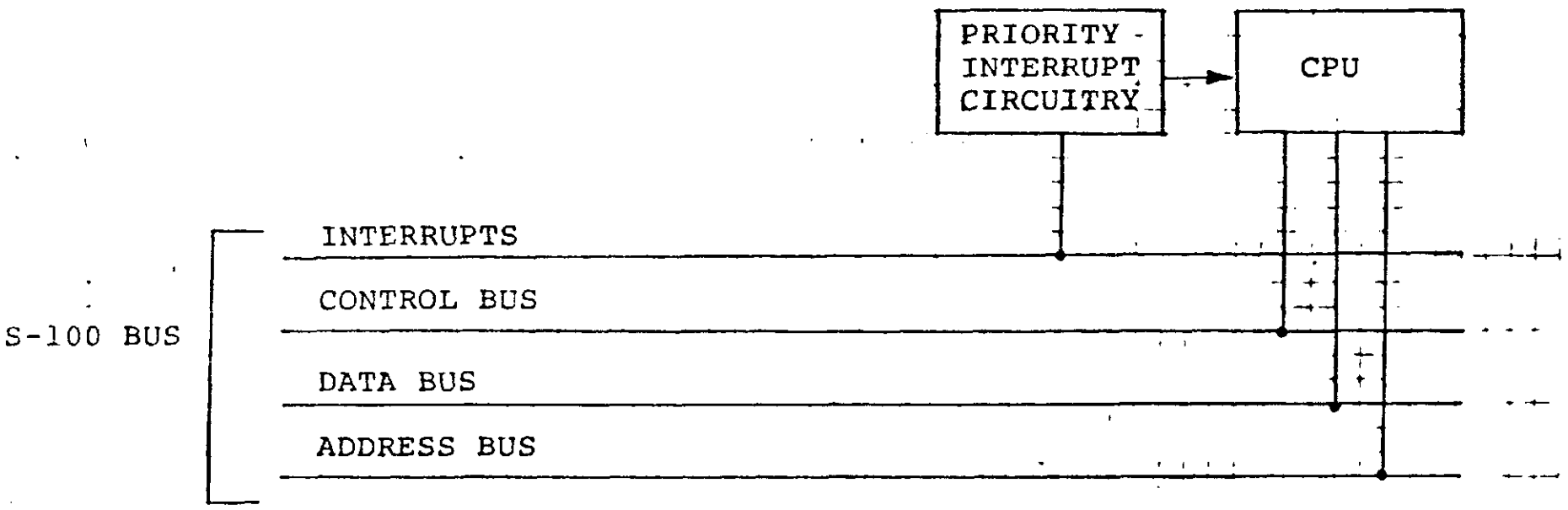
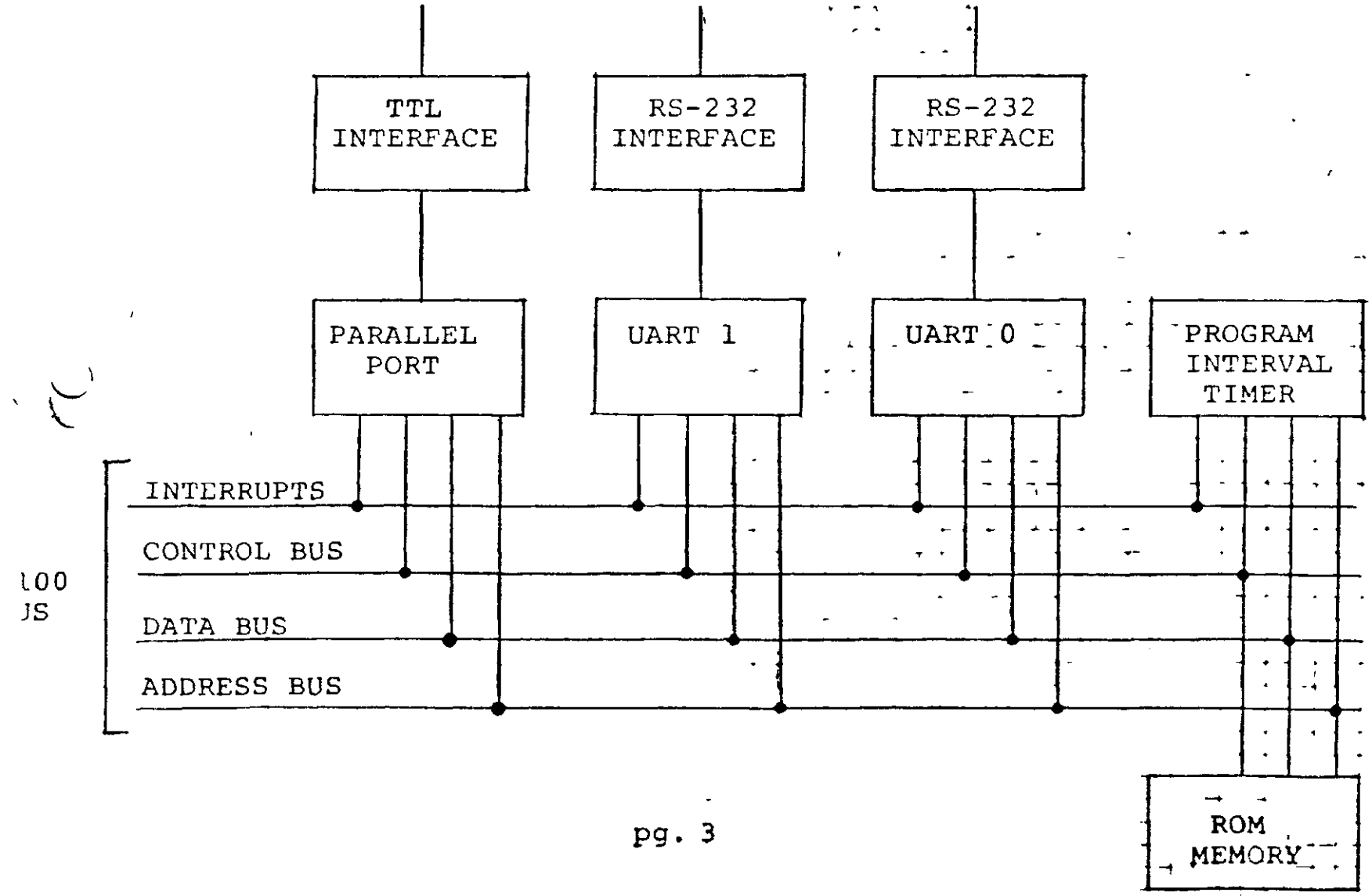


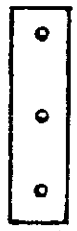
FIGURE 2 - I/O BOARD BLOCK DIAGRAM



MODEL 450 Z80 CPU BOARD

SHUNT AND JUMPER OPTIONS

JA



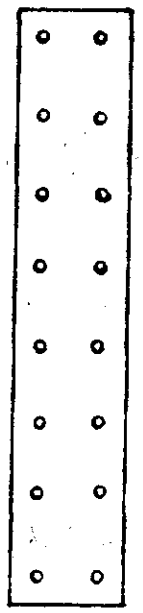
WAIT STATE SELECT LOC. 2.5A

No Shunts = No Memory Wait State

Shunt JA 1-2 = Provides One Wait State

Shunt JA 2-3 = Provides Two Wait States

JB



16	A15
15	A14
14	A13
13	A12
12	A11
11	A10
10	A 9
9	A 8

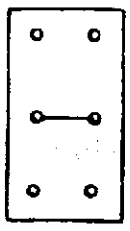
POWER ON ADDRESS SELECT LOC. 9.5A

Shunt Off = 1 Shunt On = 0

(All Shunts Off Power On Address = $FF00_{16}$)

(All Shunts On Power On Address = 0000_{16})

JC

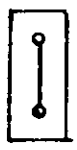


6	
5	4MHZ
4	2MHZ

CPU CLOCK SELECT: LOC. 3.5B

Cut Etch Jumper to Change CPU Clock

JD



ADDRESS MIRROR SELECT LOC. 3.5B

Cut Etch Jumper for No Address Mirror

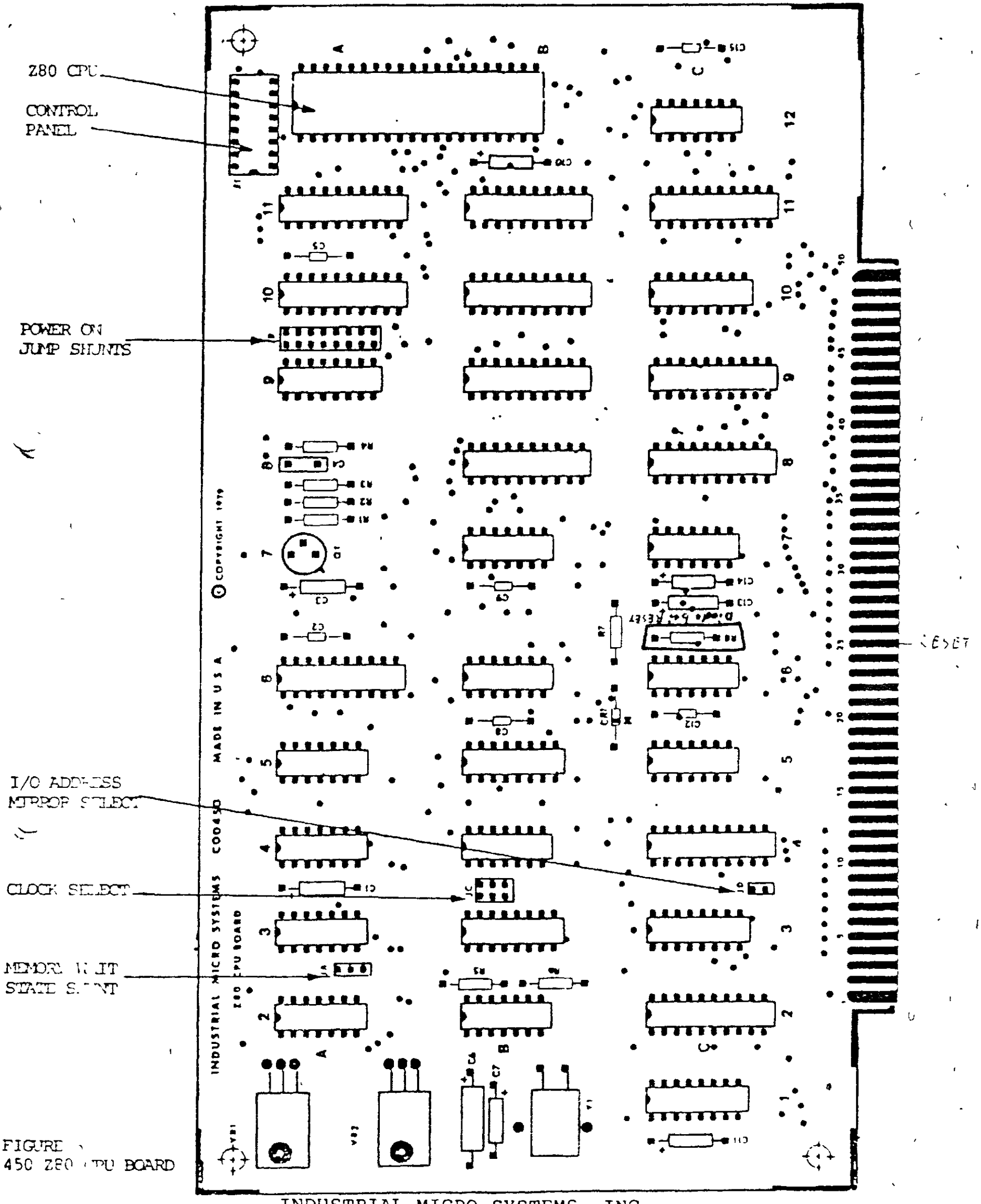
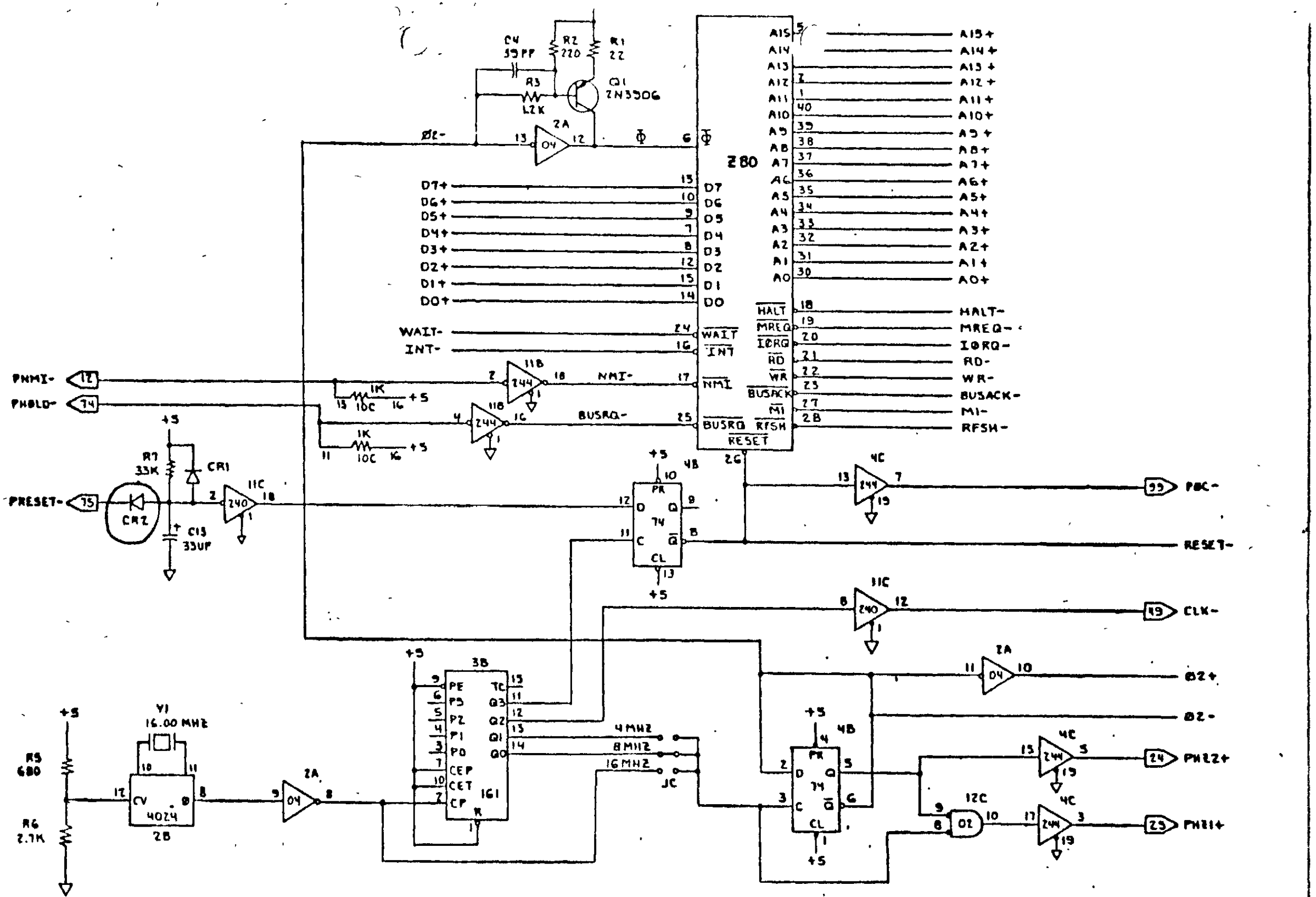
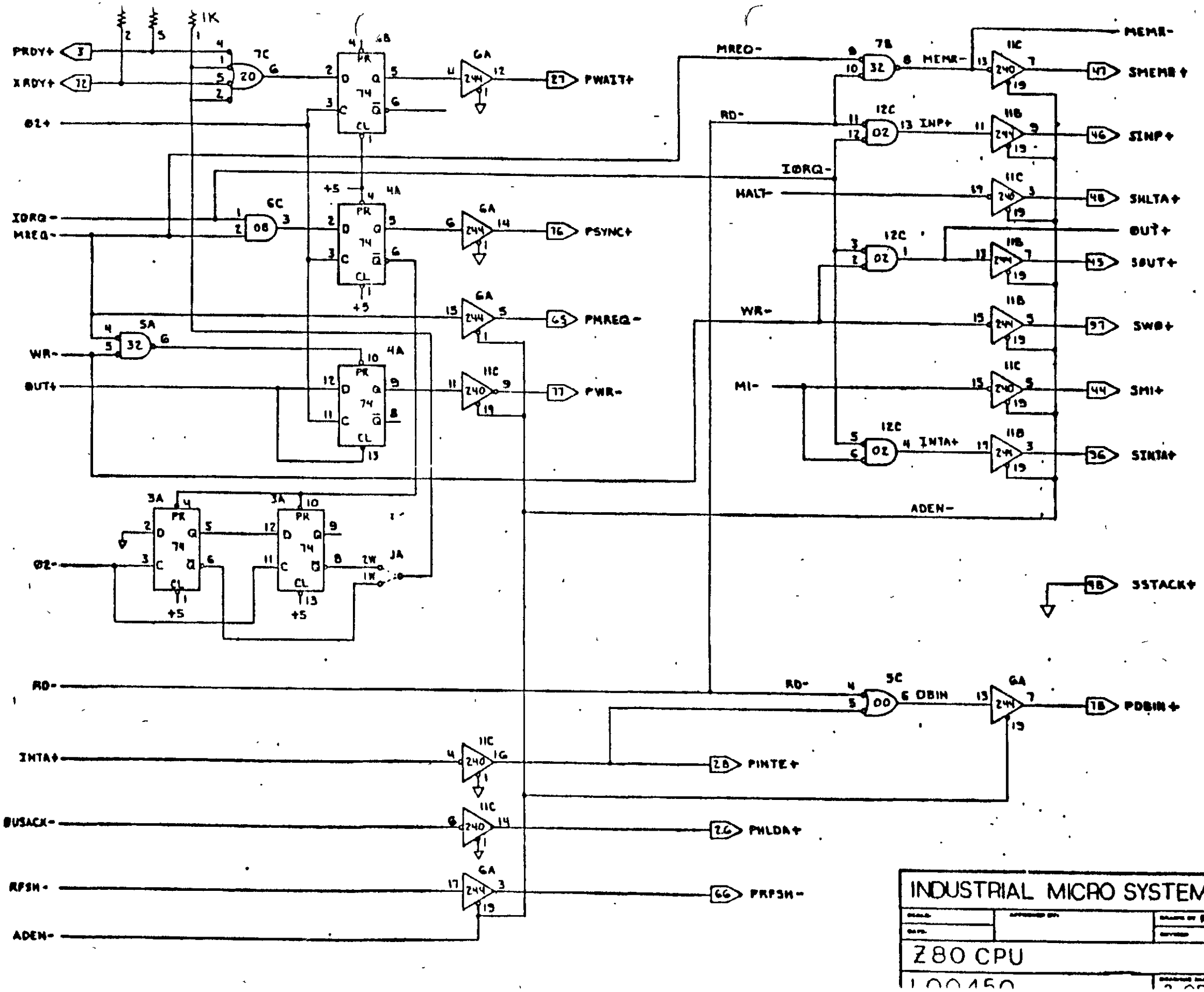


FIGURE
450 Z80 CPU BOARD



1. ALL RESISTORS ARE 1/4W ± 5%
2. ALL DIODES ARE SILICON SWITCHING

INDUSTRIAL MICRO SYSTEMS	
	DRAWN BY RJV
Z80 CPU	
L00450.	SHT 1 OF 4



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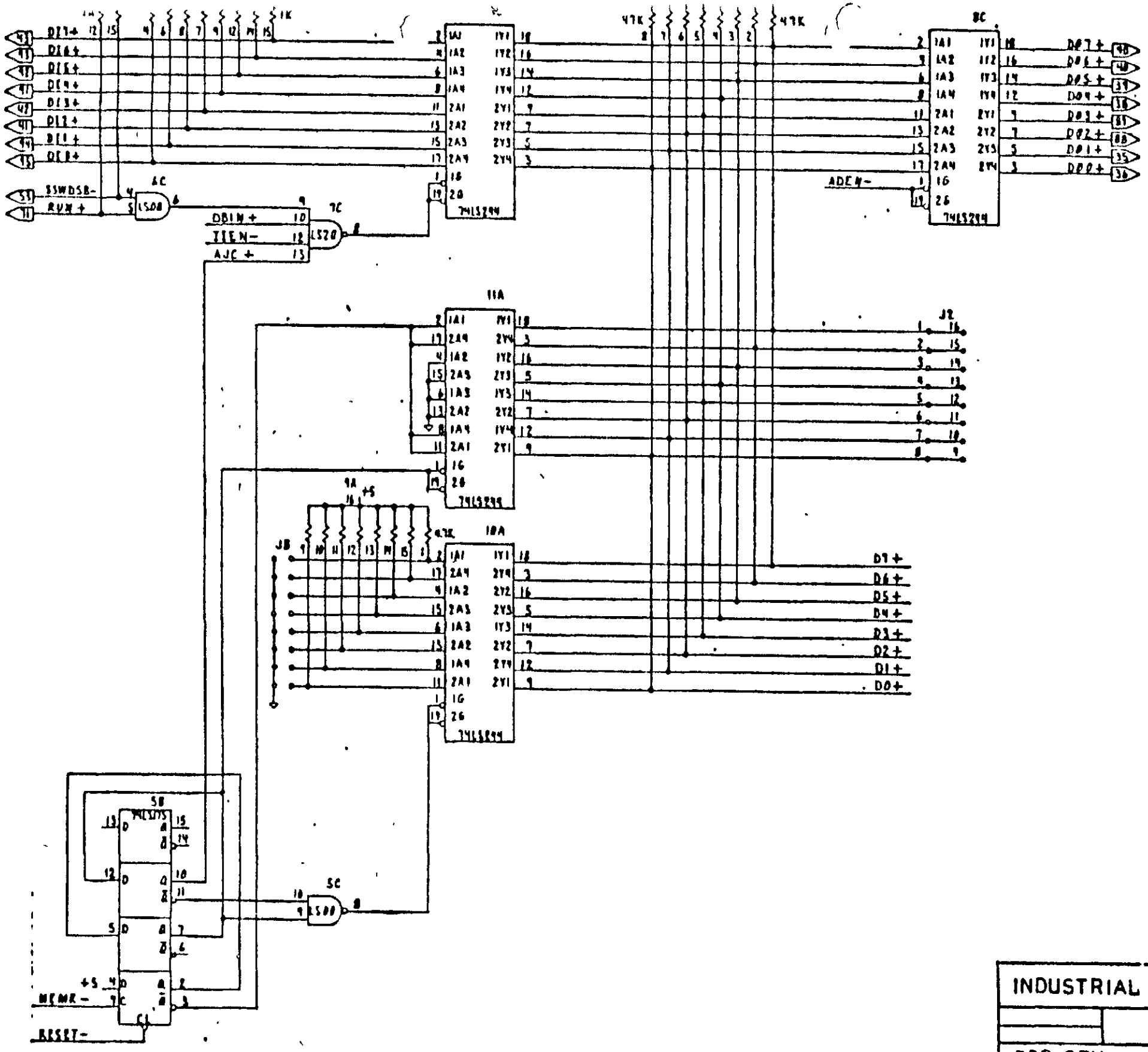
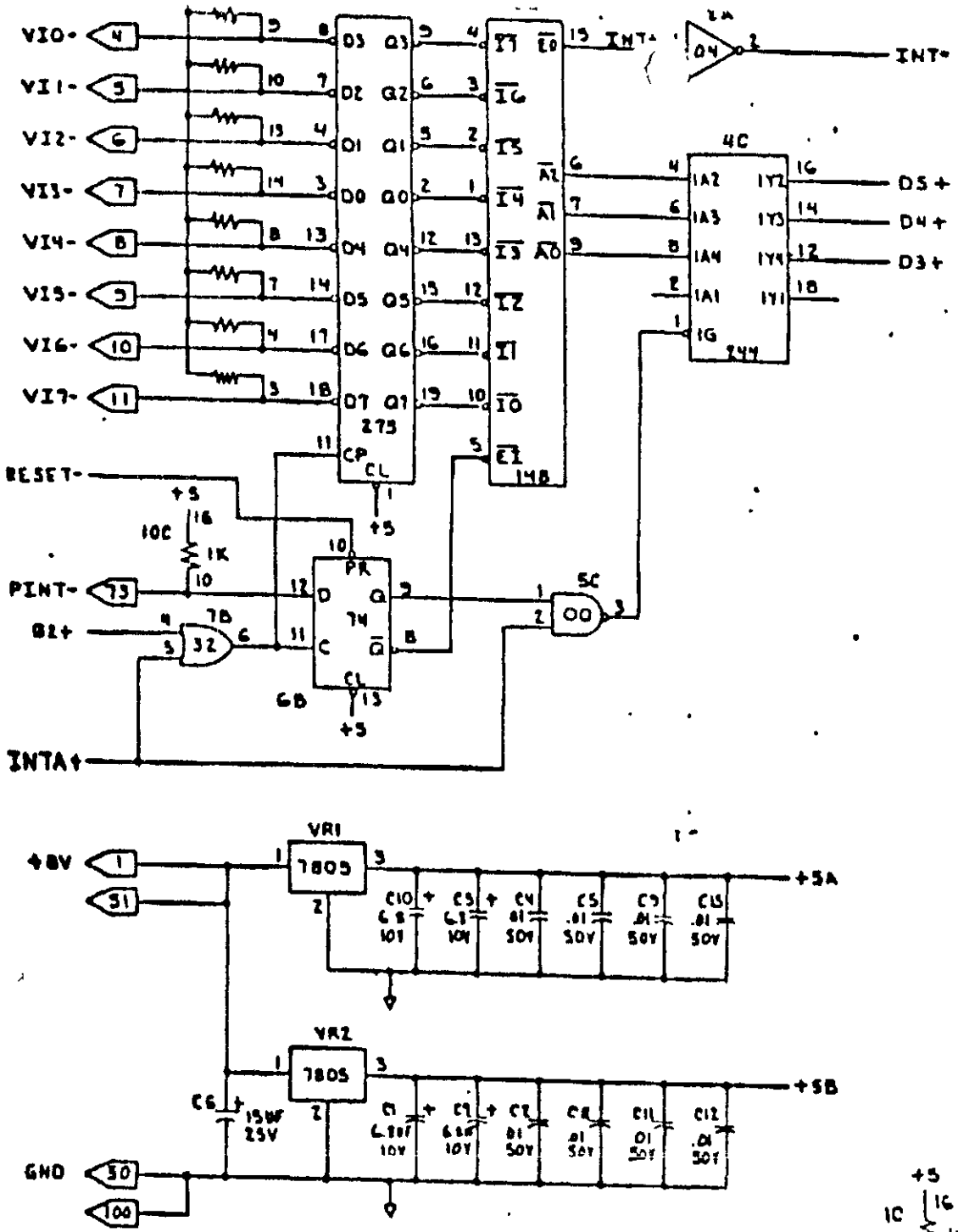
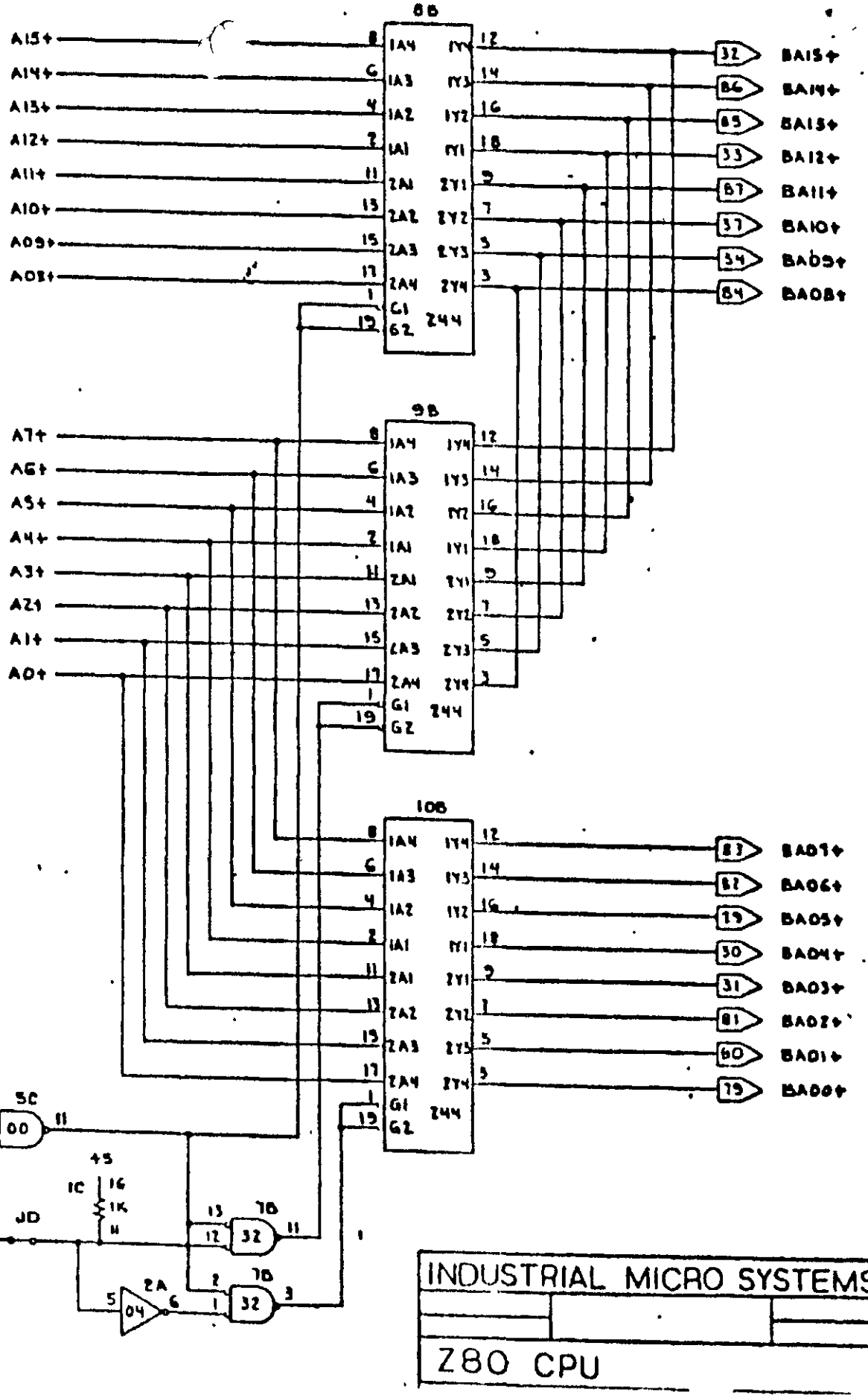
Z80 CPU		
L00450		



INDUSTRIAL MICRO SYSTEMS		
Z80 CPU		
L00450		3 OF 4





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Z80 CPU