MDS-800 INTELLEC® MDS MICROCOMPUTER DEVELOPMENT SYSTEM

Modular microcomputer development system for development and implementation of MCS™-80 and Series 3000 Microcomputer Systems

Intel 8080 microprocessor, with 2 μs cycle time and 78 instructions, controls all Intellec MDS functions.

16K bytes RAM memory expandable to 64K bytes.

2K bytes ROM memory expandable to 14K bytes.

Hardware interfaces and software drivers provided for TTY, CRT, line printer, high speed paper tape reader, high speed paper tape punch, and Universal PROM Programmer.

Universal bus structure with multiprocessor and DMA capabilities.

Eight level nested, maskable, priority interrupt system.

Optional PROM programmer peripheral capable of programming all Intel PROMs.

ICE (In-Circuit Emulator) options extend Intellec MDS diagnostic capabilities into user configured system allowing real time emulation of user processors.

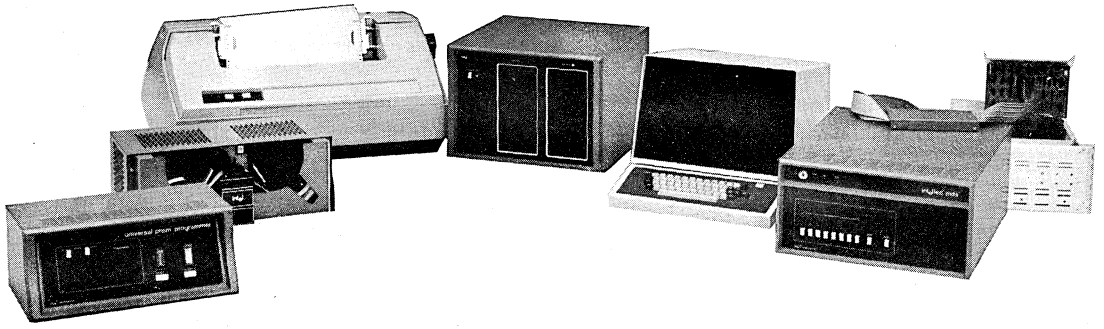
Optional I/O modules expandable in groups of four 8-bit input and output ports to a maximum of 88 ports (all TTL compatible).

ROM resident system monitor includes all necessary functions for program loading, debugging, and execution.

RAM resident macro assembler used to assemble all 8080 machine instructions with full macro and conditional assembly capabilities.

RAM resident text editor with powerful string search, substitution, insertion, and deletion commands.

The Intellec® MDS is a modular microcomputer development system containing all necessary hardware and software to develop and implement Intel MCS™-80 and Series 3000 microcomputer systems. The addition of MDS options and peripherals provides the user with a complete in-circuit microcomputer development system, supporting product design from program development through prototype debug, to production and field test.



INTELLEC® MDS HARDWARE

The standard Intellec® MDS consists of four microcomputer modules (CPU, 16K RAM Memory, Front Panel Control, and Monitor), an interconnecting printed circuit motherboard, power supplies, fans, a chassis, and a front panel. Modular expansion capability is provided by 14 additional sockets on the motherboard.

The CPU module uses Intel's powerful NMOS 8-bit 8080 microprocessor. The 8080's 2 μs cycle time, 78 instructions, unlimited subroutine nesting, vectored interrupt, and DMA capabilities are fully utilized by the Intellec MDS. Bus control logic resolves bus contention conflicts between the CPU module and other modules capable of acquiring control of the bus. The CPU module interfaces with a sixteen line address bus and a bidirectional eight line data bus. 8080 status signals are decoded and utilized for memory and I/O operations. An eight-level, nested interrupt priority system, complete with an interrupt priority push-down stack, resolves contention for 8080 interrupt servicing.

The RAM memory module contains 16K bytes of Intel 2107 dynamic RAM which operates at full processor speed. All necessary address decoding and refresh logic is contained on the module.

The front panel control module provides system initialization, priority arbitration, and real time clock functions. System initialization routines reside in a 256 byte, PROM resident, bootstrap loader. An eight-level priority arbitration network resolves bus contention requests among potential bus masters. A 1 ms interrupt request generator, which can be disabled under program control, provides real time clock functions. A 10 ms automatic time-out feature is also provided to force an interrupt request if nonexistent memory or I/O is addressed.

The Monitor module contains the Intellec MDS system monitor and all Intellec MDS peripheral interface hardware. The system monitor resides in a 2K byte Intel 8316 ROM. The module contains all necessary control and data transfer circuitry to interface with the following Intellec MDS peripherals:

- Teletype
- CRT
- High Speed Paper Tape Reader
- High Speed Paper Tape Punch
- PROM Programmer
- Line Printer

The Intellec MDS universal bus structure enables several CPU and DMA devices to share the bus by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure contains provisions for up to 16-bit address and data transfers and is not limited to any one Intel microcomputer family.

The Intellec MDS front panel is intended to augment the primary user interaction medium, the system console. The simplicity of the front panel coupled with the power of the system monitor provides an efficient user/Intellec interface. The front panel contains eight interrupt request switches with corresponding indicators, CPU RUN and HALT status indicators, a bootstrap loader switch, RESET switch, and a POWER ON switch and indicator.

The basic Intellec MDS capabilities may be significantly enhanced by the addition of the following optional features.

ICE (In-Circuit Emulator) extends Intellec MDS diagnositc capabilities into user configured systems. The Intellec MDS resident ICE processor operates in conjunction with the MDS host CPU and interfaces to the user system via an external cable. The ICE processor replaces the user system processor providing real time emulation capability. MDS resident memory and I/O may be substituted for equivalent user system elements, allowing the hardware designer to sequentially develop his system by integrating MDS and user system hardware. MDS display and debug hardware eliminate the need for specially constructed user system equivalents. Augmenting these capabilities are such powerful ICE debug functions as setting breakpoints, tracing program flow, single stepping, examining and altering CPU registers and memory locations.

The Universal PROM Programmer is an Intellec MDS peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, and 8708. Programming and verification operations are initiated from the Intellec MDS system console and are controlled by programs resident in the Intellec MDS and Universal PROM Programmer.

The addition of a single or dual drive Diskette Operating System significantly reduces program development time. An intelligent controller, constructed around Intel's powerful Series 3000 computing elements, provides diskette interface and control. Intel's software operating system (IDOS) in conjunction with the diskette operating system hardware provides a highly efficient and easy to use method of assembling, editing, and executing programs.

Customized user I/O requirements may be satisfied by adding I/O modules. Each I/O module contains four 8-bit input ports (latched or unlatched), four 8-bit latched output ports (with adjustable strobe pulses), and eight system interrupt lines. All inputs and outputs are TTL compatible. Optional I/O may be expanded to a maximum of 44 input and 44 output ports.

Memory may be expanded by adding RAM or PROM modules in user defined combinations. Up to 64K bytes of RAM may be added in 16K byte increments. PROM (Intel 8702A) may be added in 256 byte increments by adding PROM modules with socket capacity for 6K bytes and populating each module with the desired number of PROMs. Maximum PROM capacity is 12K bytes. RAM/PROM memory overlap is resolved by giving PROM priority.

DMA (direct memory access) modules work in conjunction with the Intellec MDS universal bus to maximize the efficiency of data transfers between MDS memory and selected I/O devices. Each module contains all the necessary control and data transfer logic to implement a complete DMA channel.

A ROM simulator composed of high speed bipolar RAM emulates Series 3000 bipolar microprogram ROM memory. Each ROM simulator module may be used in 512 X 16 or 1024 X 8 configurations.

INTELLEC® MDS SOFTWARE

Resident software provided with the Intellec® MDS includes the system monitor, 8080 macro assembler and text editor. Used together, these three programs simplify program preparation and speed the debugging task.

The system monitor provides complete control over operation of the Intellec MDS. All necessary functions for program loading and execution are provided. Additional commands provide extensive debug facilities and PROM programming functions. System peripherals may be dynamically assigned either via monitor commands or through calls to the system monitor's I/O subroutines.

Programs may be loaded from the reader device in either BNPF or hexadecimal format. Utility commands which aid in the execution and checkout of programs include:

- initialize memory to a constant
- move a block of memory to another location
- display memory
- modify RAM memory
- examine and modify CPU registers
- set breakpoints
- initiate execution at any given address
- perform hexadecimal arithmetic
- examine and modify the interrupt mask

The Intellec MDS System Monitor contains a powerful and easily expandable input/output system, which is built around four logical device types; console device, reader device, punch device and list device. Associated with each logical device may be any one of four physical devices. The user controls physical device assignment to each logical device through a System command.

Drivers are provided in the system monitor for the Universal PROM Programmer, ASR 33 teletype, high speed paper tape reader, high speed paper tape punch, line printer, and CRT. The user may write his own drivers for other peripheral devices and easily link them to the system monitor.

All system peripherals may be accessed simply by calling I/O subroutines in the system monitor. In addition, the user may dynamically reconfigure his system by monitor commands or by calling system subroutines which can assign a different physical device to each logical device. The user may also determine the current system peripheral configuration, check I/O status and determine the size of available memory.

The monitor is written in 8080 Assembly Language and resides in 2K bytes of ROM memory.

The Intellec MDS Resident Assembler translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation.

Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

The assembler performs its function in three passes. The first pass builds the symbol table. The second pass produces a source listing and provides error diagnostics. The third pass produces the object code. If the punch and list devices are separate (e.g. a high speed punch or printer is available) passes 2 and 3 may be combined into one pass.

Object code produced by the assembler is in hexadecimal format. It may be loaded directly into the Intellec MDS for execution and debugging or may be converted by the system monitor to BNPF format for ROM programming.

The assembler is written in PL/M[T.M.]-80, Intel's high level systems programming language. It occupies 12K bytes of RAM memory including space for over 800 symbols. The symbol table size may be expanded to a maximum of 6500 symbols by adding RAM memory. All I/O in the assembler is done through the system monitor, enabling the assembler to take advantage of the monitor's I/O system. The assembler is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec MDS.

The Intellec MDS editor is a comprehensive tool for the entry and correction of assembly language programs for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered directly from the console keyboard or from the system reader device. Text is stored internally in the editor's workspace, and may be edited with the following commands:

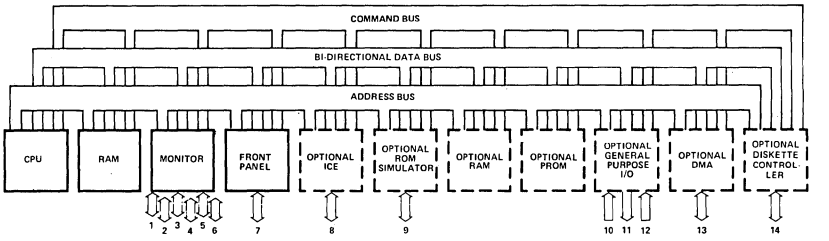
- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace may be listed to the system console or written to the system list or punch device for future use.

The text editor is written in PL/M[T.M.]-80. It occupies 8K bytes of RAM memory, including over 4500 bytes of workspace. The workspace may be expanded to a maximum of 58K bytes by adding RAM memory. All I/O in the editor is done through the system monitor, enabling the editor to take advantage of the monitor's I/O system. The editor is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec MDS.



NOTES:
1. PROM PROGRAMMER DATA/STATUS/COMMANDS
2. HIGH SPEED PUNCH DATA/STATUS/COMMANDS
3. HIGH SPEED READER DATA/STATUS/COMMANDS
4. PRINTER DATA/STATUS/COMMANDS
5. CRT DATA/STATUS/COMMANDS
6. TTY DATA/STATUS/COMMANDS
7. FRONT PANEL STATUS/SWITCH INPUTS
8. USER SYSTEM CPU OR MCU PIN SIGNALS
9. USER SYSTEM ROM PIN SIGNALS
10. EIGHT INTERRUPT LINES
11. FOUR 8-BIT OUTPUT PORTS
12. FOUR 8-BIT INPUT PORTS
13. DMA DEVICE DATA/STATUS/COMMANDS
14. DISKETTE DRIVE DATA/STATUS/COMMANDS

INTELLEC® MDS BLOCK DIAGRAM

HARDWARE SPECIFICATIONS

WORD SIZE
Host Processor (Intel 8080)
- Data: 8 bits
- Instruction, 8, 16, or 24 bits

MEMORY SIZE
RAM: 16K bytes expandable to 64K bytes using optional modules.

ROM: 2K bytes expandable to 14K bytes in 256 byte increments using optional PROM modules.

PROM: 256 bytes expandable to 12K bytes using optional modules.

Total: RAM, ROM and PROM may be combined in user defined configurations up to a maximum of 64K bytes.

MACHINE CYCLE TIME
Host Processor (Intel 8080): 2.0 μS

BUS TRANSFER RATE
Maximum bus transfer rate of 5 MHz.

SYSTEM CLOCKS
Host Processor (Intel 8080) Clock: Crystal controlled at 2 MHz ±0.1%.

Bus Clock: Crystal controlled at 9.8304 MHz ±0.1%.

I/O INTERFACES
CRT:
- Baud Rates: 110/300/600/1200/2400/4800/9600 (selectable).
- Code Format: 7–12 level code (programmable).
- Parity: Odd/even (programmable).
- Interface: TTL/RS232C (selectable).

TTY:
- Baud Rate: 110
- Code Format:
  - Input: 10 level or greater.
  - Output: 11 level.
  - Parity: Odd.
  - Interface: 20 mA current loop.

High Speed Paper Tape Reader:
- Transfer Rate: 200 cps.
- Control: 2-bit output. 1-bit input.
- Data: 8-bit byte
- Interface: TTL

Punch:
- Transfer Rate: 75 cps
- Control: 2-bit output 1-bit input
- Data: 8-bit byte
- Interface: TTL

Printer:
- Transfer Rate: 165 cps
- Control: 2-bit status input 1-bit output
- Data: ASCII
- Interface: TTL

PROM Programmer:
- Control: 3 strobes for multiplexed output data.
- Data: 8-bit bidirectional
- Interface: TTL

GENERAL PURPOSE I/O (OPTIONAL)
Input Ports: 8-bit TTL compatible (latched or unlatched); expandable in 4 port increments to 44 input ports.

Output Ports: 8-bit TTL compatible (latched); expandable in 4 port increments to 44.

Interrupts: 8 TTL compatible interrupt lines.

INTERRUPT
8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

DIRECT MEMORY ACCESS
Standard capability on Intellec bus; implemented for user selected DMA devices through optional DMA module – maximum transfer rate of 2 MHz.

MEMORY ACCESS TIME
RAM: 450 ns
PROM: 1.3 μs using Intel 8708A PROM.

PHYSICAL CHARACTERISTICS
Dimensions: 8.5" X 19" X 17"
21.6 cm X 48.3 cm X 43.2 cm
Weight: 65 lb (29.5 kg)

ELECTRICAL CHARACTERISTICS

DC POWER SUPPLY (Volts)	POWER SUPPLY CURRENT (Amps)	BASIC SYSTEM CURRENT REQUIREMENTS (Amps)	
		Maximum	Typical
+ 5 ±5%	35.0	9.0	6.6
+12 ±5%	3.0	0.7	0.4
–10 ±5%	3.0	0.2	0.2
–12 ±5%	0.5	––	––

AC POWER REQUIREMENTS
50–60 Hz; 115/230 VAC; 150 Watts

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0 to 55°C

SOFTWARE SPECIFICATIONS

CAPABILITIES

System Monitor:

Devices supported include:

- ASR 33 teletype
- Intel high speed paper tape reader
- Paper tape punch
- CRT
- Printer
- Universal PROM programmer
- 4 logical devices recognized
- 16 physical devices maximum allowed

Macro Assembler:

800 symbols in standard system; automatically expandable with additional RAM memory to 6500 symbols maximum.

Assembles all seventy-eight 8080 machine instructions plus 10 pseudo-operators.

Text Editor:

12K bytes of workspace in standard system; automatically expandable with additional RAM memory to 58K bytes.

OPERATIONAL ENVIRONMENTAL

System Monitor:

Required hardware:

- Intellec MDS
- 331 bytes RAM memory
- 2K bytes ROM memory
- System console

Macro Assembler:

Required hardware:

- Intellec MDS
- 12K bytes RAM memory
- System console
- Reader device
- Punch device
- List device

Required software:

- System monitor

Text Editor:

Required hardware:

- Intellec MDS
- 8K bytes RAM memory
- System console
- Reader device
- Punch device

Required software:

- System monitor

Tape Format:

Hexadecimal object format.

MDS OPTIONS

MDS-016	16K Dynamic RAM
MDS-406	6K PROM (sockets and logic)
MDS-501	DMA Channel Controller
MDS-504	General Purpose I/O Module
MDS-600	Prototype Module
MDS-610	Extender Module
MDS-620	Rack Mounting Kit

MDS EMULATORS/SIMULATOR

MDS-ICE-30	3001 In-Circuit Emulator
MDS-ICE-80	8080 In-Circuit Emulator
MDS-SIM-100	Bipolar ROM Simulator

MDS PERIPHERALS

MDS-UPP	Universal PROM Programmer
MDS-PTR	High Speed Paper Tape Reader
MDS-DOS	Diskette Operating System

MDS INTERFACE CABLES/CONNECTORS

MDS-900	CRT Interface Cable
MDS-910	Line Printer Interface Cable
MDS-915	High Speed Reader Interface Cable
MDS-920	High Speed Punch Interface Cable
MDS-930	Peripheral Extension Cable
MDS-940	DMA Cable
MDS-950	General Purpose I/O Cable
MDS-960	25-pin Connector Pair
MDS-970	37-pin Connector Pair
MDS-980	60-pin Motherboard Auxiliary Connector
MDS-985	86-pin Motherboard Main Connector
MDS-990	100-pin Connector Hood

EQUIPMENT SUPPLIED

Central Processor Module
RAM Memory Module
Monitor Module (System I/O)
Front Panel Control Module
Chassis with Motherboard
Power Supplies
Finished Cabinet
Front Panel
ROM Resident System Monitor
RAM Resident Macro Assembler
RAM Resident Text Editor
Hardware Reference Manual
Reference Schematics
Operator's Manual
8080 Assembly Language Programming Manual
System Monitor Source Listing
8080 Assembly Language Reference Card
TTY Cable
European AC Adapter
AC Cord