NCR

Personal Computer

Pc8

Technical Reference

First Edition, July 1985

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YOUR NCR PERSONAL COMPUTER PC8 AND THIS MANUAL

Your NCR PERSONAL COMPUTER PC8 is a powerful business/professional personal computer. It is designed to act not only as an independent, self-sufficient system, but also as a control center for systems fulfilling a wide range of business, scientific and technological requirements.

Essential electronics are contained on the controller board. Where possible, LSI components have been used, providing compactness and a high degree of reliability. The microprocessor is the powerful and versatile 80286, which can be supplemented by the 80287 co-processor, if required. With the additional support of Direct Memory Access, high processing speeds can be achieved. 256 Kilobyte of random access memory are included in the standard version, over and above video RAM.

Also included on the main board is a real-time clock integrated circuit. A battery ensures that time continues to be registered, even after the computer has been switched off. Battery powered CMOS RAM also stores basic information concerning the disk and memory configuration of your system.

Full access to the system bus is available at the expansion card assembly. In addition to display and disk controller boards, this assembly can accomodate up to six cards to expand the features of your system.

The NCR PERSONAL COMPUTER PC8 is operationally compatible with a number of other widely used personal computers. This provides for portability of a large number of software applications and hardware extensions between your NCR PERSONAL COMPUTER PC8 and other personal computers you may have occasion to use.

This Manual is intended for designers, system integrators, and programmers who require detailed information about the construction and operation of the NCR PERSONAL COMPUTER PC8. Information is included about the I/O bus, signal levels and timing, power requirements, and pin assignments. In addition, details are given about low-level software control of hardware functions.

With the help of the information contained in this Manual, you may be intending to make hardware or software changes to the NCR PERSONAL COMPUTER PC8 for specialized use. Because of the complex nature of computer technology, we must stress that NCR cannot accept responsibility for problems arising from such changes. At the same time, we are constantly endeavouring to maintain the quality of information provided in this Technical Reference Manual. Therefore, if you find that there is a particular aspect of information not already provided in this Manual, or if you want to let us know how useful you find it, please ask your supplier to forward your comments to us.

NCR PERSONAL COMPUTER PC8

TECHNICAL REFERENCE MANUAL

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MODELS AND OPTIONS

The NCR PERSONAL COMPUTER consists of the main unit and the keyboard. The computer is available in different models, and has a variety of options that can be added to each model. Expansion boards from non-NCR ("third party") manufacturers can be used with the NCR PERSONAL COMPUTER, as well as expansion boards offered by NCR.

The standard unit is made up of the following parts:

* Cabinet
* Power supply
* 1.2 MB flexible disk drive with or without a hard disk drive
* Main Processor Board with:
  - 80286 Microprocessor
  - 256 KB Random Access Memory (RAM)
  - 64 bytes battery maintained CMOS RAM holding time/date and equipment status
  - 32 KB Read Only Memory (ROM)
  - PROM containing unique system unit identification (for software protection)
  - Plug-in board option expansion slots (6 full bus access, 2 limited bus access)
  - Disk drive controller plug in board, occupying one of the full bus access slots

SYSTEM OVERVIEW

To make up a complete system a display controller board must be installed in one of the limited bus access slots and a display unit connected.

The most extensive configurations of magnetic storage media which can be accomodated in the main unit:

* 1 flexible disk drive
  2 full-height or 2 half-height hard disk drives

* 2 flexible disk drives (second drive 1.2 MB or 360 KB)
  1 full-height or 2 half-height hard disk drives
  1 multi-mode tape

* 2 flexible disk drives (second drive 1.2 MB or 360 KB)
  1 full-height hard disk drive
  1 half-height hard disk drive

The disk controller board included in the main unit can support a maximum configuration of two flexible and two hard disk drives. The multi-mode tape requires a separate controller.

MODEL IDENTIFICATION

The model number is shown on the plate at the back of the unit:

```
3279 - XX XX - XX XX
 |     |  |    |  |
 |     |  |    |  |____ Language
 |     |  |    |_______ Voltage/Frequency
 |     |  |____________ Sub Model
 |     |_______________ Major Model
 |_____________________ Class
```

Class	3279		]
Major Model	01	256 KB Memory	]
	02	512 KB Memory	]
Sub Model	01	1.2 MB Flexible Disk	]
	02	1.2 MB Flex + 20MB Hard Disk + Ser./Par. Board	]
Voltage/ Frequency	80	100 to 127 Volts/ 200 to 240 Volts (switchable)	]
Language	00	US English	]
	01	International English	]
	02	UK English	]
	03	Spanish	]
	05	French	]
	06	German	]
	09	Swedish	]
	10	Danish	]
	11	Norwegian	]
	12	Italian	]
	20	Finnish	]

SYSTEM COMPONENTS

This section introduces elements of the NCR PERSONAL COMPUTER shared by all models. Figure 1.1 provides an easy-to-follow diagram illustrating the most important components on the main processor board and those external functions with which the main processor board interfaces.

The CLOCK is the key to co-ordination of the entire system. This unit consists of a crystal supplying a signal of frequency 16 MHz to a Clock Controller. The 88284 Clock Controller divides the frequency of this input signal, in order to provide a suitable timing signal (8 MHz) for the main system microprocessor (CPU), as well as timing signals for other system components.

The TIMER is an integrated circuit which can be programmmed to produce a variety of signals at various intervals. Accuracy is ensured by the Timer deriving its synchronizing signals, by way of suitable frequency division, from the system Clock. You can use the Timer for programmed interval timing. In addition, the Timer can be used to provide the frequencies required if you wish to play music on the computer. The Timer is also used for refreshing random access memory (see below).

The Central Processing Unit (CPU), often simply called "microprocessor", is widely acknowledged as the most "influential" of the integrated circuits. It is the CPU which passes on instructions supplied by you, the programmer, to the other units in the system. Optionally, the CPU can be supported by the 80287 Co-Processor. The Co-Processor is capable of performing, in response to simple instructions, floating-point calculations which would otherwise require extensive programming of the CPU.

The NCR PERSONAL COMPUTER makes use of two types of memory: read only memory (ROM), and a large random access memory (RAM) of at least 256 KB. Read only memory contains instructions for the CPU which enable the latter to get the system started, as well as a "library" of short, but useful, programs known under the collective term BIOS (Basic Input/Output System). It is the task of the BIOS to constantly maintain communication between the CPU and the other system units.

Random access memory can likewise contain program instructions for the CPU, but it is also used for storing data being processed by the the program. The random access memory of your NCR PERSONAL COMPUTER is "dynamic", which means that its contents can be changed very quickly, thus providing for fast processing. This also means that memory must be "refreshed" at fixed intervals, to prevent its contents from disappearing. Fortunately, you need not normally be concerned about providing refresh cycles, as this is taken care of by the Timer.

The Direct Memory Access (DMA) Controllers are used for the transfer of large blocks of data to and from memory. DMA is particularly useful for reading data from or writing data to flexible disk. The CPU does not then have to specify a memory address for each byte read or written. Instead, all the CPU has to tell the DMA Controller is 1) that data is to be transferred between memory and flexible disk, 2) the address of the first byte in memory to be accessed, and 3) the number of bytes to be transferred.

The I/O CONTROLLER is used for bi-directional communication with the keyboard. In addition, it keeps a note of the settings of system configuration switches, so that programs can detect the NCR PERSONAL COMPUTER model being used.

The INTERRUPT CONTROLLERS provide fast notification of the CPU in the event that a system unit requires urgent attention. This is especially important for the Timer and keyboard: the Timer, because an accurate clock (whether your own or provided by the operating system) must not miscount the number of ticks; the keyboard, because this is the most expedient way for the user to intervene during execution of a program.

64 bytes of battery-maintained CMOS RAM are used for the encoding of a number of system characteristics (memory, disk drives) as well as an accurate clock and calendar.

Additional equipment can be interfaced via one or more of the system bus I/O connectors inside the computer cabinet.

The system BUS provides the lines by which communication between the units of the system can take place. The bus really consists of three busses. The address bus conveys memory or I/O map addresses by which memory bytes or external devices can be accessed. Data is passed as parallel signals on the data bus. Control bus is a collective term for those signals which otherwise influence data flow within the system, for example, signals which determine whether the direction of data flow is read or write, and whether transfer is to/from memory or an I/O device. Your NCR PERSONAL COMPUTER includes a BUS CONTROLLER which relieves the CPU of such bus arbitration duties.

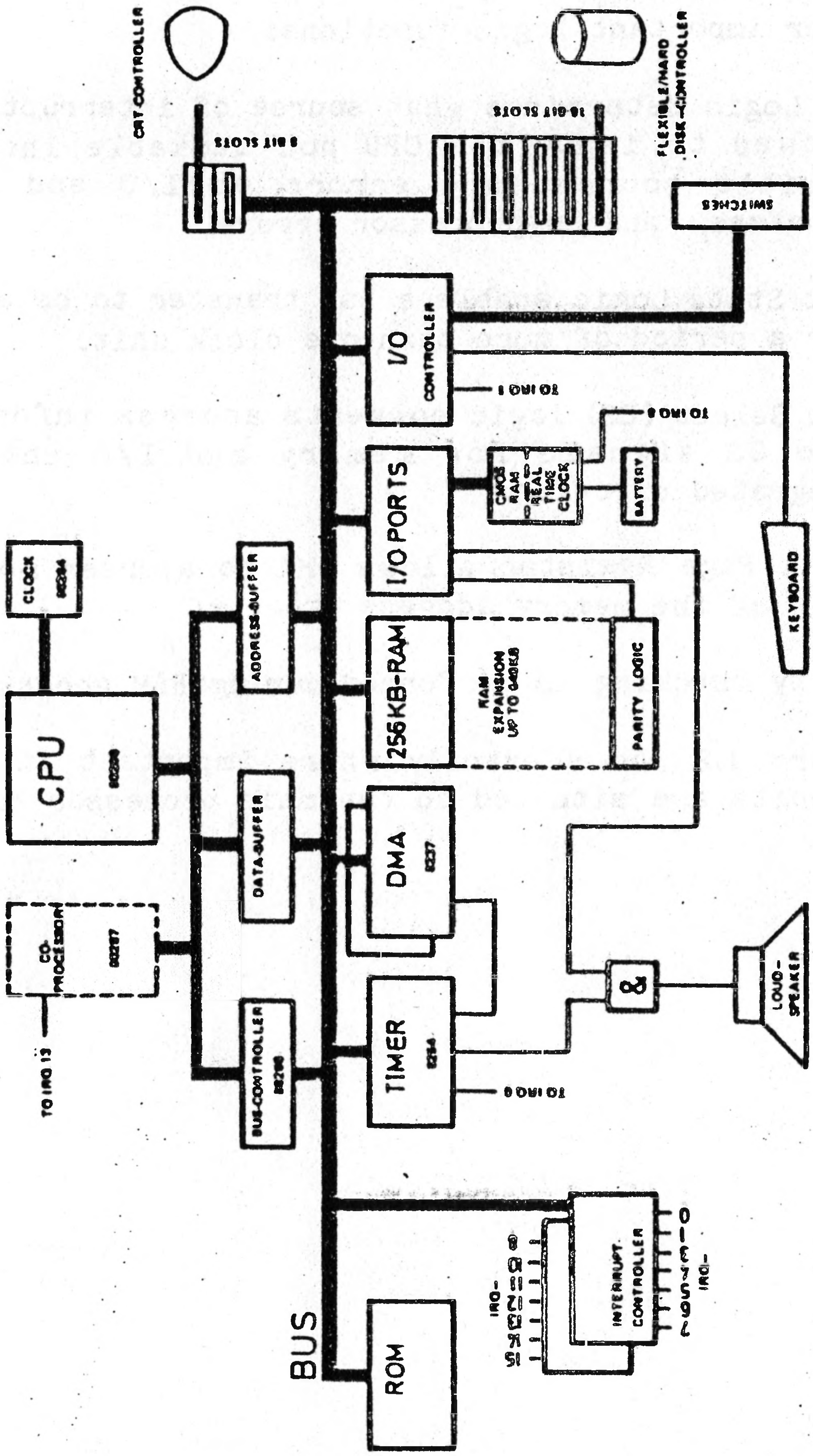


Figure 1.1 System overview

Other important logic functions:

NMI Logic determines what source of interrupt may be allowed to issue the CPU non-maskable interrupt. Possible sources are errors on I/O and memory transfers, and co-processor errors.

Wait State Logic enable a bus transfer to be executed over a period of more than one clock unit.

Chip Select (CS) logic converts address information into CS signals for memory and I/O interface integrated circuits.

A DMA Page Register allows DMA to address more than 64 KB of the memory address area.

Parity checking is performed during RAM access.

Figure 1.2 shows exactly where important integrated circuits are situated on the main processor board.

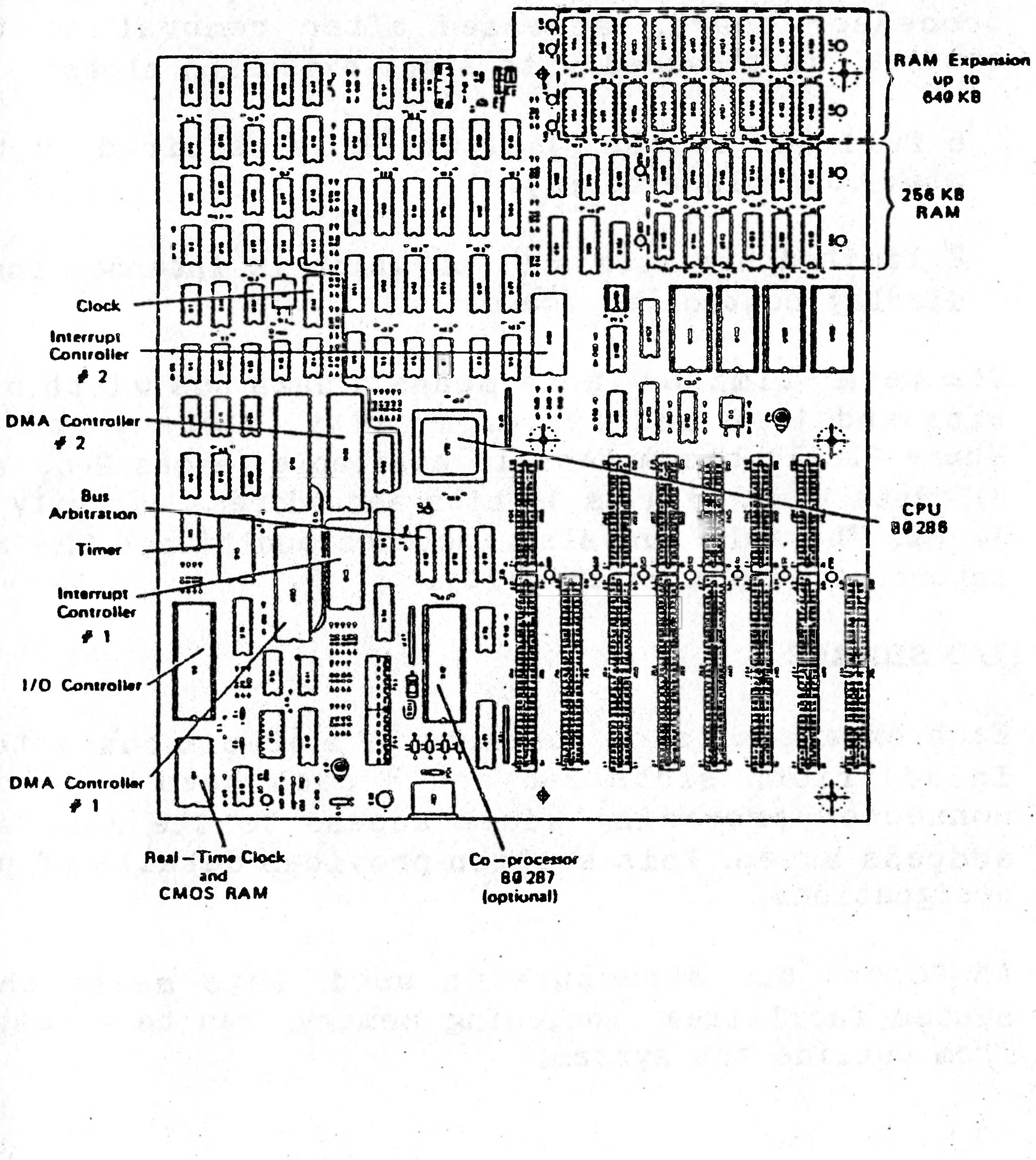


Figure 1.2 Main processor board IC locations

SYSTEM CONNECTION

The NCR PERSONAL COMPUTER can accomodate up to eight expansion boards (including the disk control and display control boards). For this purpose, the main processor board, accessed after removal of the cabinet, is provided with eight expansion slots:

6 full bus access (1 of which is required by the disk controller board)

2 limited bus access (1 of which is intended for a display controller board)

The term "limited" here means a data bus width of 8 bits and 1 MB address capability (slots 1 and 7). Where "full" bus access is available (slots 2-6, and 8), data bus width is 16 bits and address capacity is 16 MB. The full bus also includes additional DMA and interrupt detection capacity.

I/O SIGNALS

Each expansion slot consists of a 62-pin connector. In addition, slots 2-8 and 8 each have a 36-pin connector providing wider access to the data and address buses. This section provides details of pin designations.

An "open" bus structure is used. This means that system facilities, including memory, can be accessed from outside the system.

B		A	
1	GND	1	I/O CH CHK/
2	RESET DRV	2	SD7
3	+ 5V	3	SD6
4	IRQ9	4	SD5
5	- 5V	5	SD4
6	DRQ2	6	SD3
7	- 12V	7	SD2
8	OWS	8	SD1
9	+ 12V	9	SD0
10	GND	10	I/O CH RDY/
11	SMEMW/	11	AEN
12	SMEMR/	12	SA19
13	IOW/	13	SA18
14	IOR/	14	SA17
15	DACK3/	15	SA16
16	DRQ3	16	SA15
17	DACK1/	17	SA14
18	DRQ1	18	SA13
19	REFRESH/	19	SA12
20	CLK	20	SA11
21	IRQ7	21	SA10
22	IRQ6	22	SA9
23	IRQ5	23	SA8
24	IRQ4	24	SA7
25	IRQ3	25	SA6
26	DACK2/	26	SA5
27	T/C	27	SA4
28	BALE	28	SA3
29	+ 5V	29	SA2
30	OSC	30	SA1
31	GND	31	SA0

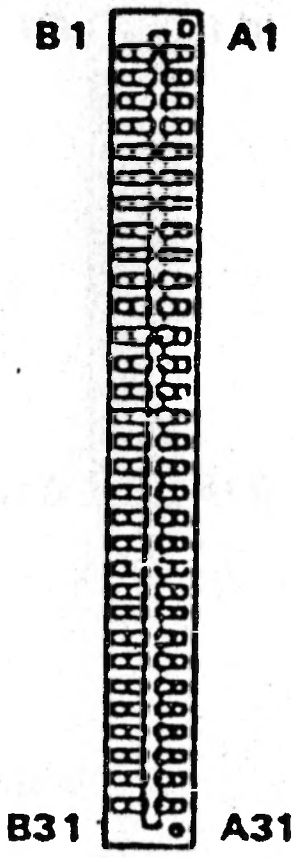


Figure 1.3 System bus pin designations (limited bus)

D		C	
1	MEM CS16/	1	SBHE
2	I/O CS16/	2	LA23
3	IRQ10	3	LA22
4	IRQ11	4	LA21
5	IRQ12	5	LA20
6	IRQ13	6	LA19
7	IRQ14	7	LA18
8	DACK0/	8	LA17
9	DRQ0	9	MEMR/
10	DACK5/	10	MEMW/
11	DRQ5	11	SD8
12	DACK6/	12	SD9
13	DRQ6	13	SD10
14	DACK7/	14	SD11
15	DRQ7	15	SD12
16	+ 5V	16	SD13
17	MASTER/	17	SD14
18	GND	18	SD15

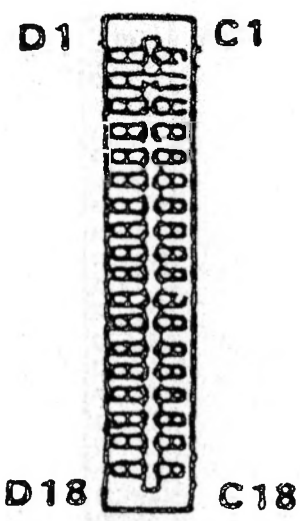


Figure 1.4 System bus pin designations (extension to full bus)

The following signals are provided for at all eight slots.

RESET DRV Output
This signal is issued in response to a system reset.

BALE Output
Provided by the 82288 bus arbitration IC to latch addresses from the CPU (BALE falling edge). When used with AEN, the address is for DMA (BALE is active during DMA cycles).

AEN Output
This signal is used by the DMA Controller to indicate that it is in control of the address and data busses, as well as the MEMW/, MEMR/, IOW/, and IOR/ lines.

This bus reservation is especially important, as the DMA Controller needs the data bus for the 8 most significant bits of the RAM address to be accessed.

SA0 - SA19
Address lines for a memory and I/O address space of 1 MB.

SD0 - SD7
Data lines for 8-bit transfers.

IRQ3-IRQ7, IRQ9 Input
Input signals to the Interrupt Request Register of the 8259A Programmable Interrupt Controller. The signal must remain high until the interrupt is acknowledged by the microprocessor.

DRQ1-DRQ3 Input
DMA request lines to the 8237 DMA Controller for 8-bit transfers. These lines can be programmed at the DMA Controller to active low or active high.

DACK1-DACK3 Output
DMA request acknowledge lines. These lines can be programmed at the DMA Controller to active low or active high (the BIOS software specifies active low).

SMEMW/ Output
Determines that data on the data bus is for writing to a selected address in random access memory. This signal is asserted by /MEMW, provided that the address decodes to the lowest 1 MB of CPU address space.

SMEMR/ Output
Determines that RAM data from a selected address is to be placed on the data bus. This signal is asserted by /MEMR, provided that the address decodes to the lowest 1 MB of CPU address space.

IOW/ Input-Output
Determines that the data on the bus is for reading by a device. This signal can be asserted by CPU or DMA controller.

IOR/ Input-Output
Instructs a device to read data from the bus. This signal can be asserted by CPU or DMA controller.

TC Output
The Terminal Count signal supplied by the DMA Controller when the programmed number of bytes has been transferred.

IO CH RDY Input
This signal is normally high. It can be pulled low by a device which requires more than one machine cycle for the transfer of data.

IO CH CHK/ Input
This signal active indicates an I/O or RAM parity error.

OSC Output
The system crystal oscillator signal of frequency 14.31818 MHz. This signal has equal high and low periods. Note that this signal is not synchronous with the system clock.

CLK Output
A 50% duty cycle frequency of 8 MHz for CPU clocking purposes. Where a frequency output is required, use shoud be mane of the system bus OSCillator connection.

OWS/ Input
When this signal is low, the CPU understands that the current bus cycle can be completed without intervention of additional Wait cycles. The signal is derived from an address decoding gated with a 16-bit I/O read or write instruction, where no Wait cycles are required. For 8-bit I/O operations requiring a minimum of two Wait states, the signal should be driven active one system clock following the active gating of the read/write instruction with the device address decode.

REFRESH/ Input/Output
This signal indicates that a memory refresh cycle is taking place, but it can also be provided externally to instigate a refresh cycle.

The following signals are provided for by the 36-pin full bus extension.

LA17 - LA23
This is the address bus extension, allowing up to 16 MB to be mapped. These signals are valid when BALE is high. They are not latched during CPU cycles

SD8 - SD15
The eight MSBs of the full 16-bit data bus.

MASTER/ Input
After a DMA request has been acknowledged, an external device can assert this signal in order to take over the system bus. However, memory refresh is inhibited during this time.

SBHE Input/Output
Indicates or enables a transfer of data on the 8 MSBs of the data bus.

MEM CS16/ Input
Decoded from LA17-LA23, this signal gives notification of a 16-bit memory cycle (requiring one Wait state).

IO CS16/ Input
An address decoding provides this signal which gives notification of a 16-bit I/O cycle (requiring one Wait state).

MEMW/ Input/Output

Indicates that data for memory storage is on the data bus. This signal can be issued by the CPU or DMA controller, or can be accepted from an external source.

MEMR/ Input/Output
Instructs memory to place data on the data bus. This signal can be issued by the CPU or DMA controller, or can be accepted from an external source.

IRQ10 - IRQ14 Input
Input signals to the Interrupt Request Register of the 8259A Programmable Interrupt Controller. The signal must remain high until the interrupt is acknowledged by the microprocessor.

DRQ0, DRQ5 - DRQ7 Input
DMA request lines to the 8237 DMA Controller for 16-bit transfers. These lines can be programmed at the DMA Controller to active low or active high.

DACK0, DACK5 - DACK7 Output
DMA request acknowledge lines. These lines can be programmed at the DMA Controller to active low or active high (the BIOS software specifies active low).

CONFIGURATION SWITCHES

The main processor board includes three groups of configuration switches (jumpers) which require setting as illustrated in Figure 1.5, before the computer is used for the first time, and after any of the hardware features concerned has been changed.

The ROM type selector jumper block has the following significance:

Pins Connected	Address Selection	ROM Selection
1 - 8 2 - 7	+ 5 vdc to ROM pin 27 A15 to ROM SEL decoder	16 KB
3 - 6 4 - 5	A15 to ROM pin 27 A16 to ROM SEL decoder	32 KB

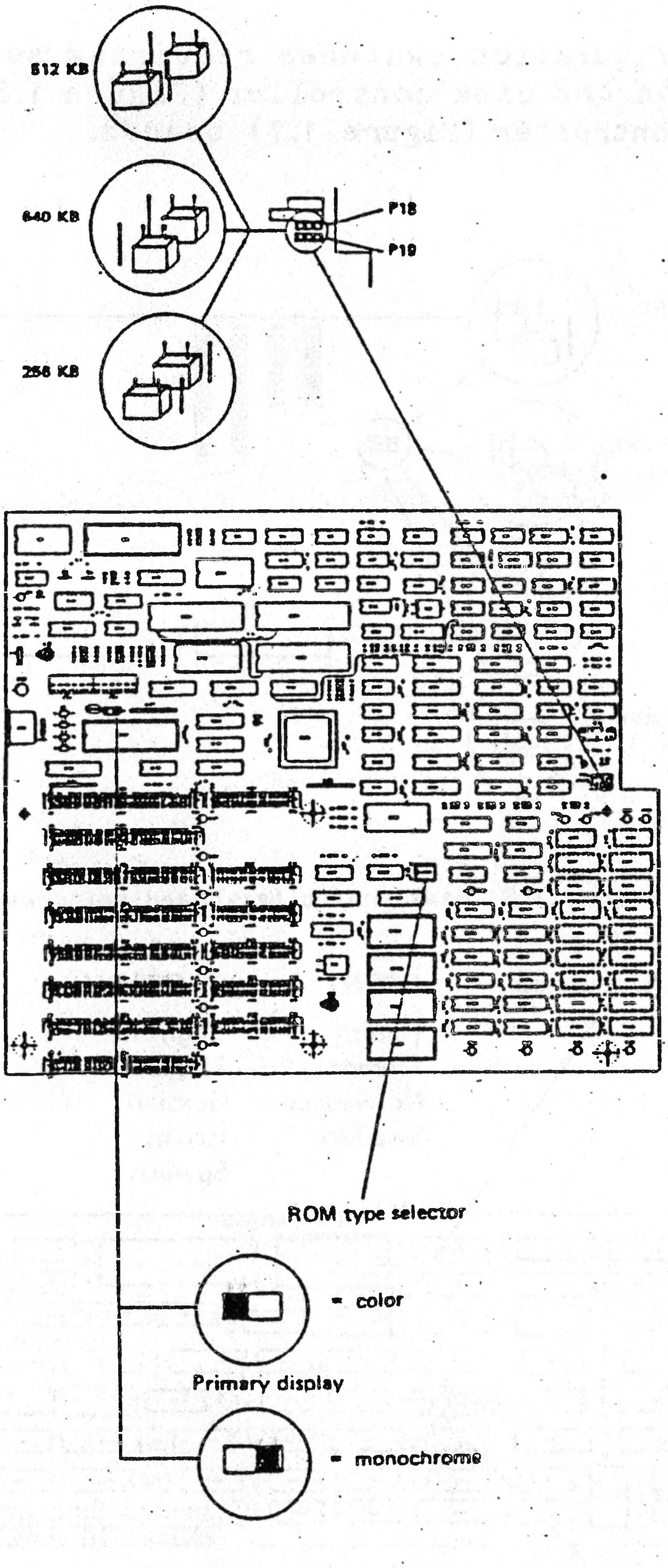


Figure 1.5 Main processor board switches

Other configuration switches requiring setting are present on the disk controller (Figure 1.6) and the display controller (Figure 1.7) boards.

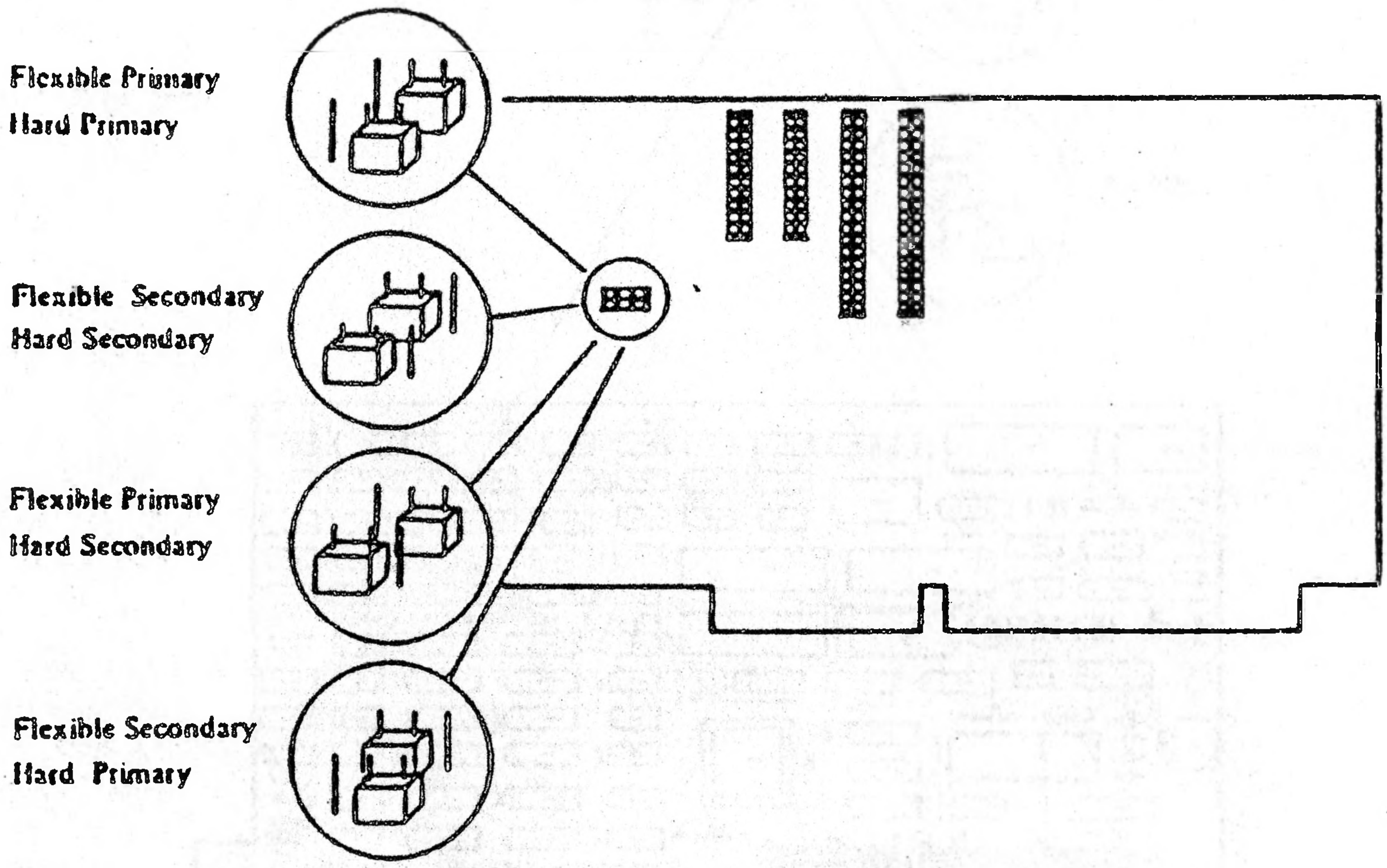


Figure 1.6 Disk controller board switches

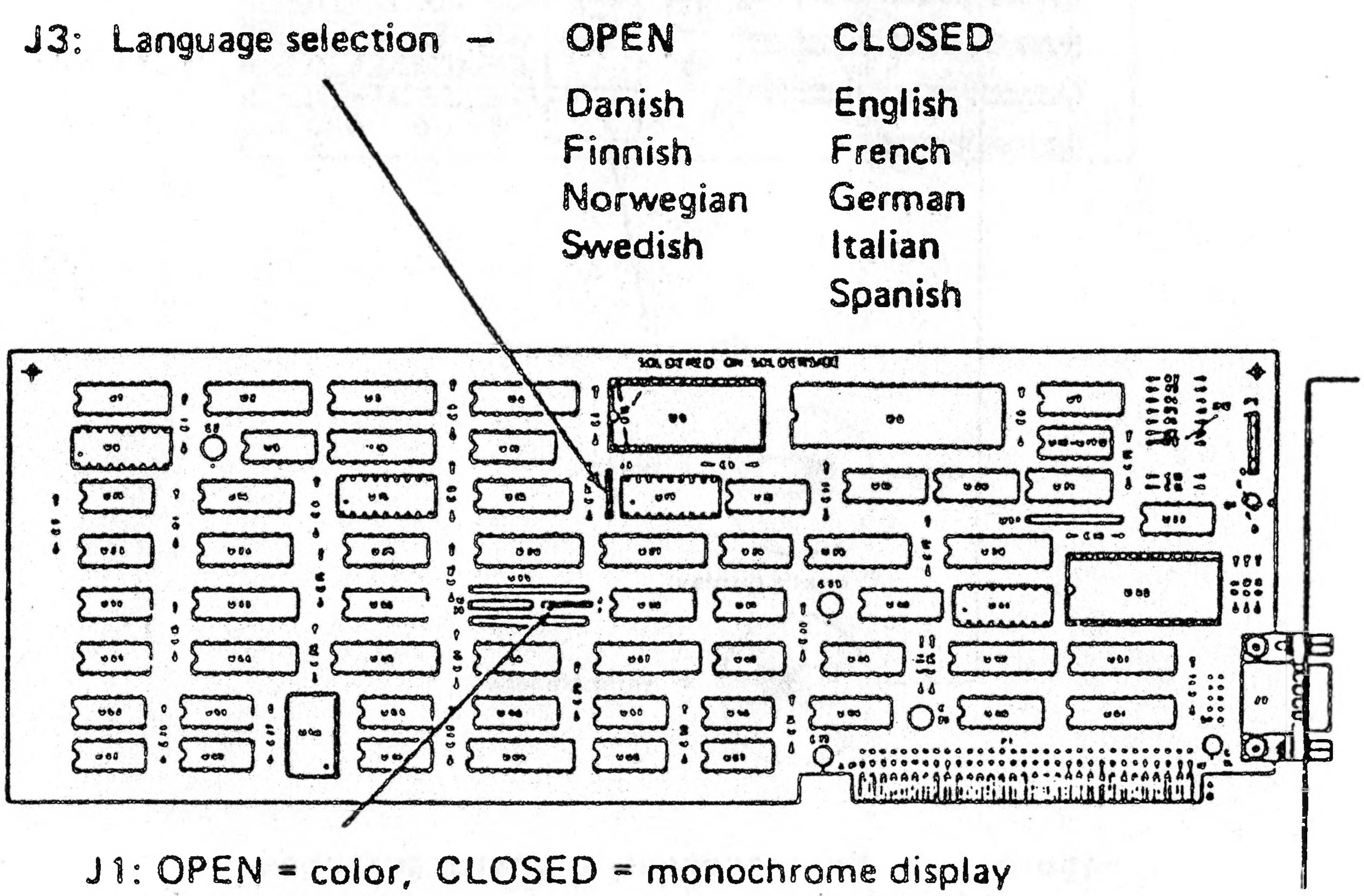


Figure 1.7 Display controller board switches

MEMORY EXPANSION

The NCR PERSONAL COMPUTER is supplied with 256 KB random access memory on the main processor board. This memory occupies the lowermost CPU addresses. Memory can be upgraded to 512 KB (address 7FFFFH) or 640 KB (address 9FFFFH). Memory expansion beyond 640 KB requires the installation of a separate memory board.

Memory expansion Kit 3299-K110 contains integrated circuits for 128 KB. When installing these on the main processor board, the sockets must be populated as shown in Figure 1.8, and the appropriate main processor board configuration switches set (see previous section).

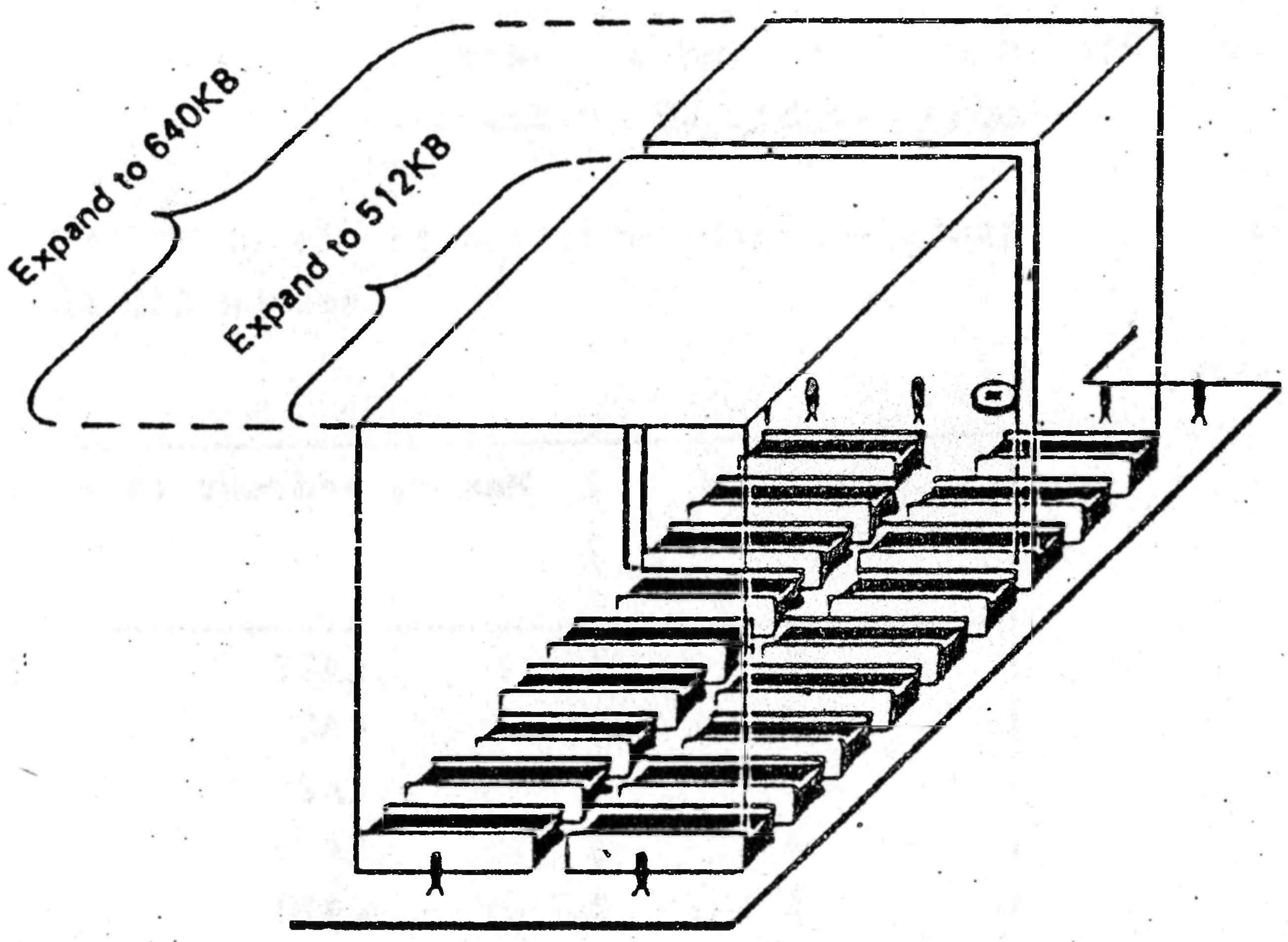
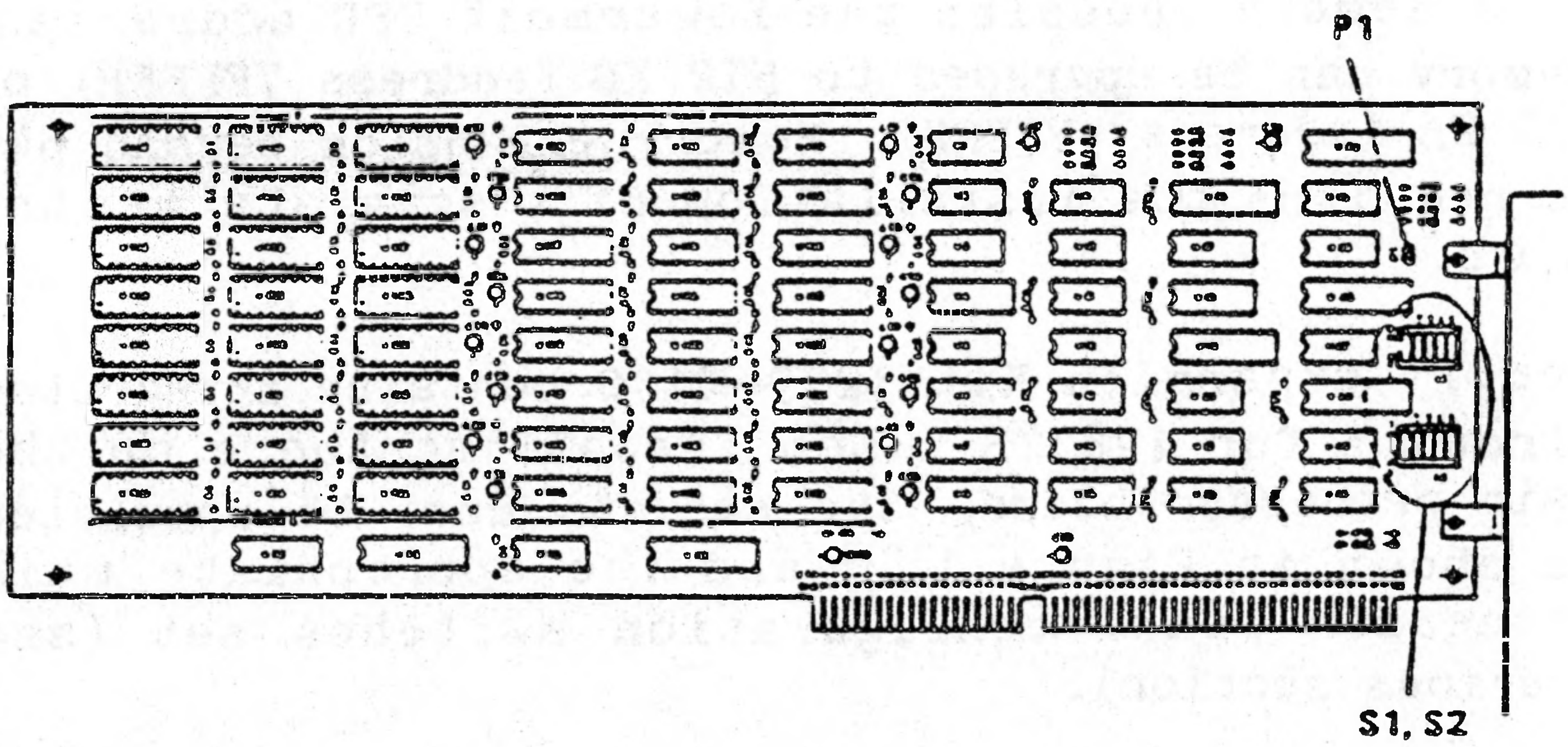


Figure 1.8 Main processor board memory expansion

Configuration switches on any memory expansion board (s) installed (3299-K111, 3299-K112) must be set to reflect the amount of memory on the memory expansion board and the start address(es) of the memory expansion (see Figure 1.9).



Jumper P1: closed for 1MB on board
open for 512 KB on board

S1: start address selection for first 512 KB
S2: second 512 KB

Switch on block S1/S2	Memory address line
1	LA23
2	LA22
3	LA21
4	LA20
5	LA19

Figure 1.9 Memory expansion board switches

It is possible to install more than one memory expansion boards, subject to availability of slots (full bus access), but address areas set by the switch blocks S1 and S2 must not overlap. It is also important to make sure that a starting address does not cause a clash of addresses with main processor board and display memory (lower CPU addresses) or Read Only Memory (higher CPU addresses).

THE MEMORY MAP

Figure 1.10 sets out the memory map of the NCR PERSONAL COMPUTER.

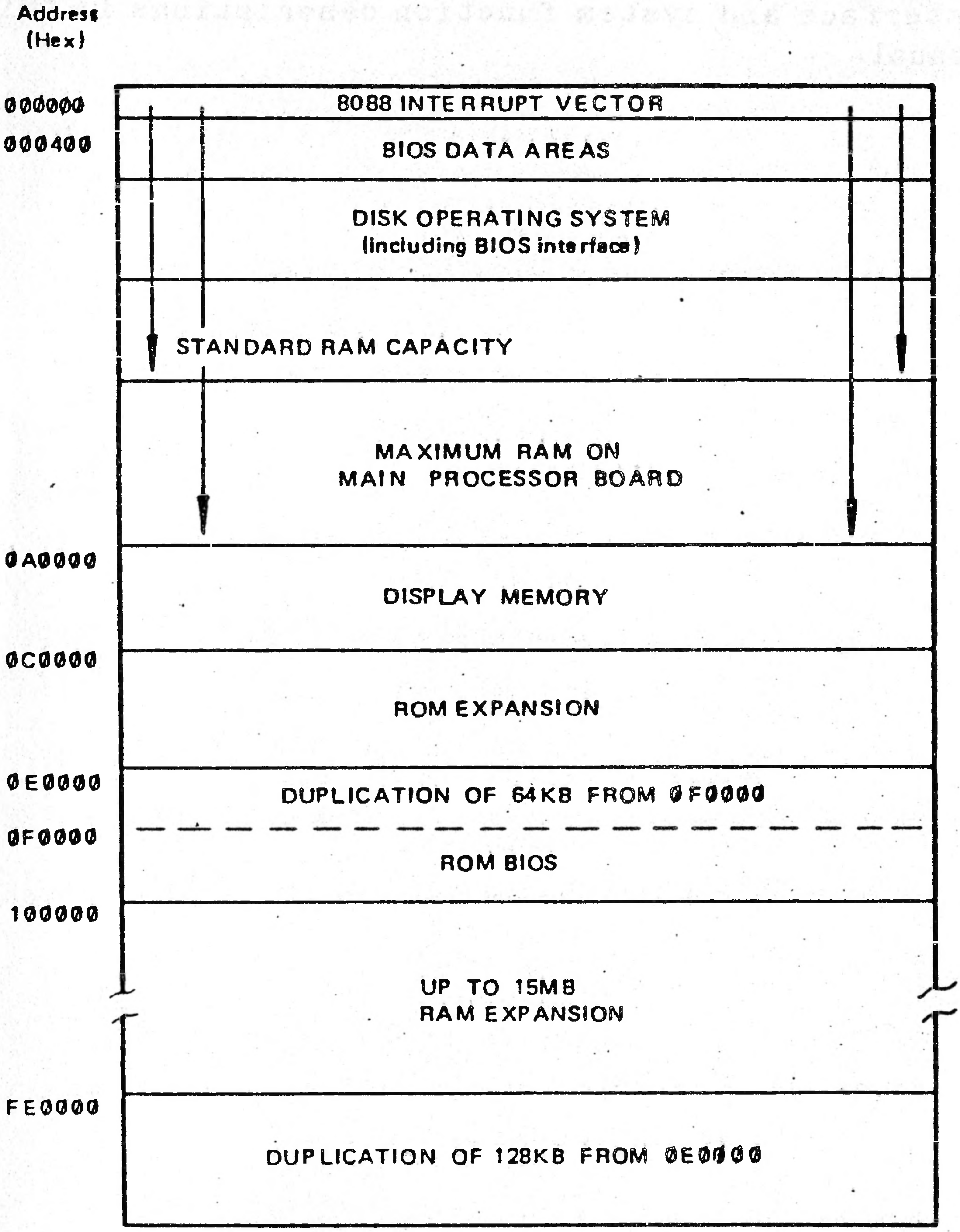


Figure 1.10 Memory map

THE I/O MAP

Figure 1.11 illustrates the use of port addresses in the I/O map of the NCR PERSONAL COMPUTER. Details of system use are to be found in the appropriate interface and system function descriptions in this Manual.

Port (hex)	System Use
00-1F	DMA Controller 1 (8237)
20-3F	Programmable Interrupt Controller (8259) (Master)
40-5F	Programmable Interval Timer (8254)
60-6F	Parallel Input/Output Interface (8042)
70-7F	Real-time clock and NMI
80-9F	DMA Page Select Register
A0-BF	Programmable Interrupt Controller 2 (8259)
C0-DF	DMA Controller 2 (8237)
E0-EF	Software Protection PROM
F0	Clear Co-processor Busy
F1	Reset Co-processor
F8-FF	Co-processor
1F0-1F8	Hard disk
200-207	Reserved (games adapter)
278-27F	Parallel interface 2
2F0-2F7	Reserved
2F8-2FF	Asynchronous Serial I/O (2)
300-31F	Reserved
360-36F	Reserved
378-37F	Parallel Interface 2
380-38F	DLC Interface and Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Character Display Controller
3C0-3CF	Reserved
3D0-3DF	Graphics Display Controller
3F0-3F7	Flexible Disk Controller
3F8-3FF	Asynchronous Serial I/O (1)

Figure 1.11 I/O map

THE POWER SUPPLY

The primary-switched power supply contained in the main unit supplies power to the following parts of the system:

* Main processor board
* One or two flexible disk drives
* One or two hard disk drives
* Expansion slots
* Keyboard
* Display (primary output)

The power supply is cooled by a fan with temperature-dependent rotation speed. The fan supply is <= + 12 Vdc (pin P5 is ground).

Primary input characteristics of the power supply are given in Figure 1.12.

Voltage (switchable) Nominal	Min.	Max.	Frequency (Hz) Min.	Max.	Max. Current (Amps)
115	100	127	57	63	5
230	200	240	47	53	3

Figure 1.12 Power source requirements

Figure 1.13 gives details of secondary, rectified output power. In addition, a Power Good signal is provided, which is capable of driving up to six TTL loads. For reasons of output stability, a dummy load resistor is connected as long as no hard disk drive is installed.

Voltage Nominal	Voltage Tolerance (%)		Load current (amps) Min.	Load current (amps) Max.	Max. power (W)
+ 5	- 4 to	+ 5	7.0	19.8	99
- 5	- 8	+ 10	0.0	0.3	1.5
+ 12	- 4	+ 5	2.5	7.3	87.6
- 12	- 9	+ 10	0.0	0.3	3.6
			Total power dissipation		191.7

Figure 1.13 Power output

Figures 1.14 and 1.15 show power cable connections to the main processor board and the disk drives.

Connector	Pin	Voltage/Signal
J8	1	Power Good
	2	+ 5 Vdc
	3	+ 12 Vdc
	4	- 12 Vdc
	5,6	Ground
J9	1,2	Ground
	3	- 5 Vdc
	4,5,6	+ 5 Vdc

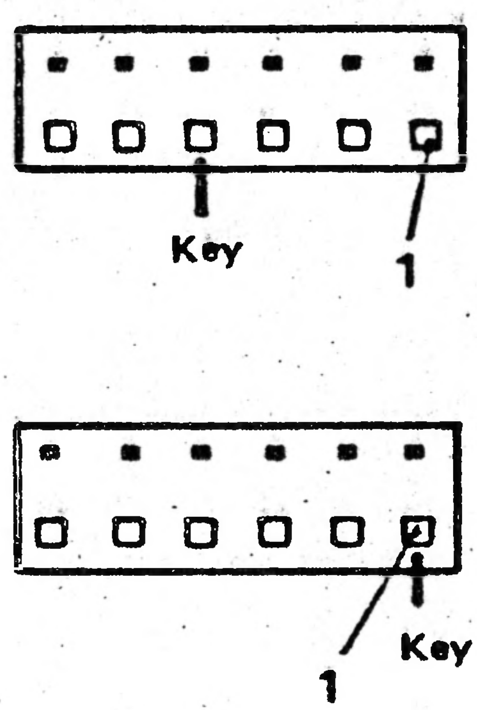


Figure 1.14 Power connections to main processor board

Connector	Pin	Voltage/Signal
J2	1	+ 12 Vdc
	2,3	Ground
	4	+ 5 Vdc

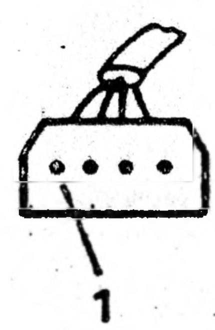


Figure 1.15 Power connections to disk drives

THE BATTERY

Providing power for the real-time clock and CMOS RAM is a 6 Volt Lithium battery. The pin assignments of its connector are shown in Figure 1.16.

Pin	Voltage
J21-1	+ 6 Vdc
J21-2	Key
J21-3	No connection
J21-4	Ground

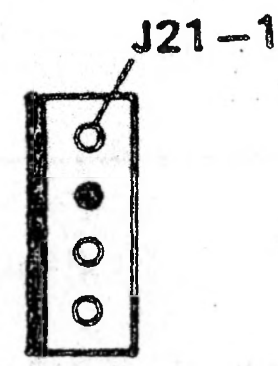


Figure 1.16 Battery connector

SOFTWARE PROTECTION

Use of an application can be effectively confined to a single main unit by making successful execution dependent on the identification of a unique code. Such a code is held in a PROM mapped into I/O addresses in the range

OEOH - OEFH

The PROM structure of this machine identification is set out below. All digits are coded as 4-bit binary values (e.g. "9" is coded as 1001), other characters are ASCII-coded (e.g. "C" is coded as 43H).

I/O address byte (Hex)	Contents	Significance
E0	C	
E1 - E2	3279	NCR Class (3 is lowest nibble)
E3	00	
E4	17	(1 is lower nibble)
E5	hyphen (2DH)	
E6 - E8		Tracer no. in 6 digits
E9	00	
EA - EE	00	Can be used for customer expansion (own PROM)
EF	00	

Programmable Intelligence

This Chapter introduces a number of highly versatile integrated circuits present on the main processor board. The ICs described perform functions which to many users are not always evident at first sight, but which are, however, integral to the efficient working of your NCR PERSONAL COMPUTER. These ICs are the Timer, the Programmable Interrupt Controllers, the Parallel Input/Output Interface, and the DMA controllers.

The Timer, as its name suggests, provides a useful tool for real-time applications. It can be set to issue an output signal after a programmed delay on a one-off basis, or it can supply repeated signals at programmed intervals. It can even be used to supply oscillator frequencies for the small loudspeaker (this is described in a separate Chapter).

The Programmable Interrupt Controllers detect and manage service requests not only from selected peripheral devices but also from other internal system functions, such as the Timer. The obvious advantage of a Programmable Interrupt Controller is that the system microprocessor (Central Processing Unit) does not have to continuously check the other units ("polling") to see if they are requiring attention: the CPU is interrupted only if a unit has expressly requested attention and the Programmable Interrupt Controller has decided, on the basis of its programmed priority logic, that the request deserves attention.

The Parallel Input/Output Interface relates to a number of system functions: it reads keyboard data as well as the system hardware configuration (memory, disk, co-processor, display), and has certain enabling functions (serial I/O, RAM parity check).

PROGRAMMABLE INTELLIGENCE

The Direct Memory Access (DMA) controllers offload the CPU where blocks of data have to be transferred to and from random access memory. Although the CPU cannot use the system bus during DMA cycles, it can perform internal register arithmetic. Bus arbitration circuitry ensures that CPU and DMA controller do not clash over the system bus.

The Real-Time Clock provides clock and calendar functions. Time and date can be read from battery-supported CMOS RAM in the CPU I/O map. This RAM totalling 64 bytes, also contains system configuration information.

Your NCR PERSONAL COMPUTER can include other programmable integrated circuits dedicated to more readily recognized peripheral control functions, for example the serial I/O, CRT, flexible and fixed disk controller interfaces. These are described in the relevant Chapters of this Manual.

The system microprocessor is an 80286, with the possible addition of an 80287 mathematics co-processor. There is a wealth of generally available literature on the this family of microprocessors to which you can refer.

RECOVERY TIME

Because of the high frequency at which the CPU is clocked, it is inadvisable to address another integrated circuit with consecutive CPU instructions. The reason for this precaution is that some ICs may not recover in time following the first I/O operation.

To avoid posssible problems insert a "dummy" CPU instruction between I/O operations to the same IC. A JUMP SHORT (relative) instruction fulfils this requirement:

```
JMP SHORT $+2                  ;Opcode EB 00
```

This is usual assembly language syntax for "jump two bytes ahead of the first byte of this instruction", that is, simply go to the next instruction. A simple register-to-register instruction will not delay long enough.

80286/80287 CO-ORDINATION

The co-processor, which can be installed as an option, is clocked with 2/3 of the CPU clock frequency. The co-processor functions as a device in CPU I/O address space. The following ports are dedicated to the CPU/co-processor interface:

OF8H-OFFH	Transfer of opcodes and operands from CPU to co-processor, and return of results.
OF1H	Writing the value zero to this port sets the co-processor's Real Address mode of operation. This is the power-on/reset status. (Protected mode is achieved at CPU level by means of SETPM followed by the ESCape instruction.)
OFOH	Writing the value zero to this port clears the co-processor's Busy latch.

When an unmasked co-processor error occurs, the Busy signal and interrupt request 13H are issued.

THE PROGRAMMABLE INTERVAL TIMER

Interval timing in the NCR PERSONAL COMPUTER is provided by an 8254 Programmable Interval Timer. This integrated circuit can be used as three independent 16-bit counters. The Timer is interfaced to the data bus, so that Timer values can be transmitted and read by the microprocessor. In addition, the Timer can be used to generate interrupts at programmed intervals or a single interrupt after a specific interval. Counting is carried out internally by the Timer, either as a binary or a Binary Coded Decimal (BCD) operation. Counting speed is determined by an external clock signal. Counting is achieved by decrementation of a Counter from the value loaded down to zero.

HARDWARE CONFIGURATION

Communication between Timer and microprocessor is via the Port addresses 40H-43H (see Figure 2.1).

Instruction	Function
OUT 40H	Load Counter 0
OUT 41H	Load Counter 1
OUT 42H	Load Counter 2
OUT 43H	Specify Timer operation
IN 40H	Read Counter 0
IN 41H	Read Counter 1
IN 42H	Read Counter 2
IN 43H	No operation

Figure 2.1 Timer ports

The signal frequency of 1.19318 MHz common to all three clock inputs of the Timer (CLK0, CLK1, CLK2) is derived from a 14.318 MHz crystal with capacitive trimmer adjustment, an 8284A Clock Controller, and one further division (by 2). Note that this is separate from the crystal from which the CPU clock is derived.

The three output signals from the Timer (OUTO, OUT1, OUT2) are issued to the following system components:

OUTO - Timer Interrupt (type 8) to the 8259A Programmable Interrupt Controller. This Timer output is set to an effective frequency of approximately 18.2 ticks per second (more accurately: 18.2065) by loading the 16-bit Counter with the maximum decrement value of zero (not OFFFFH: terminal count is not attained until the decrementing counter passes to zero).

OUT1 - Memory Refresh line. Initialization firmware requires only the lower 8 bits of the decrement Counter. The value set is 12H, which yields a signal period of approximately 14 microseconds.

OUT2 - Signal to the parallel input/output interface with unrestricted user availability.

TIMER PROGRAMMING

Counters can be programmed independently of one another. Before a counter is initialized it is in an undefined state. The following programming steps are required, in order to set up a Timer Counter.

One byte must be transmitted to the Timer's Control Register via Port 43H. The value of this byte is made up as shown in Figure 2.2.

D7	D6	D5	D4	D3	D2	D1	D0	via Port
COUNTER		R/W SELECT		MODE			BCD	43H

Figure 2.2 Timer control register

COUNTER is a two-bit binary value 0-2, denoting the number of the Counter to be accessed. Therefore, to access Counter 2, D7 should be set and D6 zero.
R/W SELECT determines the way in which the specified Counter is to be loaded or read. The type of operation to be carried out (read or load) depends on whether an IN or OUT instruction is being used (the Timer has pin connections for /RD and /WR signals). The significance of the binary value contained in these two bits is as follows:

0 Counter Latching (see below)
1 Read/load more significant byte of Counter
2 Read/load less significant byte of Counter
3 Read/load both Counter bytes (less significant first)

BCD: if this bit is set, the 16 bits of the selected Counter are used as a 4-digit BCD counter. If this bit is zero, the Counter represents a 16-bit binary value.
MODE may be a binary value 0-5 in three bits. The following modes can be implemented in the NCR PERSONAL COMPUTER hardware (applications requiring a rising edge at the GATE can be implemented only with Timer 2):

0 - Output on terminal count
1 - Programmable one-shot
2 - Rate generator
3 - Square wave generator
4 - Software triggered strobe
5 - Hardware triggered strobe

These Timer modes are described in detail in the following sections. Timing characteristics for the Timer modes are illustrated in Figure 2.3.

Output on Terminal Count (Mode 0)

Following the loading of the Counter, the signal OUTput pin for that Counter goes low, and remains low until the Counter has decremented to zero. The OUT signal then goes high, and remains high until the Counter is next programmed. If you write a new value to the Counter before the old count has expired, decrementing resumes from the new value. From the hardware point of view, mode 0 is enabled by a high signal at the Gate for the specified Counter. This signal is permanently present at the Gate for Counters 0 and 1.

Programmable One-Shot (Mode 1)

OUTput goes low following a rising edge at the GATE, and goes high at terminal count. Resetting the counter value while OUTput is low does not affect the current terminal count, but comes into effect the next time the OUTput signal goes from high to low. The one-shot can be re-triggered without any need to reload the Counter.

Rate Generator (Mode 2)

An OUTput low pulse of one clock is issued upon terminal count. This cycle is initiated by the GATE going from low to high, and continues until the GATE goes low. A newly set Counter value comes into effect after the next OUTput pulse.

Square Wave Generator (Mode 3)

As Mode 2, except that OUTput remains high for the first half of the count and goes low for the second half (achieved by decrementing by 2 at each clock). If the Counter specifies an odd number, the first decrement in the first countdown is by 1, the next countdown starts with a decrement of three. This sequence is repeated until the GATE goes low.
The square-wave characteristic of this mode makes it suitable for driving louspeaker circuitry.

Software Triggered Strobe (Mode 4)

As soon as this mode has been loaded, the OUTput for the selected Counter on the Timer goes high. When the Counter has been subsequently loaded, counting begins. As soon as the count has decremented to zero, the OUTput goes low for one clock period, and then high again. If your software reloads the Counter during decrementing, the new Counter value takes effect at the next clock signal. As in mode 0, operation of mode 4 is dependent on the presence of a

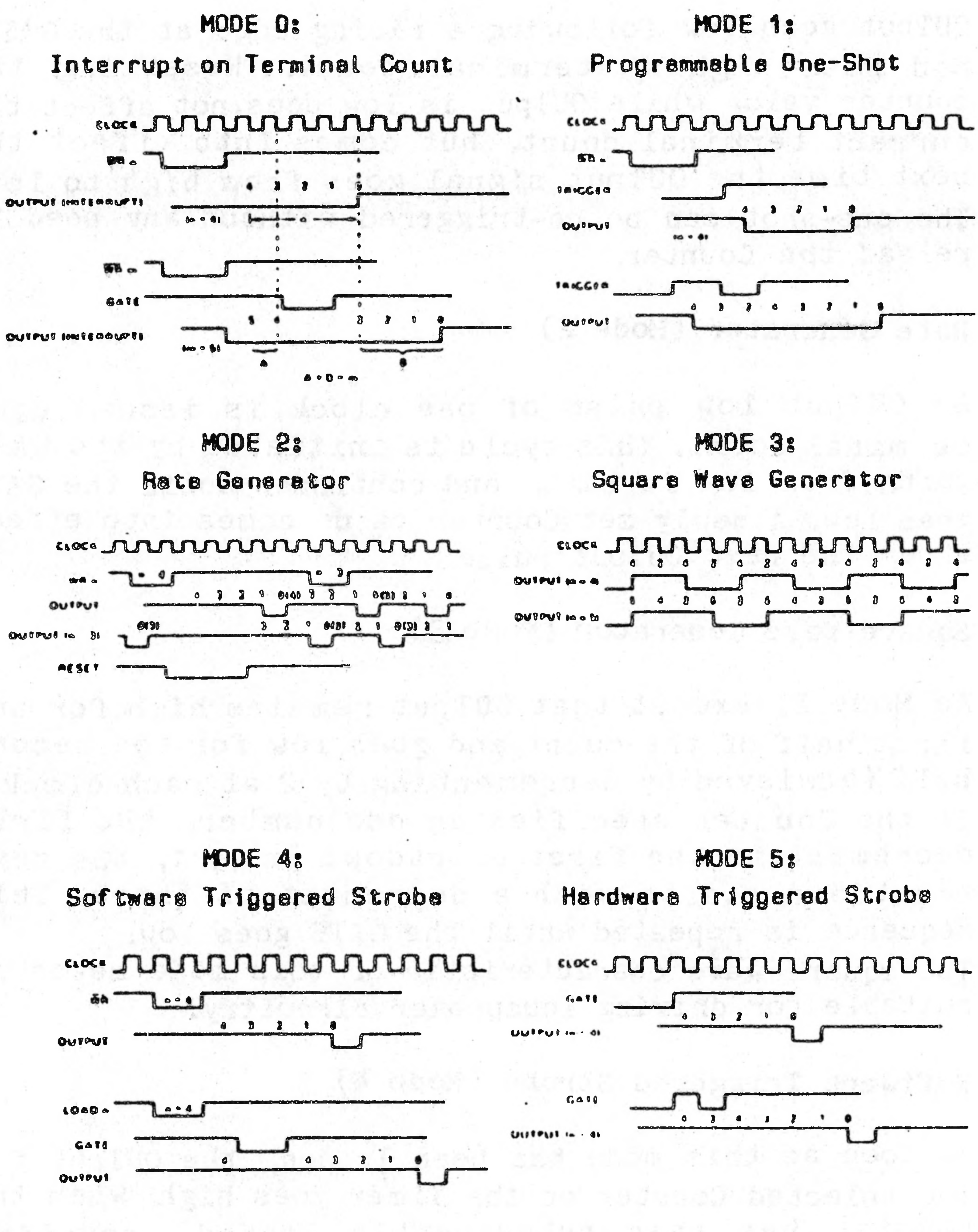


Figure 2.3 Timer Modes

high signal at the Gate (decrementing would be suspended if this signal were low).

Hardware Triggered Strobe (Mode 5)

Following a rising edge at the GATE, counting starts. The count continues until terminal count, whereupon the output goes low for one clock period. The count can be re-triggered at the GATE without reloading the Counter.

Timer Parameters

Following the Timer Control Register byte detailed above, the Timer expects the number of bytes specified in the two bits R/W to be transmitted by the microprocessor (load operation), or the specified number of bytes to be read. The one or two-byte value is then read from or written to the data bus. Loading all zeros into a Counter results in a maximum count (OFFFFH in binary, 9999 in BCD counting).

Note that it is not necessary to read or write immediately after setting the Timer Control Register. However, the specified number of bytes must be read or written. In mode 0, as soon as the Timer recognizes that the first (or only) byte is being transmitted, the decrementing process is suspended until the new Counter contents have been read.

Reading the Counters

Reading Counter registers requires some care in order not to disturb the counting process. A Counter can be read directly or via a Counter Latch. The former method requires counting to be inhibited during the reading process. This can be achieved only by controlling the Gate or suspending the clock signal to the Counter which is to be read. For this reason, you should use the Counter Latch method.

To read a Counter Latch, a byte must be written to the Control Register, specifying the Counter and with

D5 and D4 zero (this command has no effect on the MODE and BCD settings). Then issue a read Counter byte to the Control Register and read the one or two bytes specified.

THE PROGRAMMABLE INTERRUPT CONTROLLER (PIC)

INTRODUCTION

Why use Interrupts?

There are two methods by which a call for attention from a device can be recognized by a program. One method is for the microprocessor to sample the status of the device at periodic intervals (polling), whereupon the program decides whether that status represents a call for attention. The other method is for the processor to be "interrupted" by a signal from the device, and then to proceed to a program routine which deals with the special situation. Afterwards, execution of the interrupted program may continue, if desired.

The advantage of the first method is that a large number of devices can be read via the computer port addresses, without additional hardware. This method can be most effectively applied in situations where information from a device is constantly required at regular intervals. Disadvantages arise when this need for information, or the device requests for attention, are only occasional and irregular. Polling then means in many cases ineffective use of microprocessor time. Furthermore, the time which elapses before the device request for attention is recognized can vary, depending on conditional branches taken within the current program.

For these reasons, it is often more practical to make use of the ability of the microprocessor to recognize an external interrupt in the form of a signal at the INTR pin. Assuming that interrupts at the microprocessor are currently enabled, the interrupt signal is noted by the microprocessor in an internal flip-flop, and another microprocessor pin issues a signal acknowledging the presence of the interrupt signal. Although the microprocessor does not proceed to deal with the interrupt until completing the current instruction cycle (assembler instruction), it is not necessary to synchronize the issuing of an interrupt with the microprocessor.

Interrupts and the Microprocessor

Following acknowledgement of the interrupt by the microprocessor, the interrupting device must place an 8-bit value on the data bus. This value represents one of 256 different interrupt "types". The first five types of interrupt are reserved by the microprocessor for special, internal purposes:

- Type 0 Division by Zero.
- Type 1 Single Step.
- Type 2 Non-maskable Interrupt: this interrupt type is recognized when a signal (active low) is present at the NMI pin of the microprocessor.
- Type 3 This interrupt type is recognized when a software interrupt is issued by means of the one-byte INT instruction.
- Type 4 Integer Overflow.

The NCR PERSONAL COMPUTER hardware makes use of the fifteen interrupt types in the range 8-17H, in addition to the NMI (described at the end of this section). The Basic Input/Output System software (BIOS) uses a number of other interrupt types for "software" interrupts (INT instruction).

Starting with the next instruction cycle, the microprocessor automatically PUSHes the flags onto the stack and clears the interrupt flag, thus disabling further interrupts. Following this, the current values of the Code Segment and Instruction Pointer are PUSHed onto the stack, and new values, determining the starting address of the interrupt service routine, are fetched from the "interrupt vector" which occupies the first 1024 bytes of machine memory. After this routine has dealt with the interrupt situation, and provided that the interrupt service routine is concluded by an IRET instruction, the Code Segment and Instruction Pointer are restored to their former values. The flags are likewise restored, with the effect that the interrupt flag is enabled for further interrupts. (It is admissible for the interrupt service routine to enable the interrupt flag, thus allowing interrupts to be nested.)

The "interrupt vector", in the microprocessors's "Real Address" mode, is the 1024-byte area at the beginning of machine memory, where the CS and IP values for up to 256 interrupt types are held. Therefore, addresses 0-3 are concerned with interrupt type 0, addresses 4-7 with type 1, and so on. In each case, the paragraph value (CS) of the address of the interrupt handling routine must be present in the two uppermost bytes of the four byte block, the Instruction Pointer value in the two lowermost bytes. For example, the CS part of the starting address of the interrupt service routine for interrupt type 10 (0AH) is fetched from bytes 2AH and 2BH, the IP value from bytes 28H and 29H.

INTERRUPT CONTROLLER HARDWARE AND LOGIC

The NCR PERSONAL COMPUTER makes use of two 8259A Programmable Interrupt Controller (PIC) integrated circuits in a master/slave configuration. One PIC can control up to eight interrupts from different sources, tell the microprocessor which device has requested attention, and allow the programmer to set priorities among the possible interrupts.

Refer to the schematics in the Appendices regarding the integration of the PICs into the NCR PERSONAL COMPUTER hardware.

Use of the interrupt lines which can be controlled by the PICs is shown in Figure 2.4.

Interrupt Request No. (PIC #)	Microprocessor Int. Type No. (CS+IP in int. vector)	IRQ Line accessible at bus connection	Hardware Function
0 (#1)	8 (20H-23H)	not accessible	Timer 0
1 (#1)	9 (24H-27H)	not accessible	Keyboard
2 (#1)	0AH (28H-2BH)	not accessible	interrupt from #2
3 (#1)	0BH (2CH-2FH)	B25	COM2
4 (#1)	0CH (30H-33H)	B24	COM1
5 (#1)	0DH (34H-37H)	B23	Parall. I/F2
6 (#1)	0EH (38H-3BH)	B22	Flex. Disk
7 (#1)	0FH (3CH-3FH)	B21	Parall. I/F1
8 (#2)	70H (1C0H-1C3H)	not accessible	Real-T. Clk
9 (#2)	71H (1C4H-1C7H)	B4	Softw.->IRQ2
0AH (#2)	72H (1C8H-1CBH)	D3	Reserved
0BH (#2)	73H (1CCH-1CFH)	D4	Reserved
0CH (#2)	74H (1D0H-1D3H)	D5	Reserved
0DH (#2)	75H (1D4H-1D7H)	D6	Co-processor
0EH (#2)	76H (1D8H-1DBH)	D7	Fixed disk
0FH (#2)	77H (1DCH-1DFH)	not accessible	Reserved

Figure 2.4 PIC interrupt requests

PROGRAMMING THE PIC

The 8259A Programmable Interrupt Controller can be regarded as consisting of four logical aspects, as shown in Figure 2.5. This programming description deals with the most important general aspects of programming the PIC, drawing special attention to those programming elements which are essential to it's functioning in the NCR PERSONAL COMPUTER environment. For a complete description of the PIC hardware and software interfacing possibilities, you may wish to refer to the publications of the integrated circuit manufacturer.

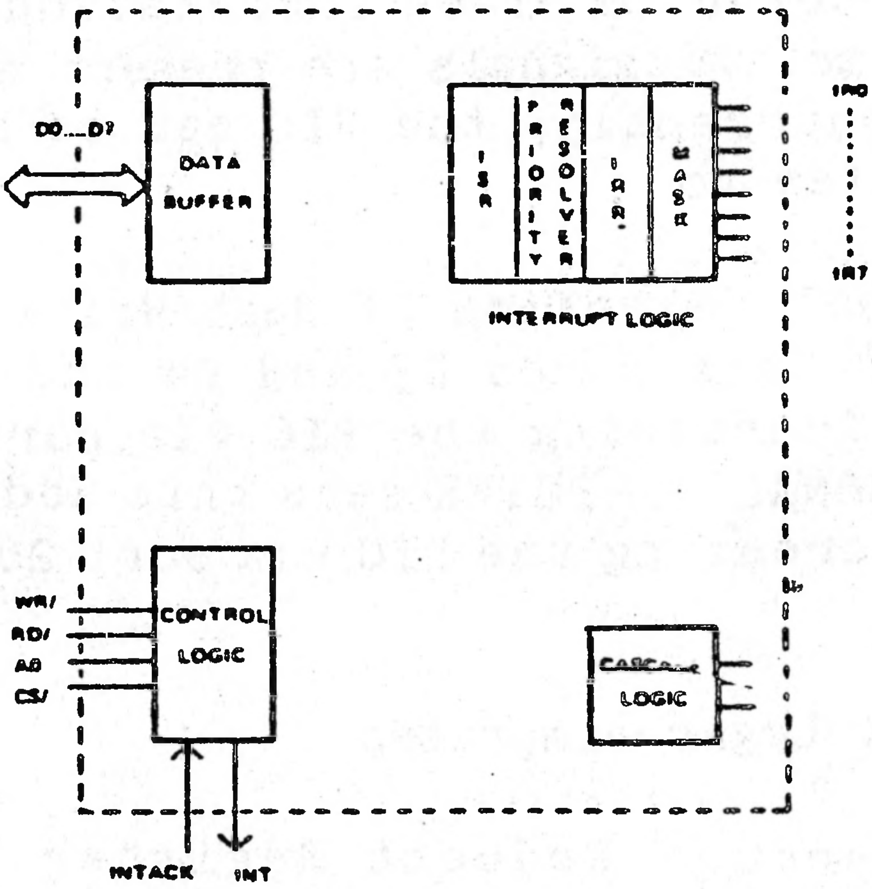


Figure 2.5 PIC architecture

The data buffer provides a three-state interface to the system bus.

The Control Logic consists of

* Selection of the PIC by means of an (active low) signal to the CS/ pin. If this signal is not present, the PIC cannot be read or written to.

* Issuing an interrupt signal (active high) to the microprocessor and awaiting acknowledgement

(active low) from the microprocessor. In 8088 mode, the first of these acknowledgement signals places the identity of an interrupt in the In-Service Register (see below). A second signal causes the PIC to place an interrupt number on the data bus, with which the processor will calculate the four bytes (CS+IP) to be read from the interrupt vector in machine memory.

* The Read/Write logic. Following an active low signal at the WR/ pin, the PIC can receive commands from the microprocessor. If there is an (active low) signal at the RD/ pin, the PIC can be instructed to place information on the data bus. If active signals are present at both these pins concurrently, the PIC can be neither read nor written to.

* Additional selection of Read/Write functions by means of data lines D3 and D4 and the address line 0. Addressing the PIC via port 21H of the NCR PERSONAL COMPUTER sets this address line to high, addressing the PIC via port 20H sets it to low.

The Interrupt Logic comprises

* The Interrupt Request Register (IRR). This register notes for each of the eight interrupt lines whether an interrupt is waiting to be handled. A bit in the IRR is set by a signal (active high) on the corresponding interrupt line. This signal must remain high until the processor is ready to deal with that interrupt.

* The In-Service Register (ISR). This register stores interrupts which are currently being handled. The bit for a particular interrupt is set as soon as the acknowledgement signal arrives from the microprocessor. The corresponding bit in the IRR is then reset.

* The Priority Resolver. This decides the priority of the interrupts. An interrupt acknowledgement

signal transfers the interrupt with the highest priority from IRR to ISR.

* Interrupt Mask Register. This register disables individual interrupt request lines by means of a bit mask. Masking an interrupt request (IR) line does not affect the other IR lines.

The Cascade Logic uses three lines so that up to eight slave PICs can be addressed. The slave is addressed by the master whenever the former has to place an interrupt type number on the bus. Therefore, the cascade line are output for a master PIC, and input for a slave PIC.

In principle, each Interrupt Request signal can be supplied by a separate slave PIC. The NCR PERSONAL COMPUTER master PIC uses only one IR line for slave connection (IR2).

Communication between microprocessor and PIC consists of Initialization Command Words (ICW) and Operation Command Words (OCW) transmitted to the PIC, and PIC register status (IRR, ISR, IMR, or interrupt type) read by the processor. Figure 2.6 summarizes the signals required in order to switch between these various modes of communication. The software means by which these initialization and operational functions are achieved is explained in the remainder of this description of interrupts.

A0	RD/	WR/	D3	D4	
0	1	0	x	1	Data bus is to be read by PIC as ICW1.
0	1	0	0	0	.... OCW2.
0	1	0	1	0	.... OCW3.
1	1	0	x	x	Data bus is read by PIC as OCW1, ICW2, or ICW3, according to logic sequence of commands (see below).
0	0	1			The PIC is to place IRR, or ISR, or interrupt type on data bus, according to contents of previous OCW2.
1	0	1			The PIC is to place IMR on data bus.

Figure 2.6 PIC addressing

Note: These commands are valid only if the CS line is active (low). If this line is high, or if both RD/ and WR/ are active (low), PIC access to the data bus is disabled.

Initializing the PIC

The microprocessor must place up to four Initialization Command Words (ICWs) on the data bus in order to initialize the PIC. ICW1 must be transmitted to the PIC with address line A0 at logical 0 (Port 20H for master PIC #1, 0A0H for slave PIC #2). Transmission of the other ICW's requires that A0 is set to 1 (Port 21H for PIC #1, 0A1H for PIC # 2). The format of the first two of these data bytes is shown in Figure 2.7.

	D7	D6	D5	D4	D3	D2	D1	D0	via Port
ICW1	0	0	0	1	DETECT	0	CASC	ICW4	20H/0A0H
ICW2	<—— PIC base int. type ——>					0	0	0	21H/0A1H

Figure 2.7 Initialization command words 1 and 2

D7-D5 in ICW1 are really "don't care". (They are only required in the PIC 8080 mode, where they state an interrupt vector address.)
DETECT indicates whether interrupts are level or edge triggered. The NCR PERSONAL COMPUTER firmware resets this bit (0), thus determining edge triggering.
If edge triggering is set, an interrupt is recognized upon a low to high transition on an interrupt request line. Level triggering is achieved by the presence of a high signal. Note that the interrupt signal (sequence of trigger pulses or constant high, according to DETECT mode selected) must not be removed from the interrupt request line until the first acknowledgement signal for that interrupt has been received from the microprocessor. In practical terms, this means that the IR signal should be reset at the issuing device by the interrupt service routine, otherwise the PIC may recognize the continued signal as a second interrupt request (see also "Signal Integrity", below).
CASC is zero (0) to indicate that the PIC is not single, but is operating in a master/slave configuration (cascading). This applies to both PIC #1 and PIC #2.
ICW4 is set (1) to indicate that ICW4 is included as the last Initialization Command Word.

D7-D3 in ICW2 are to contain a binary value in five bits corresponding to the microprocessor interrupt type to be issued in response to an interrupt signal at PIC pin IR0. For example, the value 8 (01000B) determines that a valid interrupt request at PIC pin IR0 will cause the PIC to notify interrupt type 40H to the microprocessor. IR1 then corresponds to interrupt type 41H, and so on. The actual five-bit value for D7-D3 used by for PIC #1 is 1, so that IR0 results in microprocessor interrupt type 8 (IR1: interrupt type 9, etc.). The corresponding value for PIC #2 is 0EH, so that IR8 governs interrupt type 70H (IR9: interrupt type 71H, etc.).

ICW3 is used by the PIC for master/slave identification. ICW1 has already stated that there is

more than one PIC in the configuration (where ICW1 indicates a single PIC, ICW3 is omitted from the initialization sequence).
For the master (PIC #1), ICW3 is a bit map reflecting those Interrupt Request lines deriving their source signals from a slave PIC. The NCR PERSONAL COMPUTER therefore requires bit 2 to be set (see Figure 2.4).
In the case of the slave (PIC #2), the five MSBs of ICW3 are zero, while the three LSBs reflect the slave's identification; therefore ICW3 for PIC #2 isgiven the value 2.

The format of ICW4 is shown in Figure 2.8.

	D7	D6	D5	D4	D3	D2	D1	D0	via Port
ICW4	0	0	0	SM	BUF	M/S	AEIO	P	21H/0A1H

Figure 2.8 Initialization command word 4

SM, if set, instructs the PIC to apply a special fully nested mode when PIC's are cascaded in a master/slave configuration. This ensures that servicing an interrupt from a slave does not preclude higher priority interrupts from the same slave.
BUF, if set, applies a buffered mode to interrupt requests.
M/S determines whether a PIC is master (1) or slave (0), provided that the BUF bit is set.

Where ICW4 is written with all three bits SM, BUF, and M/S zero, the normal fully nested mode of interrupt priority applies (see next section).

AEIO can be set or zero. When zero, this has the effect that the ISR bit is not reset until an End-of-Interrupt (EOI) command is encountered at the end of the interrupt service routine (see Operation Command Words, below). If AEIO is set, the ISR bit is reset when the PIC detects the trailing edge of the second interrupt acknowledgement signal from the

microprocessor. In order to clear this "automatic" End-of-Interrupt mode, it is necessary to repeat the PIC initialization, this time with AEIO zero.
P denotes the type of microprocessor being used in conjunction with the PIC. This bit is set (1) to denote the presence of the 80286 CPU.

Operation Command Words

Following the initialization described above, the PIC is ready to receive interrupts on all eight interrupt lines (IR0-IR7). It is good practice initially to mask (disable) all the interrupt lines, either by means of the microprocessor CLI instruction or the Operation Commands Words described below, or both. An interrupt request must not be allowed to occur until its interrupt vector entry is written and its interrupt service routine is available. Furthermore, interrupt requests which are not in use should be masked by OCW, so that spurious line signals do not pass control to a possibly non-existent interrupt service routine. Fortunately, this set-up procedure is taken care of by the initialization firmware. However, you should bear these considerations in mind, if you wish to use a particular interrupt request for a purpose other than its standard hardware function. If this is the case, you should be wary of re-assigning these hardware interrupts, as this means depriving the BIOS of its hardware interface. More often than not, such changes will entail writing alternative initialization procedures and BIOS routines.

The Operation Command Words (OCWs) make it possible for you to mask and unmask (disable and enable) individual interrupt request lines to the PIC, and to set priority schemes for dealing with interrupts. These facilities result in considerable savings of microprocessor time for your application, as an interrupt is passed to the microprocessor only if it fulfills the conditions determined by the current masking and priority scheme.

PROGRAMMABLE INTELLIGENCE

Even without Operation Command Words the PIC is capable of receiving interrupt requests. The PIC is then in the "Fully Nested Mode". Interrupt requests are regarded by the PIC as having different priorities: IR0 has the highest priority, IR7 the lowest.

As soon as the interrupt acknowledgement is received from the microprocessor, the PIC places on the data bus the interrupt type of the interrupt request (see ICW2) with the highest priority. This means that if more than one interrupt request is present at a time, the one with the highest priority is dealt with. The PIC recognizes which IR lines have requested an interrupt by inspecting its Interrupt Request Register (IRR).

The PIC then checks its In-Service Register (ISR) to see if an interrupt is currently being processed. If none is being serviced, the interrupt type is transmitted to the processor and the interrupt service routine is activated as outlined in the Introduction to this description. The ISR bit for the interrupt is now set, and the corresponding IRR bit zero.

If an interrupt is currently being serviced, the PIC checks whether the new interrupt request is of higher priority. If this is the case, the ISR bit for the new interrupt is set, and the corresponding IRR bit is reset. The new interrupt request is then allowed to interrupt the currently active interrupt service routine: flags, CS and IP of the interrupted routine are PUSHed onto the stack in the usual way, so that the microprocessor can later find its way back to this routine, without assistance from the PIC. In the event that the new interrupt request is of priority equal to or lower than that of the interrupt currently being serviced, the new interrupt request must wait (IRR bit remains set) until higher priority interrupts have been serviced.

Your software can, of course, set and clear the CPU interrupt flag (assembler instructions: STI, CLI). By clearing the interrupt flag, all interrupts to the processor, including those of higher priority, are disabled. However, interrupt requests occurring while the processor interrupt flag is cleared are not lost, as an IRR bit in the PIC is reset only when the interrupt is about to be serviced.

Once an interrupt from the PIC has been serviced, its ISR bit must be reset, so that waiting interrupts can be dealt with. Assuming that the AEIO bit in ICW4 was zero, interrupt service routines should conclude with an EIO Operation Command Word. This clears the appropriate bit in the ISR, thus informing the PIC that a particular interrupt has been serviced. Two EOIs have to be issued after servicing an interrupt to a slave PIC, as both master and slave must be informed).

There are two types of EOI commands. As long as the priority scheme is the default Fully Nested Mode, you do not have to specify which interrupt has been serviced. The PIC will automatically reset the highest priority ISR bit currently set, this representing the most recently acknowledged and serviced interrupt. Therefore, a "non-specific" EOI is all that is required. A "specific" EOI is required in situations where your software has determined a priority scheme deviating from that of the Fully Nested Mode (see OCW2, below). This is because the PIC cannot ascertain the source of the interrupt most recently acknowledged and serviced. A "specific" EOI differs from a "non-specific" EOI, in that the former must specify one of the eight interrupts.

If automatic End-of-Interrupt is active (AEIO bit in ICW4 was set), the EOI automatically issued is non-specific. You will normally use the automatic End-of-Interrupt facility only when a nested priority structure is not required, for example, when all IR lines except one are masked. To alter the value of the AEIO bit, your software must go through the complete ICW sequence again.

The masking and priority scheme of the PIC can be programmed by means of up to three Operation Command Words. OCW1 can be transmitted only when address line A0 is at logical 1 (Port 21H for PIC #1, port 0A1H for PIC #2). For the other OCWs, A0 must be 0 (Port 20H for PIC #1, 0A0H for PIC #2). Operation Command Words do not have to be issued in a particular sequence.

OCW1 masks all or selected interrupt requests to the PIC. If a bit in the Interrupt Mask register is set, the corresponding ISR bit is masked. However, once an interrupt has been acknowledged by the PIC, it will inhibit lower priority interrupt requests irrespective of subsequent masking.

	D7	D6	D5	D4	D3	D2	D1	D0	via Port
OCW1	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0	21H/0A1H

Figure 2.9 Operation command word 1

	D7	D6	D5	D4	D3	D2	D1	D0	via Port
OCW2	R	SEOI	EOI	0	0	Int. Request			20H/0A0H

Figure 2.10 Operation command word 2

The significance of bits D7-D5 in OCW2 is as follows:

R: when set, this bit instructs the PIC to rotate priority.
SEOI: when set, this bit denotes a specific End-of-Interrupt or a new priority setting. The binary value in bits D2-D0 must denote which interrupt is to be affected.
EOI: when set, this bit tells the PIC to recognize an End-of-Interrupt.

The principle of priority rotation requires a few words of explanation. Priority rotation can be applied when the default Fully Nested Mode is not required. Then the IR number of an interrupt request does not necessarily indicate its current priority. When the ISR bit of the most recently serviced interrupt has been reset, this interrupt should be given the lowest priority. This same interrupt request line must then wait a maximum of 7 interrupts before its ISR bit can be set again. This equal priority rotation can be achieved by OCW2. If both bit R and bit EOI are set (OCW2=0A0H), this is interpreted by the PIC as a "rotate on non-specific EOI". This command has the effect illustrated by the following example.

Let us assume that IR5 is waiting for attention, and that IR3 is currently being serviced. As soon as the IR3 bit in the ISR has been reset, that interrupt request line is given lowest priority. The line with the highest priority is the IR4. As the IR4 bit in the Interrupt Request Register (IRR) is not set, the PIC proceeds to deal with IR5. If a new, unmasked interrupt request appears at IR3, and assuming no further unmasked interrupts appear at IR6, IR7, IR0, IR1, and IR2, the new interrupt at IR3 will be dealt with after IR6 has been serviced.

Non-specific EOI with rotation in automatic End-of-Interrupt mode (see ICW4) can be achieved by issuing OCW2 with only bit R set (OCW2=80H). This is interpreted by the PIC as "rotate on automatic EOI", which remains in force until cleared by issuing OCW2 with all bits zero.

OCW2 can be used to set a specific priority. In this case, bits R and SEOI must be set, and the binary value of the interrupt request which is to have the lowest priority must be encoded in D2-D0. For example, if D2-D0 contain the value 4, the interrupt request with the highest priority is now 5, the interrupt request with the second highest priority is 6, and so on. This command does not actually issue an End-of-Interrupt. If an EIO is required at the same time, all three bits R, SEIO, and EIO must be set. The IR line specified in D2-D0 is then set to lowest priority, and its ISR bit is reset.

Figure 2.11 gives a summary of the various commands effected by the bits R, SEIO, and EOI.

D7 .. R	D6 .. SEOI	D5 .. EOI	
0	1	0	No operation.
0	0	0	Clear "rotate on automatic EOI" mode.
1	0	0	Rotate on automatic EOI.
0	0	1	Non-specific EOI.
0	1	1	Specific EOI.
1	0	1	Rotate on non-specific EOI.
1	1	0	Set priority.
1	1	1	Rotate on specific EOI.

Figure 2.11 Priority and termination

OCW3 is available for setting a special mask mode and reading PIC registers. OCW3 is illustrated in Figure 2.12.

	D7	D6	D5	D4	D3	D2	D1	D0	via Port
OCW3	0	SME	SM	0	1	PO	RREG	REG	20H/0A0H

Figure 2.12 Operation command word 3

SME, if set, tells the PIC to set or cancel a special mask: bit SM set then means set, bit SM means cancel the special mask. If SME is zero, SM is "don't care".

The setting of a special mask gives your software the possibility of temporarily enabling interrupts of lower priority which are currently disabled. To set a special mask, issue OCW3 with both SME and SM set. From then on every interrupt request whose bit in the Interrupt Mask Register is not set, is enabled, irrespective of nesting priority. The special mask can be changed as often as you wish by means of OCW1. The former priority scheme is restored by means of a further OCW with SME set and SM zero.

PO, if set, acts as a Polling command. Your software can use this command to detect interrupts while the microprocessor interrupt flag is cleared. The next RD/ signal to the PIC with address line A0 at logical 0 (IN from Port 20H/0A0H) causes the PIC to place the following information on the data bus:

D7	D6	D5	D4	D3	D2	D1	D0
INT	-	-	-	-	Int. Request		

Figure 2.13 Interrupt polling

If INT is zero, there is no interrupt waiting to be serviced. If INT is set, at least one interrupt is waiting to be serviced. The number of the highest priority interrupt waiting for service is represented as a 3-bit binary value in D2-D0.

RREG and REG enable your software to read the PIC registers IRR and ISR. To read one of these registers, RREG must be set. Which of these two registers is to be read is determined by REG: if REG is set, ISR is to be read, otherwise IRR. The next RD/ signal with address line A0 at logical 0 (IN from Port 20H/0A0H) causes the PIC to place the contents of the selected register on the data bus.

It is not necessary to repeat OCW3 for successive reading of the same register. The PIC remembers which of the two registers ISR and IRR was last read.

However, after placing interrupt information on the data bus by means of the PO command in OCW3, a new OCW3 is required before ISR or IRR can be read. Following initialization of the PIC, IRR is the register automatically selected for reading.

In the event that OCW3 contains both a Polling command and a read PIC register command, the Polling command overrides.

OCW3 is not used for reading the interrupt mask register (IMR). Instead, the contents of IMR are placed on the data bus when the PIC receives a RD/ signal and address line A0 is at logical 1 (IN from Port 21H/0A1H).

PIC: ROM BIOS Initialization

The following CPU instructions summarize the way in which the two PICs are initialized by the ROM BIOS of your NCR PERSONAL COMPUTER:

```
;Initialize Master via ports 20H/21H.
;
    MOV   DX,20H
    MOV   AL,11H      ;ICW1: edge triggered - ICW4 needed.
    JMP   SHORT $+2   ;Delay, see section "Recovery Time".
    OUT   DX,AL
    JMP   SHORT $+2
    INC   DX
    MOV   AL,8        ;ICW2: base interrupt is of type 8.
    OUT   DX,AL
    JMP   SHORT $+2
    MOV   AL,4        ;ICW3: slave is connected at IR2.
    OUT   DX,AL
    JMP   SHORT $+2
    MOV   AL,1        ;ICW4: normal EOI - no special priority
                      ;      scheme - CPU is 80286.
    OUT   DX,AL
;
;Issue Operation Command Word to mask all IRs.
;
    MOV   AL,CFFH     ;Mask all.
    JMP   SHORT $+2
```

```
    OUT  DX,AL       ;Address line A0=zero after ICW completion
                     ;means that OCW is OCW1 (for other OCWs
                     ;A0=1.

;
;
;Initialize Slave via ports 0A0H/0A1H.
;
    MOV  DX,0A0H
    MOV  AL,11H      ;ICW1: edge triggered - ICW4 needed.
    JMP  SHORT $+2
    OUT  DX,AL
    JMP  SHORT $+2
    INC  DX
    MOV  AL,70H      ;ICW2: base interrupt is of type 70H.
    OUT  DX,AL
    JMP  SHORT $+2
    MOV  AL,4        ;ICW3: slave identification is 2.
    OUT  DX,AL
    JMP  SHORT $+2
    MOV  AL,1        ;ICW4: normal EOI - no special priority
                     ;      scheme - CPU is 80286.
    OUT  DX,AL
;
;Issue Operation Command Word to mask all IRs.
;
    MOV  AL,0FFH     ;Mask all.
    JMP  SHORT $+2
    OUT  DX,AL       ;Address line A0=zero after ICW completion
                     ;means that OCW is OCW1 (for other OCWs
                     ;A0=1.
```

Signal Integrity

As already stated, an IR input signal must be present until the first interrupt acknowledgement from the microprocessor, irrespective of whether edge or level triggering is being used.

If the IR signal goes low before microprocessor acknowledgement, the PIC does not recognize a valid interrupt, but a signal is nevertheless recognized. This is particularly useful for detecting spurious noise on the IR lines.

If a non-valid interrupt request occurs, the PIC recognizes it as an IR7 signal. Your software for this interrupt type need only execute a microprocessor IRET instruction. In this way, the interrupt is ignored. If IR7 is being used for other purposes, your software can still distinguish between a genuine IR7 and a non-valid interrupt request: the non-valid interrupt request does not set ISR bit 7. Therefore, it is possible to detect a non-valid interrupt by examining ISR contents (read by means of OCW3) at the beginning of the interrupt service routine.

SYSTEM INTERRUPTS

Because the hardware interrupts, as well as a number of software interrupts, are already dedicated to specific functions of the NCR PERSONAL COMPUTER, a few words are necessary concerning your own application of these interrupts. Even the PIC #2 interrupt requests 0AH - 0CH (that is, interrupt types 72H - 74H) should be regarded as reserved for further system expansion.

There are two possible ways of using the 8259A interrupt requests for your own applications. One possibility is to write the address of your own interrupt service routine directly into the four vector bytes from which the 8259A interrupt fetches its interrupt service routine address. This has the disadvantage of denying the ROM BIOS access to its important system-maintaining routines. If you are going to do this, you will need to include routines to replace those which have now been by-passed, and to return to the interrupting level by means of a PIC non-specific End-of-Interrupt command.

To make life easier, the ROM BIOS has provided the possibility of adding your own interrupt service routines to those already implemented by the system for the timer and keyboard hardware. During the ROM BIOS service routines for timer (type 8) and keyboard (type 9), a software interrupt is issued: type 1CH for the timer, type 1BH for the keyboard. The addresses placed by the ROM BIOS in the interrupt vectors for these two interrupts (at 70H and 6CH, respectively) simply refer to a dummy IRET instruction at a ROM location. To address an interrupt service routine of your own for one of these interrupts in read/write memory, you need only write the CS+IP address into the interrupt vector at the appropriate location. Note that while the interrupt vector is being written, hardware interrupts must be disabled (CLI instruction). This prevents the interrupt vector entry from being read by the CPU until both words are written and the address is therefore good. Routines accessed in this way need only be concluded by an IRET instruction. The 8259A End-of-Interrupt is supplied upon return to the ROM BIOS routine.

Remember that disk operating system software may write these interrupt vector positions for interrupt service routines loaded from disk.

The Non-Maskable Interrupt (NMI) is maskable via the I/O address 70H. The interrupt is masked is as long as bit 7 at this address is zero. To enable the NMI it is necessary to set this bit. The ROM BIOS enables the NMI.

The NMI is issued in the event of an I/O device error, a RAM parity error, or any other event which drives the I/O CH CHK/ line active.

DIRECT MEMORY ACCESS

Data transfer between disk drives and random access memory is performed with the assistance of two 8237 DMA controllers. The advantage of DMA transfer is that the system microprocessor (CPU) need specify only the initial RAM address, the number of bytes to be transferred, and certain items of control information, whereupon the transfer can take place without the CPU having to manage the transfer on a byte-by-byte basis. Bus arbitration prevents the data and addresses on the system busses being read by the CPU as part of its program. Obviously, the CPU cannot make use of the busses for read/write operations while the DMA transfer is in progress, but it can still perform internal arithmetic as well as processing instructions already waiting in its internal instruction queue.

The DMA controller can manage up to four channels, for which two types of priority logic can be set. In principle, any suitable peripheral device can be serviced by DMA. It is even possible to perform memory to memory transfers.

SYSTEM INTEGRATION

The pin configuration and internal logic of the 8237 are shown in Figure 2.14. The 8237 pin connections have the following significance:

Vcc
Power supply + 5V.

Vss
Ground.

CLK Input
Clock signal controlling internal functions and the data transfer rate.

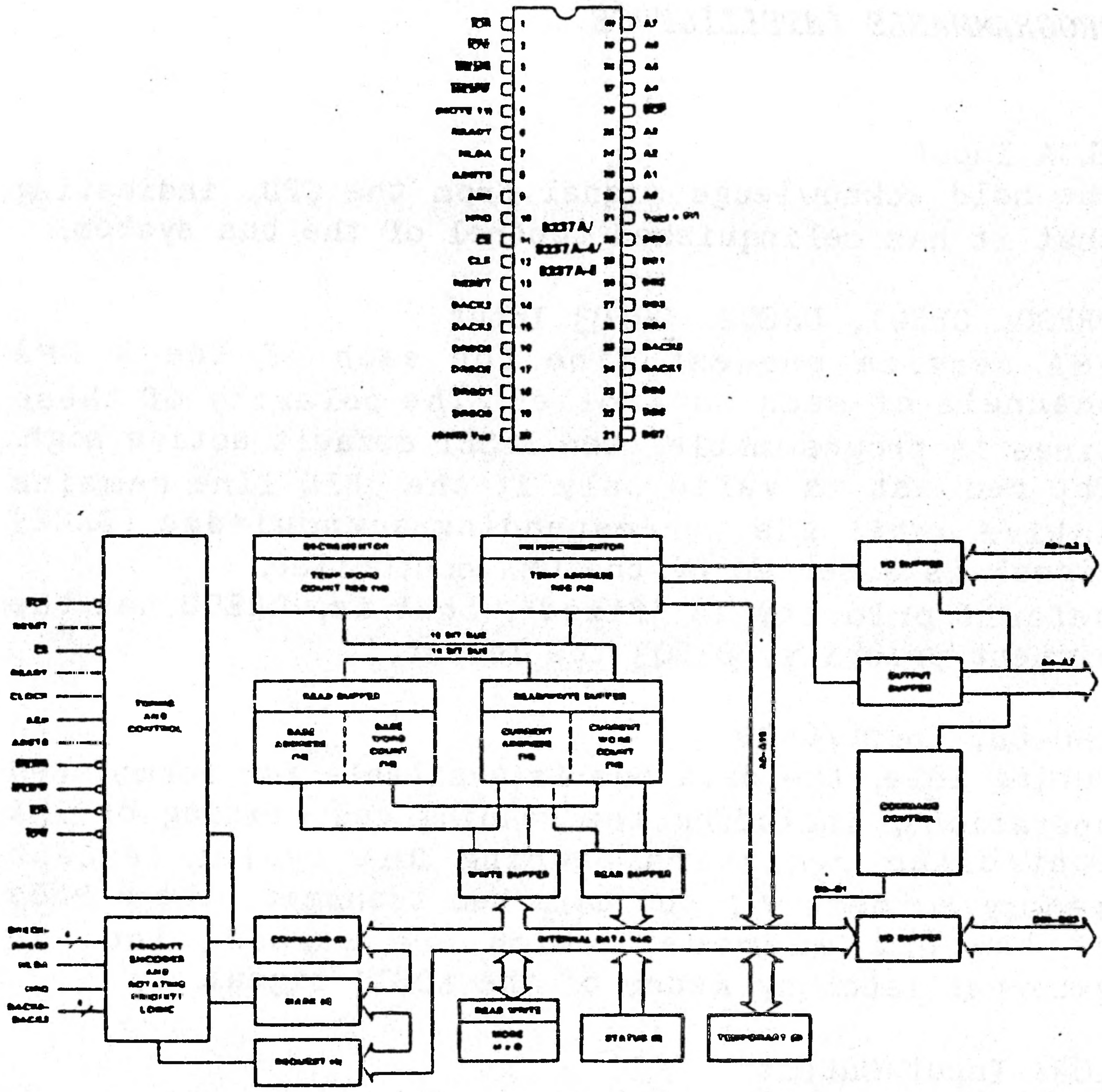


Figure 2.14 DMA controller overview

CS/ Input
Selects the DMA controller as a normal I/O device during its idle cycle. This allows the CPU to use the bus system (and program the DMA controller).

RESET Input
Clears the Command, Status, Mask, Request and Temporary registers (described in later section), as well as the first/last flip-flop. Following a reset, the DMA controller is in the idle cycle.

READY
Memory read/write puses are extended for the duration of this signal.

HLDA Input
The hold acknowledge signal from the CPU, indicating that it has relinquished control of the bus system.

DREQ0, DREQ1, DREQ2, DREQ3 Input
DMA service request line for each of the 4 DMA channels of each controller. The polarity of these lines is programmable, the RESET default active high. The request is valid only if the DREQ line remains active until the corresponding acknowledge (DACK) signal is asserted by the DMA controller.
Default priority is "fixed", that is, DREQ0 has the highest priority, DREQ3 the lowest.

DB0-DB7 Input/Output
During idle, the data bus is available for normal CPU operations, including the reading and writing of DMA controller registers. During DMA cycles (except memory to memory), the data bus transmits the 8 MSBs of the DMA address, which are strobed into an external latch by means of the ADSTB signal.

IOR/ Input/Output
In the idle cycle, this is an input control signal used by the CPU to read the control registers. In the DMA active cycle, it is an output control signal used to accept data from the peripheral device during a DMA read.

IOW/ Input/Output
In the idle cycle, this is an input control signal used by the CPU to write the 8237 registers. In the DMA active cycle, it is an output control signal used to load data to the peripheral device.

EOP (End of Process or Terminal Count)/ Input/Output
This is a bi-directional signal which terminates a DMA transfer. The signal may be external, or it is asserted by the DMA controller itself to indicate that the terminal count for a DMA channel has been reached. When this signal goes active through internal or external cause, the DMA request is considered to have been serviced. If Auto-Initialize

is enabled, the Base registers are written to the current registers of the channel concerned. The Mask and TC bits of the channel status are set (with Auto-Initialize, the Mask bit is unaffected).

A0-A3 Input/Output
In the idle cycle, these system bus address lines select 8237 registers. During DMA activity they function as the 4 LSBs of the address of the RAM location to be accessed.

A4-A7 Output
In conjunction with A0-A3, these address lines provide the 8 LSBs of the RAM address to be accessed (the 8 MSBs are placed on the data bus).

HRQ Output
With this signal, the DMA controller requests bus control from the CPU. Assuming the request line is not masked and is of adequate priority, a DREQ input to the DMA controller results in assertion of the HRQ signal. HLDA is the acknowledgement signal from the CPU.

DACK0, DACK1, DACK2, DACK3 Output
The DMA controller uses one of these signals to grant a DMA request to a peripheral device. Like the DREQ lines, they can be programmed as active high or low. Reset default is active low.

AEN Output
The Address Enable signal enables the 8-bit latch containing the 8 MSBs of the RAM address to be placed on the data bus.

ADSTB Output
Strobes the 8 MSBs of the RAM address available on the data bus into an external latch.

MEMR/ Output
Active during DMA read or memory to memory transfer.

MEMW/ Output
Active during DMA write or memory to memory transfer.

THE 8237 REGISTERS

The I/O address area between 0 and 0FH is dedicated to the DMA controller #1, the area 0C0H-0DFH to DMA controller #2. Figure 2.15 illustrates the registers which are written or read in the form of a single byte. Other registers require or return a 16-bit word representing an address or counter value. In each case, two CPU input or output instructions are required in order to specify or read the complete value. For each register an internal first/last flip-flop keeps note of which half of the word is about to be read or written: if this flip-flop is in a zero condition, the byte on the data bus represents the 8 LSBs of the word, otherwise the data byte is the 8 MSBs. The 16-bit registers are shown in Figure 2.16.

An additional I/O address area (80H-8FH) is used for the selection of DMA pages. This is described in a separate section.

Direction	Port	Operation
IN	8/0D0H	Read Status Register
OUT	8/0D0H	Write Command Register
OUT	9/0D2H	Write Request Register
OUT	0AH/0D4H	Write Single Mask Register Bit
OUT	0BH/0D6H	Write Mode Register
OUT	0CH/0D8H	Clear First/Last Flip-Flop
IN	0DH/0DAH	Read Temporary Register
OUT	0DH/0DAH	Master Clear (= hardware reset)
OUT	0EH/0DCH	Clear Mask register
OUT	0FH/0DEH	Write All Mask Register Bits

Figure 2.15 8237 8-bit programmable registers

Direction	Port	Address/Counter Operation	Channel
IN	0/0C0H	Read Current Address	0
OUT	0/0C0H	Write Base and Current Address	0
IN	1/0C2H	Read Current Count	0
OUT	1/0C2H	Write Base and Current Count	0
IN	2/0C4H	Read Current Address	1
OUT	2/0C4H	Write Base and Current Address	1
IN	3/0C6H	Read Current Count	1
OUT	3/0C6H	Write Base and Current Count	1
IN	4/0C8H	Read Current Address	2
OUT	4/0C8H	Write Base and Current Address	2
IN	5/0CAH	Read Current Count	2
OUT	5/0CAH	Write Base and Current Count	2
IN	6/0CCH	Read Current Address	3
OUT	6/0CCH	Write Base and Current Address	3
IN	7/0CEH	Read Current Count	3
OUT	7/0CEH	Write Base and Current Count	3

Figure 2.16 8237 16-bit programmable registers

It is the responsibility of software initiating DMA to ensure that a DMA request is not granted while the DMA controller is being programmed. For example, it is important to prevent DMA from being performed on a channel for which half of a 16-bit address or counter value has not yet been appropriately written. This can be achieved by one of two methods: either mask the channel concerned, or disable the controller by setting bit 2 in the Command Register.

Command Register

This register is illustrated in Figure 2.17. It can be cleared by the Reset or Master Clear instructions.

Bits:							
7	6	5	4	3	2	1	0
DACK +/-	DREQ +/-	WS	PRTY	TIMING	ENABLE	CH 0 ADDR. H	MEM-MEM

Figure 2.17 DMA Command Register

Bits 7 and 6 determine the polarity of the DACK and DREQ signals (active low for DREQ is determined by setting this bit, active low for DACK requires a zero bit).

TIMING determines whether normal (0) or compressed (1) timing is active. The latter compresses the transfer time to 2 clock cycles (this is illustrated in the section "DMA Timing" in this Chapter). If compressed timing is selected, WS selects late (0) or extended (1) write selection.

PRTY is the priority scheme selection bit. Fixed priority (bit zero) means that DMA request priority is equivalent to the sequence of request lines, DREQ0 having the highest priority. Rotating priority has the effect that the DMA request most recently serviced assumes lowest priority and priority rotates.

ENABLE, when set, prevents the controller from entering DMA active mode. This command can be used to hold the controller in the idle state while the address and counter registers are being programmed. To re-enable the controller, write this bit as zero.

Bit 1 is the Channel 0 Address Hold bit. Setting this bit means that the same address is used for all transfers on this channel.

MEM-MEM set determines that a memory to memory transfer is to take place from the address specified for Channel 0 via the Temporary Register to the address specified for Channel 1 until the Current Count Register goes to OFFFFH.

Mode Register

Mode selection information can be specified for any one of the 4 DMA channels. The actual channel selected is encoded in two bits of this register.

7	6	5	4	3	2	1	0
Transfer Mode		ADDRESS INC/DEC	AUTO INIT	Transfer Direction		Channel Select	

Figure 2.18 DMA Mode Register

Transfer Mode is a value in 2 bytes specifying Demand Transfer (0), Single Transfer (1), Block Transfer (2), or Cascade (3).

In Single Transfer mode, only one transfer is made. The Current Address Register is then altered by 1 and the Current Count Register is decremented. Even if the DREQ line is still active at completion of the transfer, bus control is released to the CPU. If DREQ is then still active, a further transfer is performed, and so on. Therefore, there is at least one machine cycle between DMA transfers. If the Current Count Register decrements from 0 to OFFFFH (Terminal Count) and Auto-Initialize is programmed (bit 4), an Auto-Initialize then occurs.

Block Transfer mode transfers continuously until Terminal Count or an external End of Process signal, whereupon Auto-Initialize occurs, if programmed. For this transfer mode, the DREQ signal need remain active only until the corresponding acknowledgement (DACK) is received.

In Demand Transfer mode the transfer runs continuously until Terminal Count or an external End of Process signal occurs. If programmed, Auto-Initialize then occurs. During the transfer, the DREQ signal must be held active. If DREQ goes inactive, the transfer is suspended, but not terminated. Re-activating DREQ rseumes the transfer process.

The Cascade Mode also applies to the DMA controller configuration of the NCR PERSONAL COMPUTER. The two controller's communicate by means of Channel 4 of #2.

The ADDRESS INC/DEC bit determines whether the value in the Current Address Register is incremented (0) or decremented (1) after each transfer.

AUTO INIT, if set, enables the Auto-Initialize mode of operation. Auto Initialize can then take place following an End of Process or Terminal Count condition. During Auto-Initialize the original values of the Current Address and Current Count Registers are restored using the values held in the Base Address and Base Count Registers (the Base registers are not affected by DMA transfer operations).

The Transfer Direction value determines whether data is to be transferred to (1) or from (2) memory, or whether data is only to be verified (0). In the verify mode, memory is not actually affected.

The Channel Select value selects one of the DMA channels 0-3.

Request Register

Assuming that Block Transfer is selected in the Mode Register, the Request Register can be used to initiate a DMA transfer, as if a hardware transfer request had been received on DREQ line. The channel to which this "software" DMA request applies is selected by the binary value of the two LSBs written to this register, with Bit 2 set. If Bit 2 is zero when this register is written, the request is cleared (other bits are "don't care"). This type of DMA request is not subject to the Mask Register (see below), but it is subject to priority control. A Terminal Count or external End of Process signal terminates the transfer in the normal way.

Mask Register

This register determines which DMA requests are inhibited (masked). One of two registers can be used to mask DMA requests, namely, Write Single Mask Register Bit (port 0AH) and Write All Mask Register Bits (port 0FH).

Write Single Mask Register Bit selects a channel by means of the binary value in the 2 LSBs of that register; Bit 2 sets or clears the mask bit for the selected channel, bits 3-7 are "don't care".

Write All Mask Register Bits sets or clears the mask bits for Channels 0-3 according to the status of bits 0-3, respectively. Bits 4-7 are "don't care".

A Clear Mask Register command allows all four DMA requests.

In addition to these posssibilities of software control, the following signal conditions affect the Mask Register:

* A mask bit is set when its channel produces an End of Process condition, if that channel is not programmed for Auto-Initialize.

* A Reset inhibits all DMA requests.

Status Register

The Status Register is illustrated in Figure 2.19. This register states which channels, if any, have received DMA requests, and whether on individual channels Terminal Count conditions or external End of Process signals have occurred. Bits 0-3 are cleared immediately upon the register being read and at Reset. Bits 4-7 are set whenever service is being requested on the corresponding channel.

Bits:							
7	6	5	4	3	2	1	0
DMA Request on Channel:				TC/EOP on Channel:			
3	2	1	0	3	2	1	0

Figure 2.19 DMA Status Register.

Temporary Register

The Temporary Register always contains the last byte transferred in a memory to memory transfer operation. This register can be read with the Read Temporary Register Command (port 0DH/0DAH) and is cleared at Reset.

Current Address Register

This register is a running record of the address used for the byte currently being transferred. This address value is incremented or decremented (in accordance with bit 5 of the Mode Register) after each byte transfer. Auto-Initialize restores the programmed value.

Current Count Register

This register functions as a counter to limit tl number of bytes transferred. It should be programm with a binary value which is one less than the numb of transfer bytes. Terminal Count occurs as soon this register has decremented from zero to OFFFF Auto-Initialize restores the programmed value.

Base Address and Base Count Registers

These are the registers used by the DMA controller store the values programmed for the Current Addre and Current Count registers. These values a required by the controller in the event of an Aut Initialize. It is not required to program the Ba registers, as they are automatically set to t values of the Current Address and Current Cou Registers when the latter are programmed by the C It is not possible to read the Base registers und CPU control.

DMA TIMING

The Figures in this section illustrate the time-b co-ordination between the various signals involved DMA transfers.

Note that memory to memory transfers require a r and write phase.

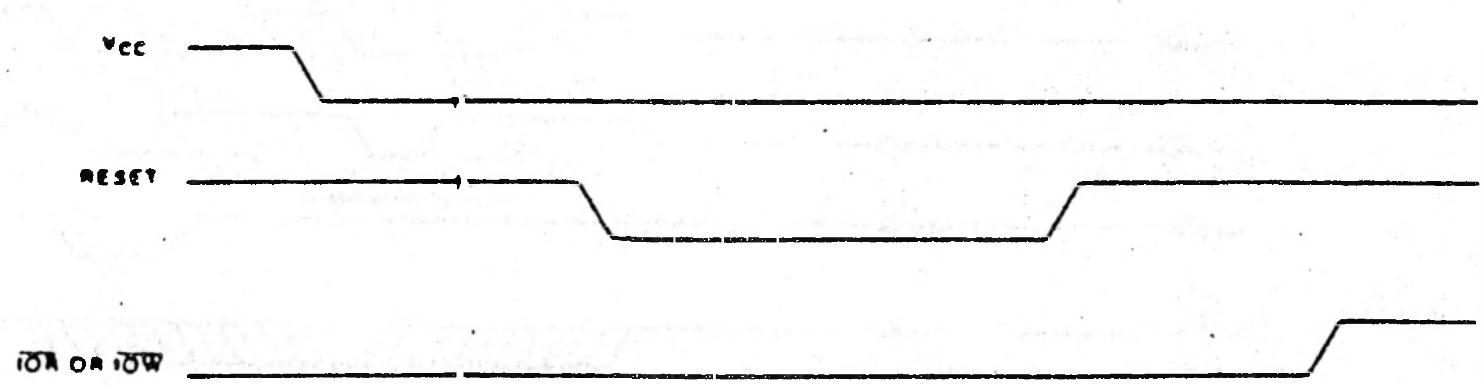


Figure 2.20 DMA Reset

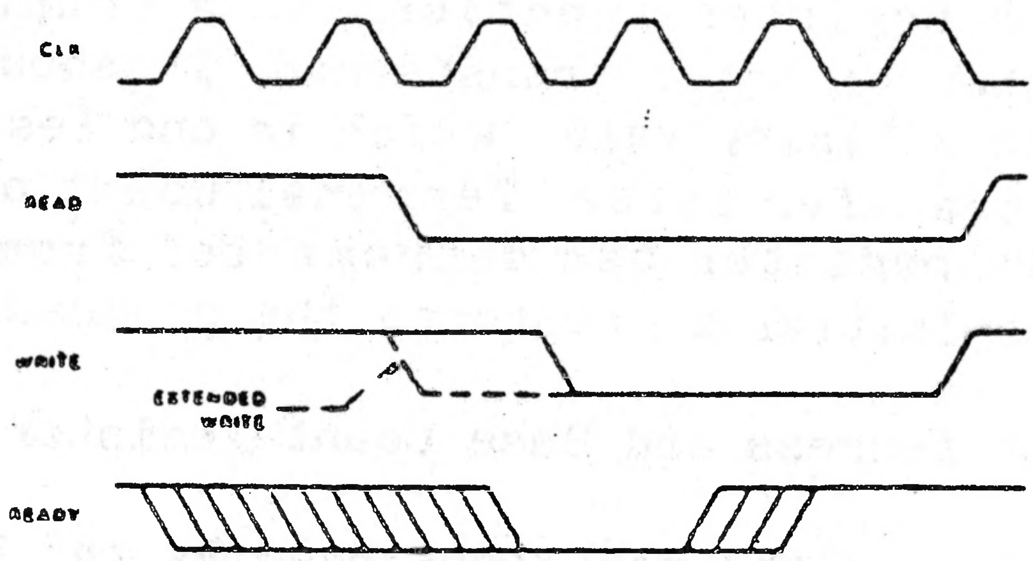


Figure 2.21 DMA Ready

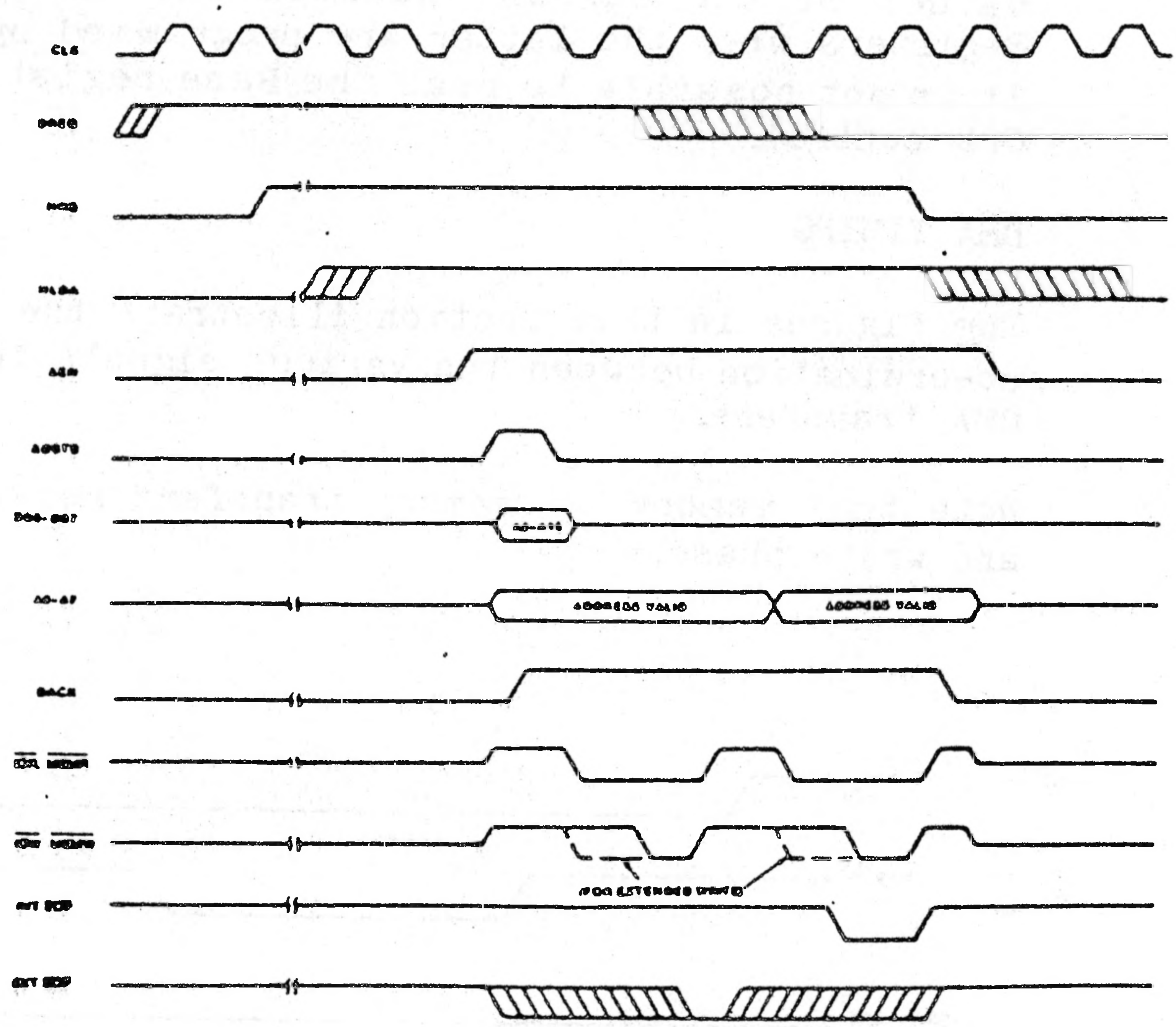


Figure 2.22 DMA transfer

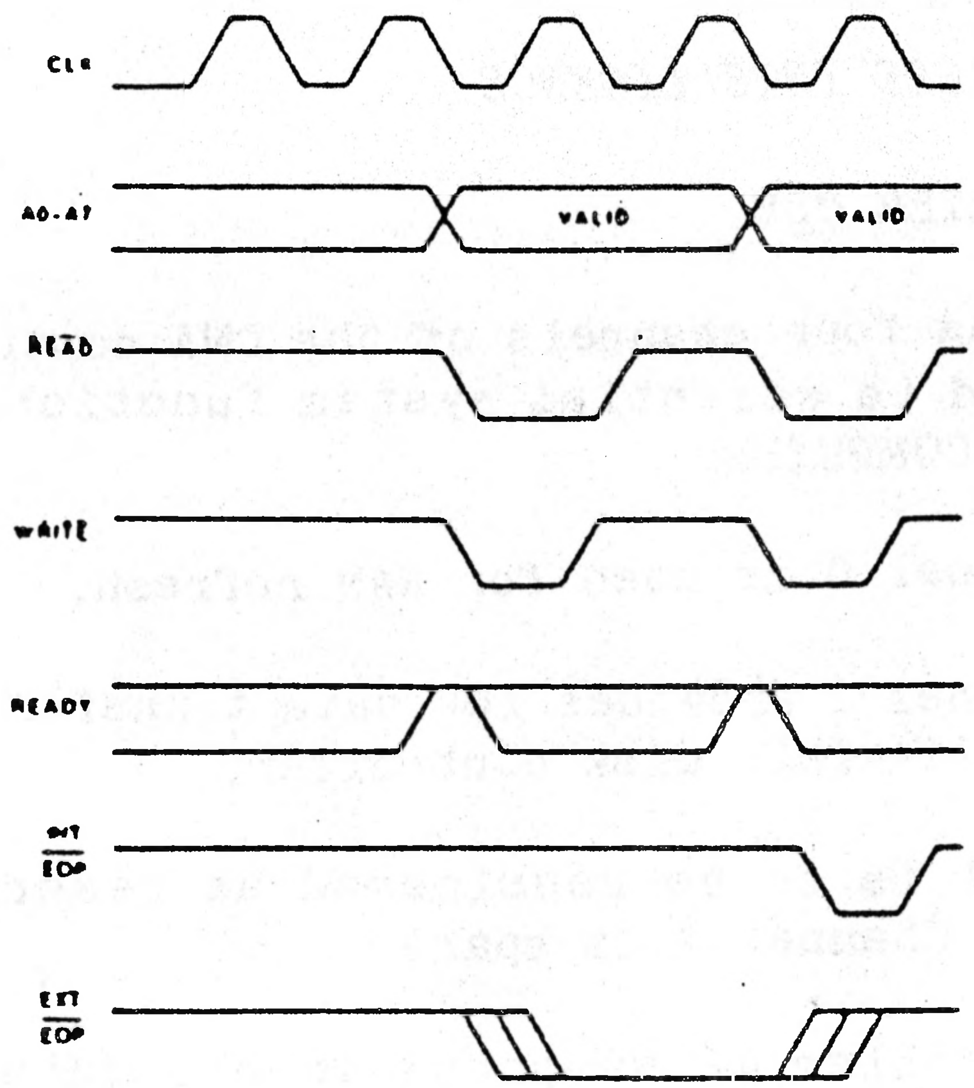


Figure 2.23 DMA compressed transfer

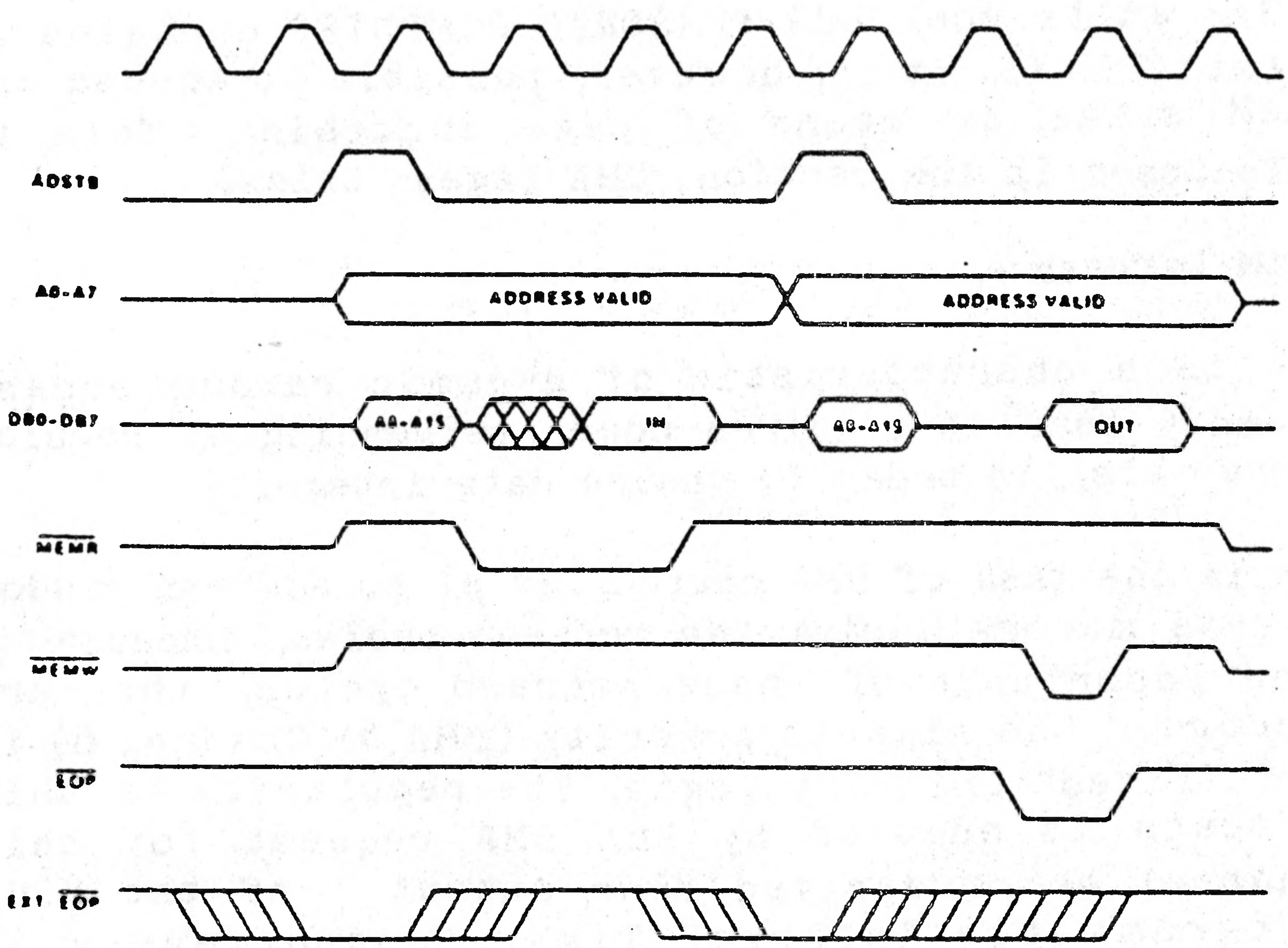


Figure 2.24 DMA memory to memory transfer

8237: SYSTEM USE

Two of the four channels of the DMA controller #1 are dedicated to essential system functions of the NCR PERSONAL COMPUTER:

* Channel 0 is used for RAM refresh.

* Channel 2 provides for data transfer to and from the flexible disk controller.

Channel 1 is to be considered as reserved for DLC purposes, Channel 4 is spare.

DMA controller #2 supports 16-bit data transfers, Channel 4 providing the cascade connection.

You will have noticed that the Address registers of the DMA controller are capable of addressing 64 KB of random access memory (#2 Channels 1-3 can address 128 KB), while your NCR PERSONAL COMPUTER contains at least 256 KB. It is, however, possible to access all RAM areas by means of page switching. This is discussed in the section "DMA Pages" below.

RAM Refresh

It is a characteristic of dynamic random access memory that it requires power refreshing at regular intervals, in order to ensure data integrity.

It is the task of DMA controller #1 to address random access memory during the refresh cycles. Because of the importance of these refresh cycles, they are accorded the highest priority (DMA #1 Channel 0) in the "fixed" priority logic. The regularity of this process is ensured by the DMA request for this channel being derived from output 1 of the 8253 Programmable Interval Timer (output every 14 microseconds). Due to way in which RAM integrated circuits are selected (see Schematics in Appendix A), the DMA controller does not have to provide fully decoded addresses. Therefore, there is no need for page switching during RAM refresh cycles.

After initialization by the system, RAM refresh requires no further CPU attention. However, you should take care not to disturb Timer 1 and DMA Channel 0 settings, as alterations might lead to loss of system control. It is also inadvisable to change the priority logic of the DMA controller, as this too could seriously impair the reliability of refresh cycle intervals.

16-bit Transfer

Channels 1 - 3 of DMA controller #2 support 16-bit transfer operations between 16-bit devices and memory. This controller is capable of accessing the entire 16 MB address space of the system in blocks as great as 128 KB, with the restriction that the transfer cannot start on an odd byte boundary. Bus lines SBHE and A0 are forced low for 16-bit transfers. The value written to a DMA Base register is then a word, not a byte address, and the Current Count register is similarly a word value.

DMA Page Selection

At first sight, it would seem that DMA controller activity is confined to a 64 KB (#2: 128 KB) block of memory, by virtue of the fact that programmable address values are 16-bit. To overcome this apparent limitation, your NCR PERSONAL COMPUTER includes page registers which allow memory to be regarded as a number of 64 KB (#2: 128 KB) blocks. However, it is not posible to define CPU-like "segments" at convenient paragraph boundaries. If the memory area you wish to access by DMA straddles one of these page boundaries, you will have to execute two DMA operations, of which the second specifies an incremented (or decremented) DMA page value.

The DMA page registers are 8-bit registers in the I/O map, as set outin Figure 2.25. Access to the full 16 MB address space requires 24 address bits (A0 - A23). The address is divided between page register and controller Channel as follows:

```
8-bit transfer
    controller         A0 - A15
    page register     A16 - A23

16-bit transfer
    controller         A1 - A16  (A0 is low)
    pageregister      A17 - A23  (reg. LSB unused)
```

DMA Controller/ Channel	I/O Addr. of Page Register
#1 0	87H
#1 1	83H
#1 2	81H
#1 3	82H
#2 1	8BH
#2 2	89H
#2 3	8AH
Refresh	8FH

Figure 2.25 DMA page registers

DMA: ROM BIOS Initialization

The following code illustrates how the DMA controllers are initialized by the ROM BIOS firmware. Note that spare Channels must also be initialized.

```
;
;Set command registers of #1 and #2.
;
      MOV   AL,0              ;Command Register:
                              ;DACK active low - DREQ active high -
                              ;write late - fixed priority - normal
                              ;timing - controller enabled - Channel
                              ;address not held - mem.—>mem. disabled.
```

```
        OUT     0D0H,AL         ;Write Command Register to #2.
        OUT     8,AL            ;                          #1.
;
;Set mode registers for #2 Channel 0 (Cascade).
;
        MOV     AL,0C0H         ;Mode Register:
                                ;Cascade - addresses increment - no auto
                                ;init - data verify - Channel is 0.
        OUT     0D6H,AL         ;Write Mode Register to #2.
;
;Set mode registers for other Channels on #1 and #2
;
        MOV     AL,40H          ;Single transfer - address increment -
                                ;no auto init - data verify - Channel 0
        OUT     0BH,AL          ;Write Mode Register to #1.
        MOV     AL,41H          ;Same to Channel 1.
        OUT     0D6H,AL         ;#2.
        OUT     0BH,AL          ;#1.
        MOV     AL,42H          ; ...... Channel 2.
        OUT     0D6H,AL         ;#2.
        OUT     0BH,AL          ;#1.
        MOV     AL,43H          ; ...... Channel 3.
        OUT     0D6H,AL         ;#2.
        OUT     0BH,AL          ;#1.
```

EQUIPMENT INFORMATION

A considerable amount of information concerning the machine configuration and status is software-readable. Examples of such information: the type of disk drive(s) installed, the amount of memory on the main processor board, the type of display being used.

Access to configuration and status information involves operations to

* the CMOS RAM, which is also accessed by the Real-Time Clock

* the 8042 Universal Peripheral Interface, whose main task is to function as the keyboard controller

CMOS RAM and the Real-Time Clock are described in a separate section in this Chapter, the keyboard in a separate Chapter.

CMOS RAM AND THE REAL-TIME CLOCK

The MC146818 is a single integrated circuit containing a Real-Time Clock and 64 bytes of CMOS RAM, of which the first 52 bytes are used. The CMOS RAM addresses are not part of the CPU memory map but are accessed as follows.

Write one byte of CMOS RAM:

```
MOV  AL,CMOS_ADDR     ;Number (0 - 33H) of byte.
OUT  70H,AL
MOV  AL,BYTE_DATA     ;Value to be written to selected byte.
OUT  71H,AL
```

Read one byte of CMOS RAM:

```
MOV  AL,CMOS_ADDR          ;Number (0 - 33H) of byte.
OUT  70H,AL
IN   AL,71H                ;Copy of byte now in AL.
```

REAL-TIME CLOCK

This section gives details of CMOS RAM bytes controlling the system clock and calendar. Figure 2.26 summarizes these 14 bytes.

CMOS Byte	Clock/Calendar Function
0	Seconds
1	Seconds alarm
2	Minutes
3	Minutes alarm
4	Hours
5	Hours alarm
6	Day of week
7	Day of month
8	Month
9	Year
0AH	Status Register A
0BH	B
0CH	C
0DH	D

Figure 2.26 Real-Time Clock CMOS addresses

The four Status registers are used as follows:

Reg.	Bit(s)	Significance
A	7	Set when the time is being updated i.e., reading time might produce an unreliable result. Otherwise zero, indicating that time can be read.
	4-6	A 22-stage divider to select one of eight time-base frequencies (010 sets 32.768 KHz).
	0-3	Selection of a divider output frequency for square wave and Real-Time Clock interrupts (0110 selects 1.024 KHz).
B	7	Set aborts any updating of time counters in progress, and inhibits counting until zero.
	6	Enables (set) or disables (zero) interrupts as programmed in Register A.

Reg.	Bit(s)	Significance
(B)	5	Enables (set) or disables (zero) alarm interrupts.
	4	Enables (set) or disables (zero) update-ended interrupt.
	3	Enables (set) or disables (zero) square wave as set in Register A.
	2	Selects binary (set) or BCD (zero) format fror time aend date storage.
	1	Selects 24-hour (set) or 12-hour (zero) format for hours counter.
	0	Enable daylight savings (1) or standard time (zero).
C	4-7	Read only flags used internally by the Real-Time Clock.
	0-3	Reserved.
D	7	This bit is set as long as the battery is providing sufficient power for the Real-Time Clock.
	0-6	Reserved.

EQUIPMENT AND STATUS

This section gives details of CMOS RAM bytes used for monitoring system configuration and status. Figure 2.27 summarizes these 38 bytes.

CMOS Byte (Hex)	System Use
E	Diagnostic Status
F	Shutdown Status
10	Flexible Disk Drive type
11	Reserved
12	Hard Disk Drive type
13	Reserved
14	Equipment
15	Base Memory (low)
16	Base Memory (high)
17	Expansion Memory (low)
18	Expansion Memory (high)
19-2D	Reserved
2E-2F	CMOS checksum
30	As 17
31	As 18
32	Date Century
33	Information

Figure 2.27 Equipment/status CMOS addresses

Address (Hex)	Bit(s)	Significance
E	7	0 = Real-Time Clock power is good 1 = loss of power to Real-Time Clock
	6	0 = checksum is good, 1 = checksum error
	5	0 = configuration info in CMOS inaccurate 1 = configuration info in CMOS reflects presence of at least one flexible disk drive and correct type display type
	4	0 = CMOS record of memory size is correct 1 = inaccurate CMOS record of memory size

Address (Hex)	Bit(s)	Significance
(E)	3	0 = hard disk drive initialization correct, so boot record can be read 1 = hard disk drive initialization error
	2	0 = time is valid, 1 = time is invalid
	0-1	Reserved
F	0-7	Used by power-on diagnostics.
10	4-7	0000 = no first flexible disk drive 0001 = 1st drive is double-sided (48 TPI) 0010 = 1st drive is high capacity (96 TPI) other values reserved
	0-3	0000 = no second flexible disk drive 0001 = 2nd drive is double-sided (48 TPI) 0010 = 2nd drive is high capacity (96 TPI) other values reserved
11	0-7	Reserved
12	4-7	0 = no first fixed disk drive <> 0 = one of fifteen possible types of first fixed disk drive (see Table)
	0-3	0 = no second fixed disk drive <> 0 = one of fifteen possible types of second fixed disk drive (see Table)

Address (Hex)	Bit(s)	Significance
(12)		

Type	Cyl.	Heads	Wr. pre-comp from cyl. ...	Landing on cyl...
0001	306	4	128	305
0010	615	4	300	615
0011	615	6	300	615
0100	940	8	512	940
0101	940	6	512	940
0110	615	4	none	615
0111	462	8	256	511
1000	733	5	none	733
1001	900	15	none	901
1010	820	3	none	820
1011	855	5	none	855
1100	855	7	none	855
1101	306	8	128	319
1110	733	7	none	733
1111 - reserved				

13	0-7	Reserved
14	6-7	00 = 1 flexible disk drive 01 = 2 flexible disk drives other values reserved
	4-5	Type of controller to primary display: 00 reserved 01 = graphics, 40 column mode 10 = 80 11 = character
	2-3	Not used

Address (Hex)	Bit(s)	Significance
(14)	1	0 = co-processor not installed 1 = co-processor installed
	0	0 = no flexible disk drives installed 1 = at least one flexible disk drive
15-16	0-15	0100H = 256 KB RAM on main process. board 0200H = 512 KB 0280H = 640 KB
17-18	0-15	Multiple of KB of expansion memory; max. value = 3A00H (for 14.5 MB)
2E-2F	0-15	Checksum of CMOS RAM addresses 10H-20H
30-31	0-7	Multiple of KB of expansion memory; max. value = 3A00H (for 14.5 MB)
32	0-7	Date century (BCD value)
33	7	0 = Upper 128 KB of possible 640 KB RAM on main processor board not installed 1 = installed
	6	Used by setup program
	0-5	Reserved
34-3F		Reserved

The ROM BIOS

If you require assembly language listings of the ROM BIOS, please contact your local NCR office.

The Keyboard

The keyboard is supplied with those keys already fitted, which have the same markings and the same position for all the country versions implemented. The remaining keys are fitted by the user from a set supplied for a specific version. Figure 4.3 shows the keys already fitted, Figure 4.4 shows the complete keyboards for the various country versions.

Special features of the keyboard are:

* Cursor movement keypad in addition to dual function cursor movement/ numeric keypad

* Tactile point of key 5 of the numeric keypad; deeper finger moulds on F and J keys

* 30 Function Keys

* Local toggling of keyboard status, independent of instructions from the main unit

* Auto-repeat and repeat delay times variable

* LED indication of status of NumLock, CapsLock, and ScrollLock keys - LEDs are extinguished at power-up initialization, so that unshifted (not shifted) and cursor movement (not digit) keys are active

* Tilting positions the keyboard in one of two possible planes: 5 and 12 degrees

* Slider switch enables use of keyboard with other types of NCR Personal Computer (not described in this Manual).

Connection to the NCR PERSONAL COMPUTER is via a screened 4-core cable. The cable is coiled over a length of approximately 600 mm (24"), the length of the uncoiled parts totals approximately 1150 mm (45"). The computer connection end of the cable is a DIN connector. The pin configuration is shown in Figure 4.1.

Pin	Color of wire	to PCB
5	green	5V
4	black	Ground
1	brown	Clock
2	white	Data
screen		Boundary line

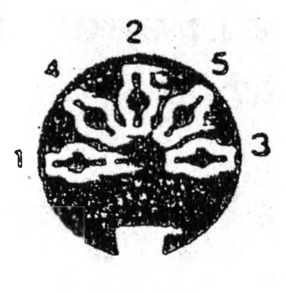


Figure 4.1 The keyboard connector

The working voltage for the keyboard is 4.75 V - 5.25 V, the maximum power drain is 250 mA. Required signal levels for Clock and Data are minimum 2.4 V (for high) and maximum 0.7 V (for low).

Data communication is clocked as illustrated in Figure 4.2. Logical levels of the data and clock signals are set out in Figure 4.3.

The bit stream of data communication is as follows:

Start bit (always 0)
8 data bits (LSB first)
Parity (completes to odd no. of data bits)
Stop bit (1)

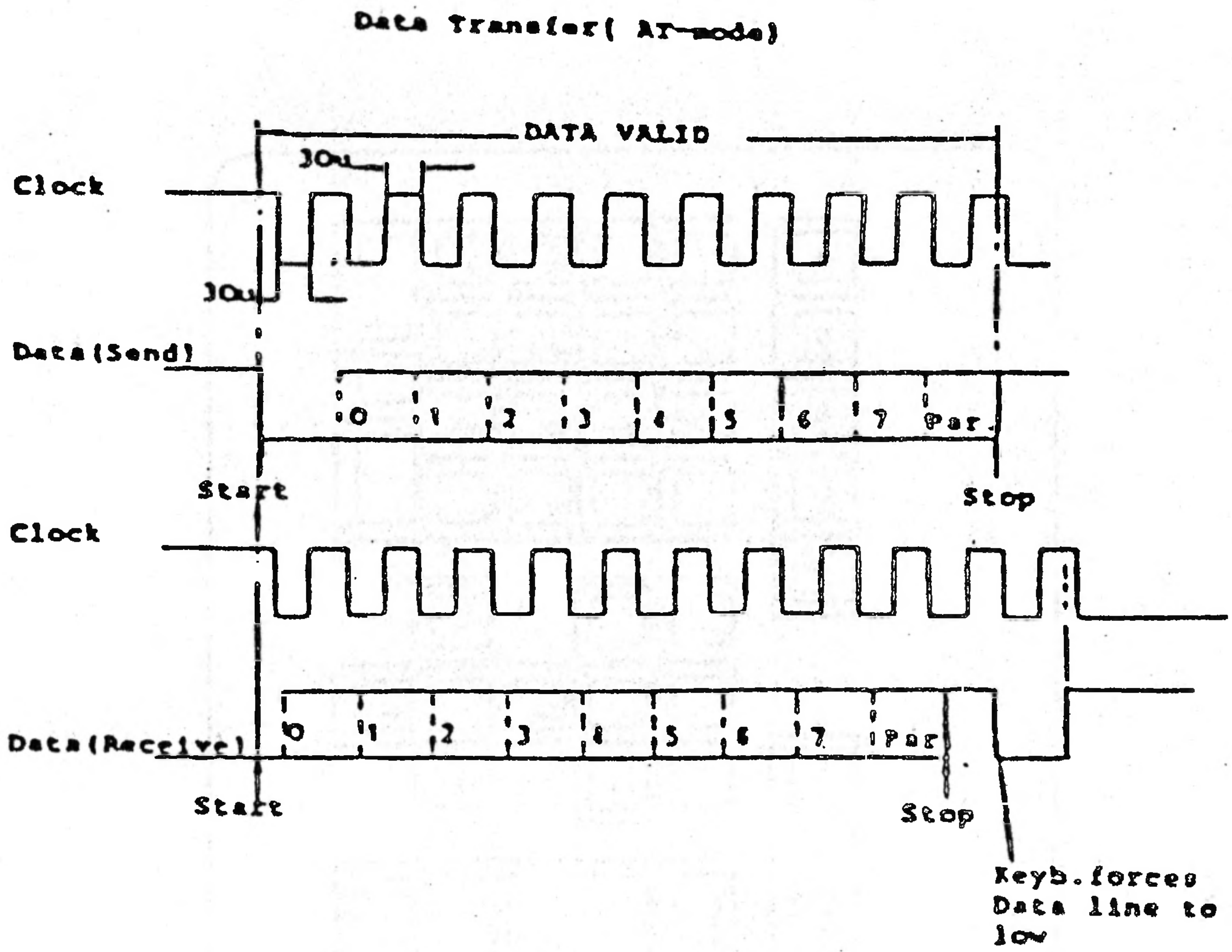


Figure 4.2 Data/Clock signals

Clock	Data	Keyboard Status	System Status	Notes
low	don't care	inhibit		no scanning
high	low	receive	req. to send	data stored in keyboard buffer
high	high	idle	idle	keyboard scans matrix (if enabled)
high to low	data bit stream	send	receive	data bit stream: start + data + parity + stop

Figure 4.3 Data/clock significance

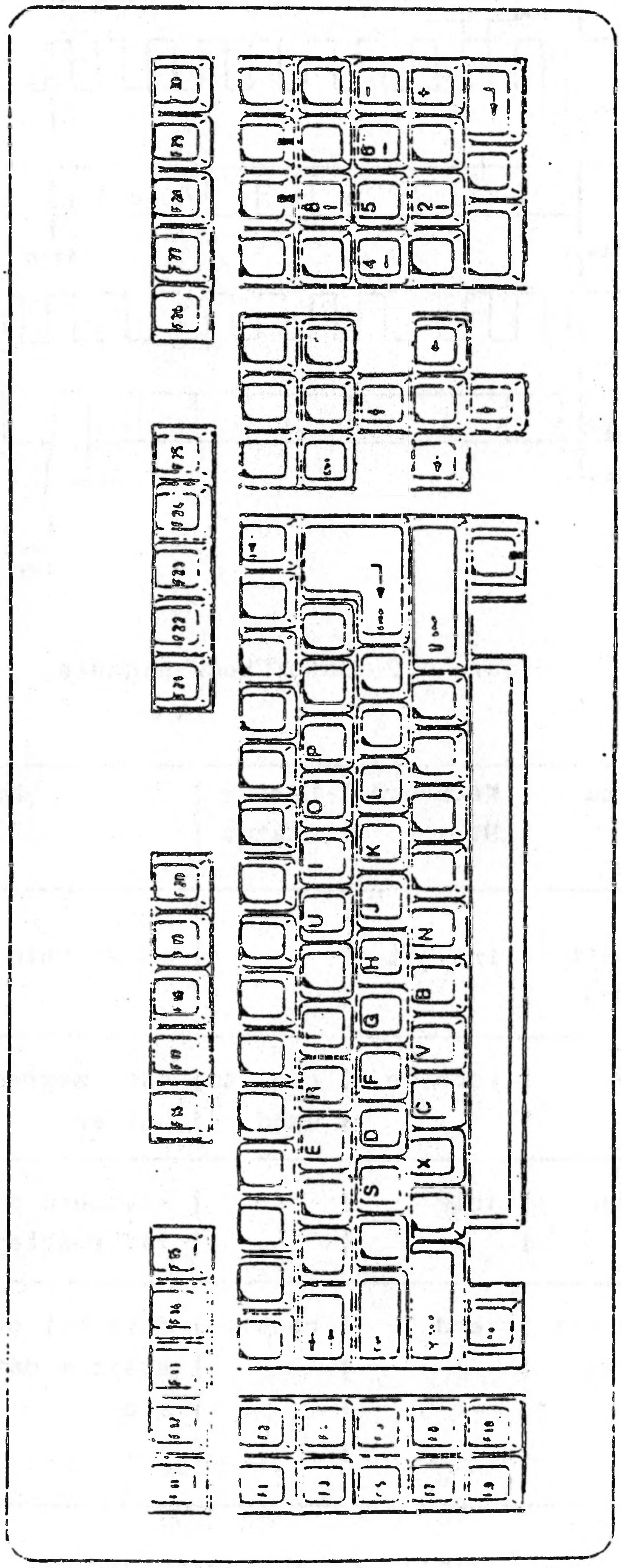


Figure 4.4 Keyboard - Common Keys

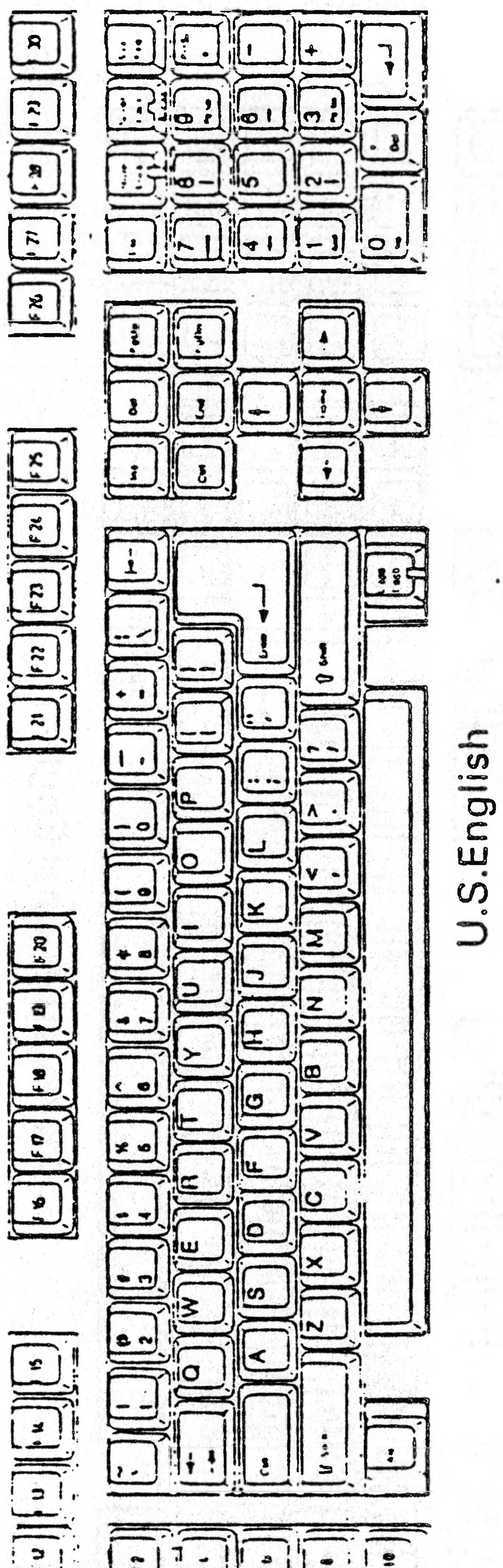


Figure 4.5 (1 of 9) Keyboard – US English

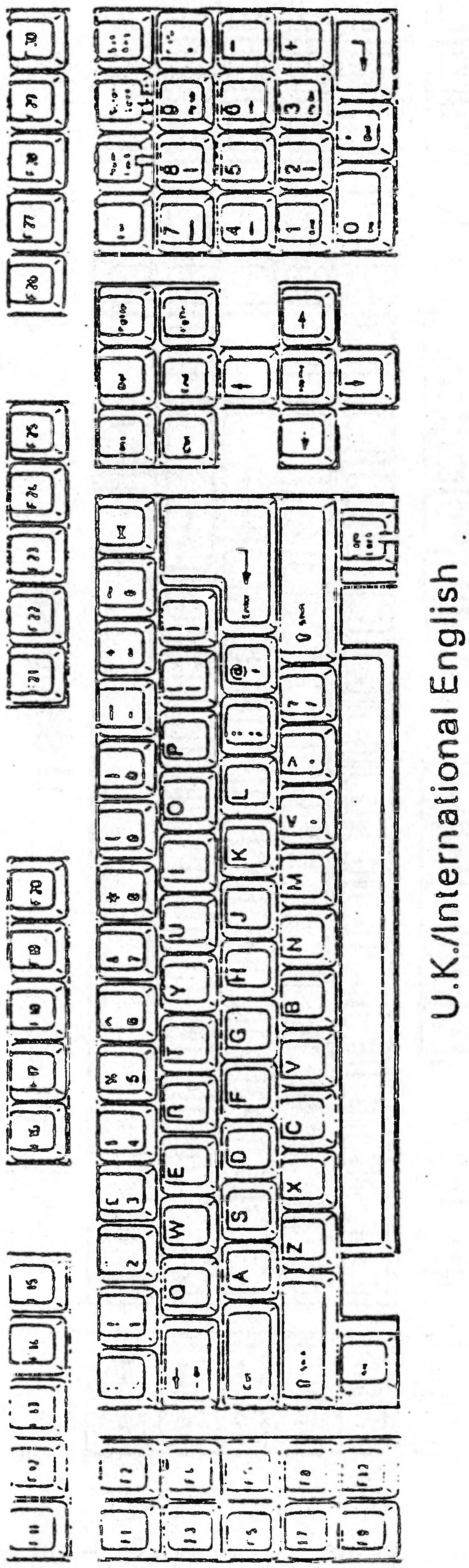


Figure 4.5 (2 of 9) Keyboard - UK English

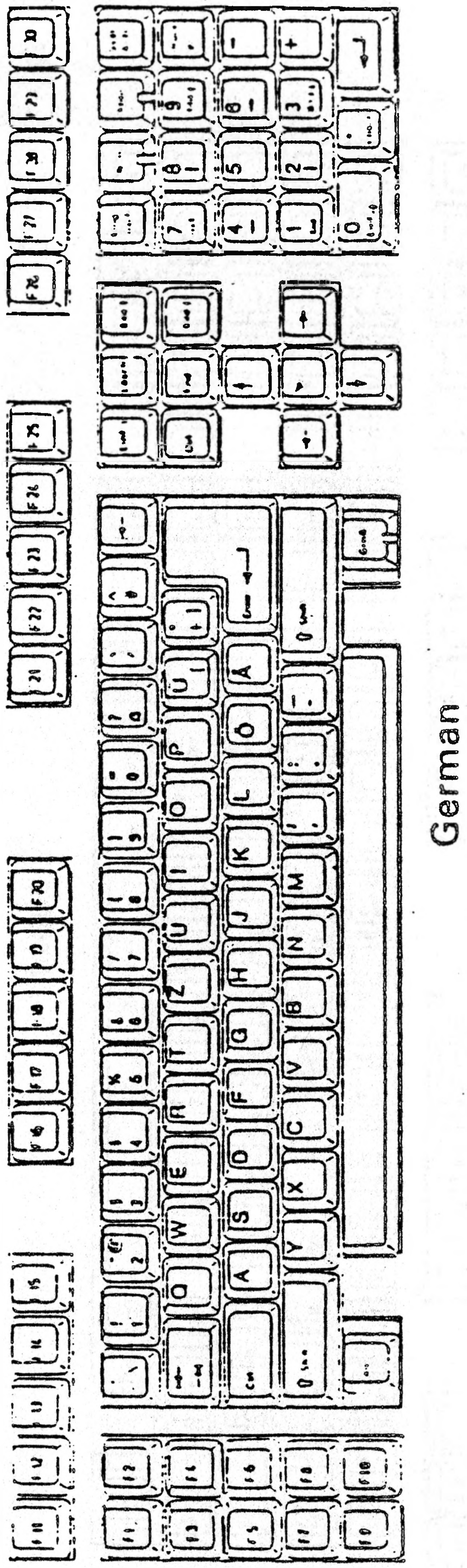
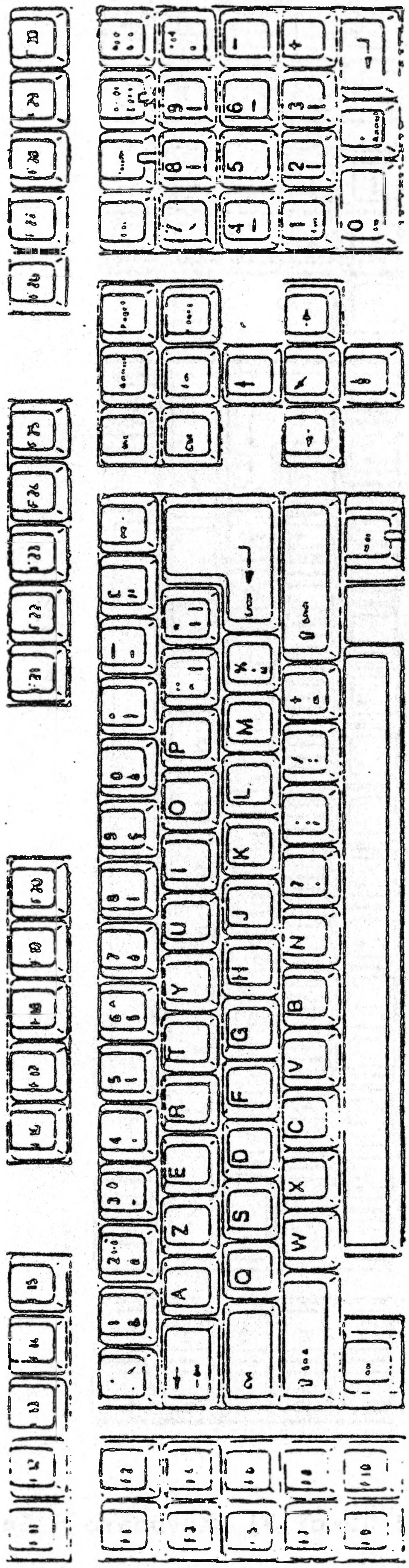


Figure 4.5 (3 of 9) Keyboard – German



French

Figure 4.5 (4 of 9) Keyboard - French

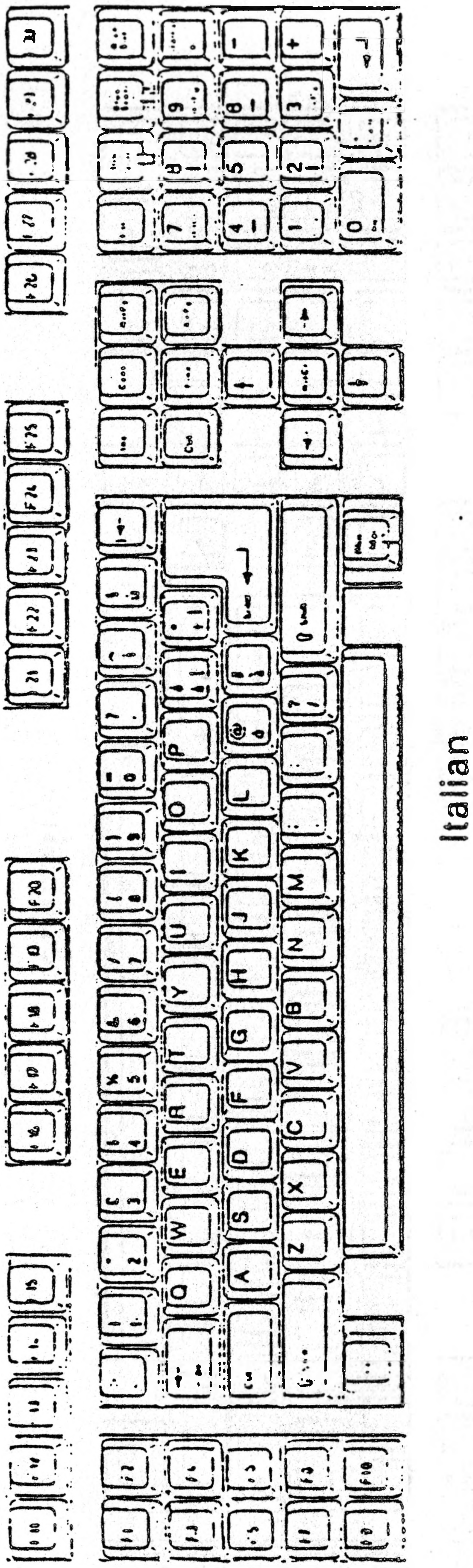
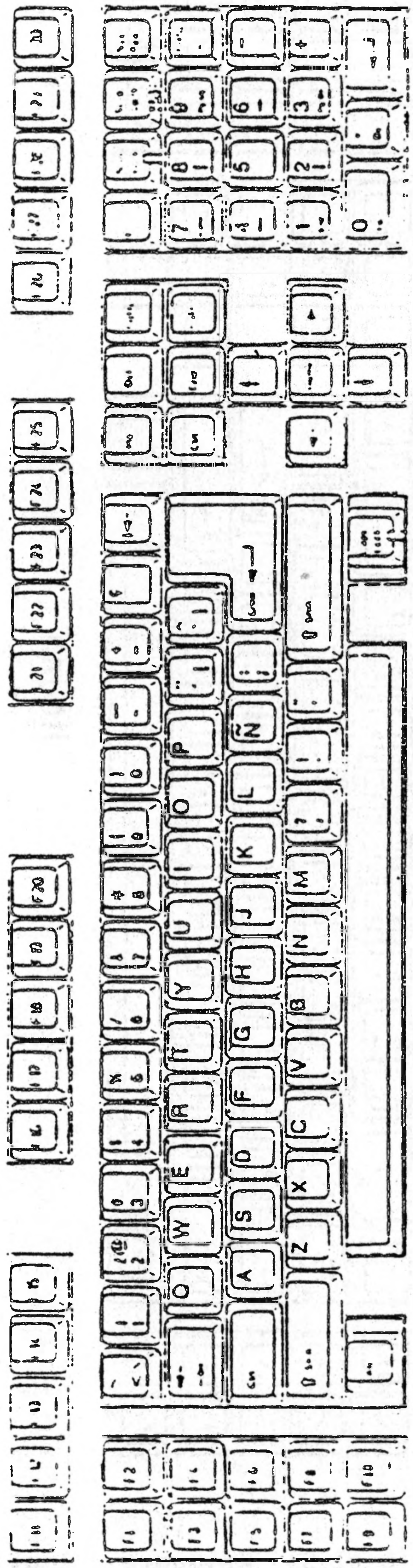


Figure 4.5 (5 of 9) Keyboard - Italian



Spanish

Figure 4.5 (6 of 9) Keyboard - Spanish

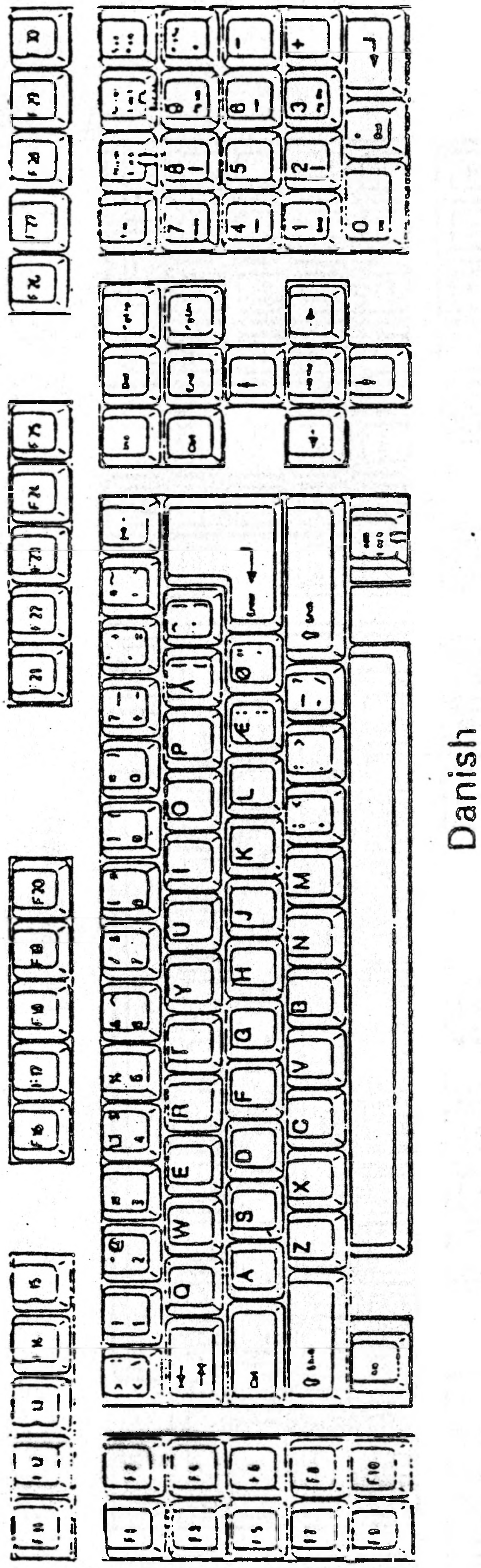


Figure 4.5 (7 of 9) Keyboard - Danish

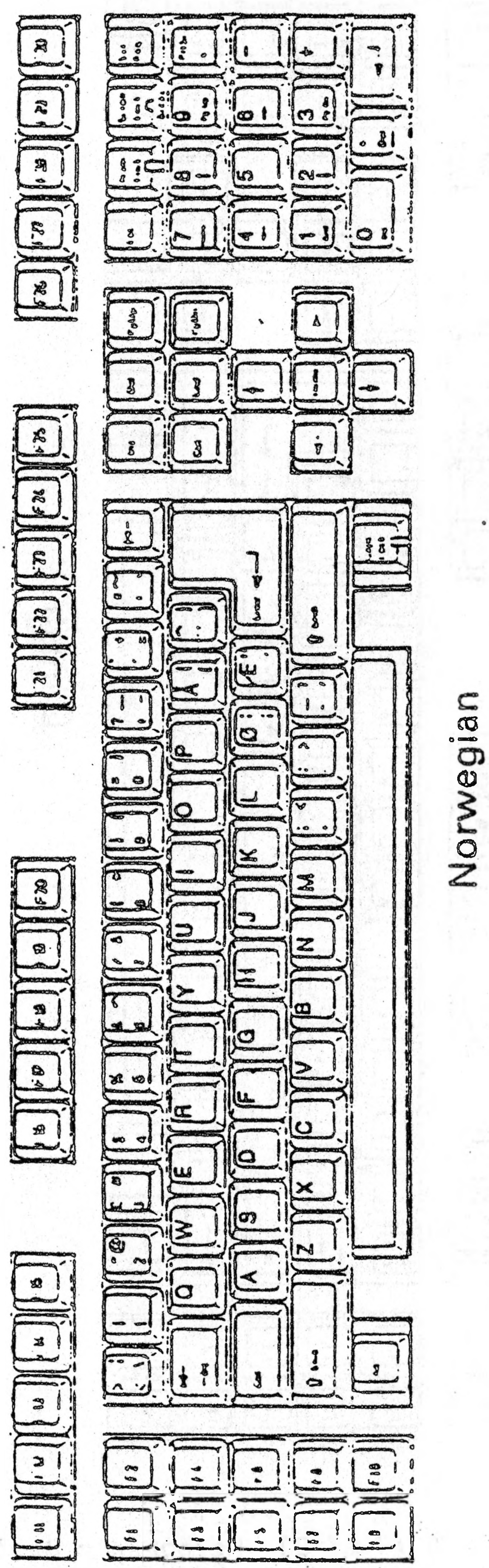


Figure 4.5 (8 of 9) Keyboard - Norwegian

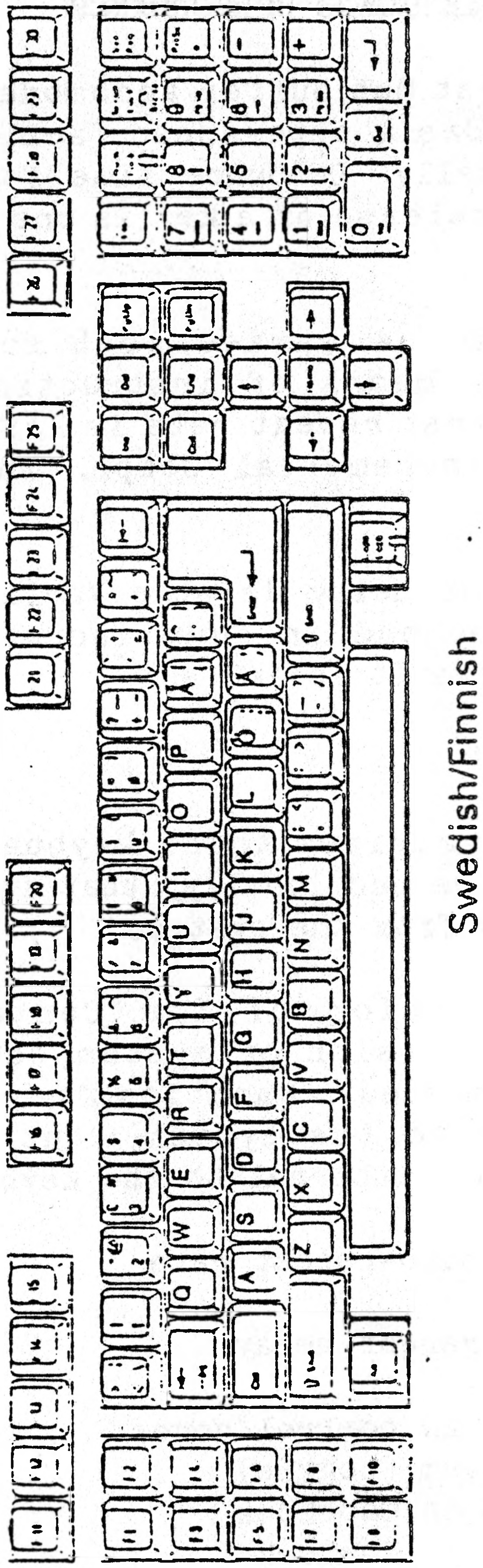


Figure 4.5 (9 of 9) Keyboard - Swedish/Finnish

KEYBOARD PERFORMANCE

A First In - First Out buffer accomodating up to 32 key codes provides a type-ahead facility. All keys repeat automatically. Debounce time for the initial depression and release of a key is one scan cycle (8 ms).

Auto-repeat can be varied both locally at the keyboard and by means of instructions from the system. The slowest repeat rate is 2/s, the fastest 30/s, with 32 incremental steps. Initialization default is 10/s.

The initial repeat delay is also variable - between 1/4 s and one second in four incremental steps. Initialization default is 1/2 s.

SPECIAL FUNCTIONS

This section summarizes those keyboard functions which can be influenced locally, that is, independent of codes received from the system.

Following depression of the Control-NumLock combination (suspension of system activity until another key is pressed), Function Keys F11 - F30 do not issue codes to the system, but take on the following functions internal to the keyboard:

F12	increment auto-repeat rate
F13	decrement
F14	increment repeat delay
F15	decrement
F16	disregard LED control codes from system (toggle)
F17	toggle LED on CapsLock
F18	NumLock
F19	ScrollLock

No special functions are assigned to F20 - F30.

As long as system activity is not suspended, F11 - F30 generate duplicate codes for F1 - F10:

F11 ... F20 = Shift-F1 ... Shift-F10
F21 ... F30 = Control-F1 ... Control-F10

KEYBOARD/SYSTEM COMMUNICATION

An 8039 or 8049 microprocessor controls generation of key codes for serial output to the main unit. The keyboard is also capable of receiving codes from the system. As already mentioned, codes are transmitted in a serialized form with start, parity, and stop bit.

CODES FROM THE SYSTEM

The following is a description one or two-byte codes recognized by the keyboard as valid instructions. Except where stated, codes elicit an acknowledgement code from the keyboard (see "Codes from the Keyboard"). An acknowledgement is also given between bytes of a two-byte sequence.

Code (Hex) First Byte	Bytes	Description
ED	2	Byte 2: bit 7 = 0 3-6 reserved 2 CapsLock LED on (1) or off (0) 1 NumLock 0 ScrollLock Note: if a key on 5-key cursor pad is pressed while numeric functions on numeric keyboard are active, the keyboard reverts internally to cursor functions on numeric keypad, but the NumLock LED is not directly influenced. Bit 1 is useful for "making good" this LED state

Code (Hex) First Byte	Bytes	Description
EE	1	Used as an "echo" code. Keyboard replies with its own echo code
F3	2	Byte 2: bit 7 = 0 5–6 repeat delay as binary value 0 = 0.25 s 1 = 0.5 s 2 = 0.75 s 3 = 1.0 s 0–4 auto-repeat as binary value
F4	1	Keyboard clears its output buffer and starts scanning the matrix
F5	1	Restores all power-on defaults, clears the output buffer, and suspends scanning until further instructions
F6	1	As F5, except that scanning continues (if enabled)
EF – F2 F7 – FD	1	Reserved "no operation" codes (an acknowledgement is issued by the keyboard).

Auto-repeat values (for F3, bits 0–4):

0	->30.0	11	->10.9	22	->4.3
1	26.7	12	10.0	23	4.0
2	24.0	13	9.2	24	3.7
3	21.8	14	8.6	25	3.3
4	20.0	15	8.0	26	3.0
5	18.5	16	7.5	27	2.7
6	17.1	17	6.7	28	2.5
7	16.0	18	6.0	29	2.3
8	15.0	19	5.5	30	2.1
9	13.3	20	5.0	31	2.0
10	12.0	21	4.6		

Code (Hex) First Byte	Bytes	Description
FE	1	Keyboard responds by repeating the last byte it transmitted. If this byte was its own repeat (re-send) code (see "Codes from the Keyboard"), the previous byte is transmitted
FF	1	Resets the keyboard. The keyboard performs its internal diagnostics.

CODES FROM THE KEYBOARD

Codes transmitted by the keyboard to the system can be single byte codes containing certain status information, or they can represent "data", that is, codes resulting from reading the keyboard matrix.

Status Codes

Code (Hex)	Description
00	Overflow of the type-ahead FIFO buffer
AA	Power-on completion - no errors
EE	Response to the system's echo command
F0	Key released, see "Keyboard Scan Codes"
FA	Acknowledgement to system
FC	Keyboard RAM or ROM error
FD	Keyboard matrix error
FE	Command received from system was invalid, or byte was received with incorrect parity

Keyboard Scan Codes

A code generated by reading the keyboard matrix represents a specific position on the keyboard; it does not conform directly to the ASCII code for the sign marked on the specific key. This means that the code returned for a key position is always the same, irrespective of country-dependent keys fitted.

Figure 4.6 shows the scan codes for the keyboard. A scan code is transmitted to the system when the key is depressed (after a pause for debounce time). When the key is released the same code is transmitted again, this time preceded by one byte of F0H. All these bytes are transmitted with start, parity, and stop bits as already stated at the beginning of this Chapter. Note that two codes are marked on each key: the actual code transmitted by the keyboard is the lower of the two. The upper codes conform to the codes generated for other NCR Personal Computers. They can be made available for software reading by special programming of the parallel I/O controller, which among other things, enables the CPU to communicate with the keyboard (see section below).

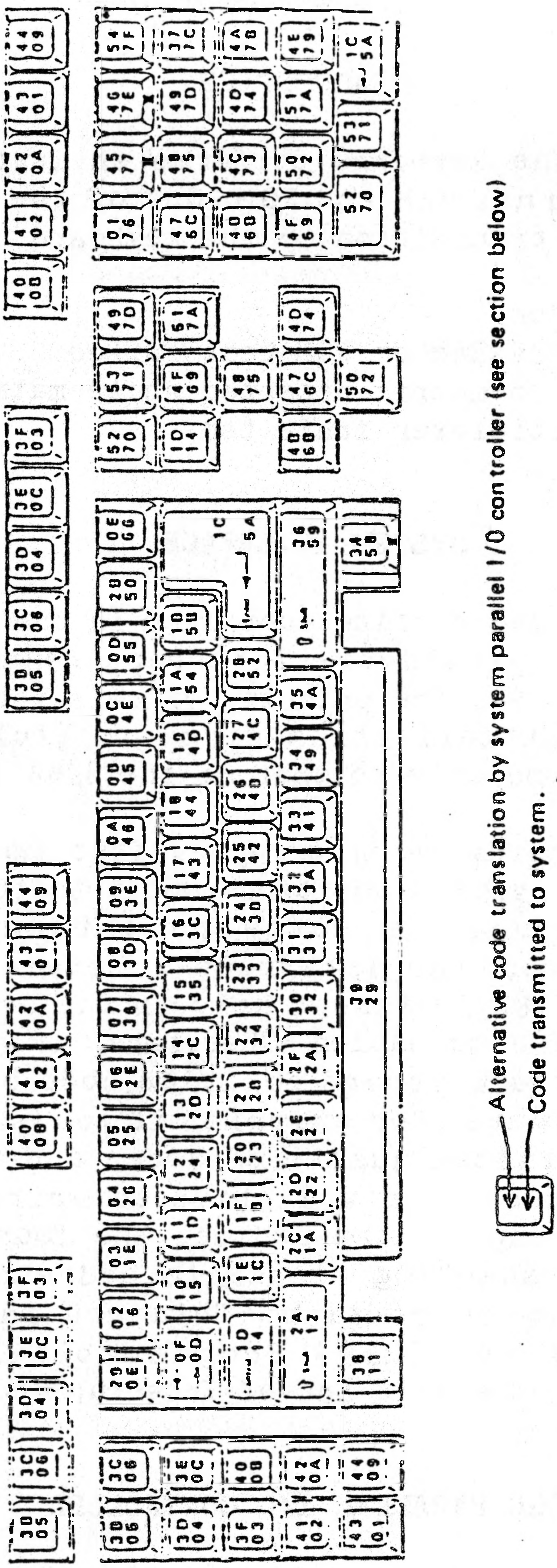


Figure 4.6 Keyboard scan codes

DIAGNOSTICS

At power-up the keyboard performs an initialization check of internal RAM and ROM. One of the following codes is then transmitted by the keyboard:

OAAH	No error
OFCH	Keyboard RAM or ROM test failed
OFDH	Error in matrix detected while matrix column de-multiplexer inhibited

SYSTEM INTERFACE

The keyboard read routine contained in the system ROM is activated by hardware interrupt request 1 (CPU interrupt type 9). The priority of this interrupt, as set by the initialization firmware (fully nested mode), is second only to that of the 8254 timer.

The keyboard hardware interrupt writes the character value of the keyboard position code into the keyboard buffer. There is a software interrupt (1BH) accessible from the interrupt 9 service routine. However, INT 1BH is issued only in the event of the Ctrl-Break key combination. Therefore, if you wish to interrogate the keyboard position code by means of your own software (for example, if you only want to check for a limited number of codes and ignore the keyboard buffer), you will have to write your own keyboard handling routine and set the four interrupt vector bytes starting at 6CH to address your own interrupt service routine. This routine must be concluded by the 8259A Progammable Interrupt Controller non-specific End-of-Interrupt command.

THE PARALLEL I/O CONTROLLER

The keyboard position code itself is read via the 8042 (or 8072) parallel interface in the I/O address map starting at port 60H (see Figures 4.7 and 4.8). The interface also includes system configuration and status information. Software accessible data/commands can be held in the following areas managed by the controller.

* A buffer holding data received from the keyboard, waiting to be read by the CPU at port 60H. A status bit indicates whether there is actually any data to be read

* A buffer holding data from the CPU, waiting to be fetched by the keyboard. A status bit indicates whether the data has been fetched, so that the CPU can send a further byte via port 60H

* An "input port" containing system configuration information. This "port" cannot be accessed directly in the system I/O map, but via commands to the controller

* An "output port" containing system control bits. This "port" also cannot be accessed directly in the system I/O map, but via commands to the controller. It should not normally be necessary to write to this port

* A "test input port" similar to the two described above

Commands to the controller and controller status are system accessible via port 64H of the system I/O map. Data is passed via port 60H. Scan codes received from the keyboard and held in buffer can be read at this port. Bytes can be written to buffer for the keyboard to fetch, provided that a command has not been issued to the controller telling it to expect data from the keyboard. A special command issued via port 64H tells the controller to read one of a sub-set of commands from port 60H.

IN/ OUT	Port (Hex)	Bit(s)	Description
IN	64		Read keyboard controller status
		0	1 = keyboard data waiting to be read by CPU, 0 = buffer empty
		1	1 = data waiting to be fetched by keyboard, 0 = buffer empty. Note: this bit must be zero before data (port 60H) or a command (port 64H) is sent to keyboard
		2	System flag, set by controller command 60H. Flag is zero at reset
		3	Used internally by controller to see whether byte written by CPU is data (= zero = port 60H) or command (= set = port 64H)
		4	0 = keyboard activity inhibited by switch on lock. Controller still communicates with keyboard, but data is not passed to/from the CPU
		5	1 = data could not be sent to keyboard before timeout occurred, or bit 6 or bit 7 is set
		6	1 = keyboard acknowledgement not received before timeout occurred
		7	1 = last byte from keyboard had even parity (= error), 0 = odd parity

Figure 4.7 Parallel I/O controller status

IN/ OUT	Port (Hex)	Value (Hex)	Description
OUT	64		Write command to keyboard controller
		20	Place last command byte issued in data buffer, so that it can be read by CPU via port 60H
		60	Instruct controller to interpret as a command the next byte placed by the CPU in the buffer (port 60H), see Figure 4.9
		AA	Perform controller's internal diagnostics, and return 55H in buffer at port 60H, provided that there is no error
		AB	Test keyboard clock and data lines, returning result in buffer (port 60H): 00 = no error 01/02 = clock stuck low/high 03/04 = data stuck low/high
		AC	Internal diagnostics
		AD	Disable keyboard (drive clock low)
		AE	Enable keyboard
		C0	Instruct controller to read contents of input port (see Figure 4.10) into buffer for reading by CPU (check status bit 0)

Figure 4.8 Parallel I/O controller commands (1 of 2)

IN/ OUT	Port (Hex)	Value (Hex)	Description
(OUT)	(64)		(Write command to keyboard controller)
		D0	Instruct controller to read contents of output port (see Figure 4.11) into buffer for reading by CPU (check status bit 0)
		D1	Write the next byte written to port 60H as the controller's output port (see Figure 4.11)
		E0	Read the controller's data and clock lines (see Figure 4.12), making this information available for CPU reading at port 60H
		Fx	Pulse the 4 LSBs of the output port (see Figure 4.11) in accordance with 4 LSBs of this command byte (x): zero means pulse, 1 means leave bit unchanged

Figure 4.8 Parallel I/O controller commands (2 of 2)

Bit	Description
0	1 = keyboard interrupt when byte waiting to be read at port 60H
1	Must be zero
2	Set/reset flag at controller status bit 2
3	1 = disable keyboard inhibit function (switch on keyboard lock inactive, see status bit 4)
4	1 = disable keyboard interface by driving clock low (see also controller commands ADH and AEH)
5	0 = interface is for enhanced (= PC8) keyboard
6	0 = scan codes as read direct from keyboard 1 = translated scan codes as used by ROM BIOS (for reasons of compatibility)
7	Must be zero

Figure 4.9 Sub-commands to controller command 60H

Bit	Description
0-3	Not used
4	Second 256 KB of RAM on main processor board is enabled (1) or disabled (0)
5	Not used
6	Primary display connected to graphics (0) or monochrome (1) display controller
7	Keyboard is inhibited (0) or not inhibited (1) by switch on lock

Figure 4.10 Controller input port

Bit	Description (bit set)
0	System reset
1	Gate A20 to access memory above 1MB
2-3	Unused
4	Activate buffer from keyboard full
5	Activate buffer to keyboard empty
6	Drive keyboard clock high
7	Drive keyboard data high

Figure 4.11 Controller output port

Bit	Description
0	Keyboard clock
1	Keyboard data
2-7	Not used

Figure 4.12 Controller test input port

Disk Storage

INTRODUCTION

Both flexible disks and hard (Winchester) disks can serve as disk storage for the NCR PERSONAL COMPUTER. Fixed disk capacity is at least 20 MB, diskette capacity is 1.2 MB (high capacity) or 320 KB/360 KB (standard capacity). Details of disk drive combinations installable in the NCR PERSONAL COMPUTER are given at the beginning of this Manual.

Both flexible and hard disk drives make use of the disk drive controller inserted in the system main processor board.

FLEXIBLE DISK DRIVES

Integrated in the computer are one or two 5 1/4-inch flexible disk drives to provide mass storage of programs and data. The drives contain read/write controller electronics, driver mechanics, read/write heads, and head positioning mechanisms.

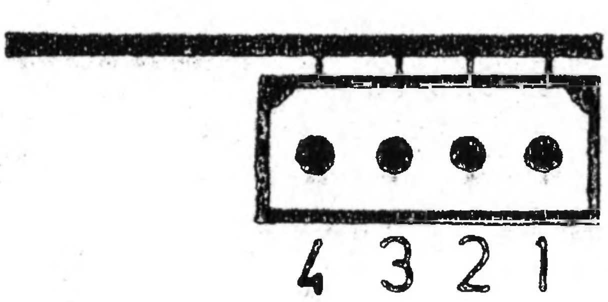
Flexible disk drives are connected in a daisy-chain configuration. A DIP resistor module provides the terminator in the last unit in the chain.

	Capacity	
	Standard	High
Tracks per inch (TPI)	48	96
Tracks per disk side	40	80
Unformatted capacity	500 KB	1.604 MB
Motor rotation speed	300 r.p.m	360 r.p.m
Motor start time	< 400 ms	< 500 ms
Head movement (track to track)	6 ms	3 ms
Average seek time	93 ms	94 ms
Latency time (at 300 r.p.m)	100 ms	83.3 ms
Data transfer rate	250 K bits/s	300 k bits/s
Data recording format	MFM	MFM
Power consumption (typical with disk rotating in drive)	12 Vdc 0.22 A 5 Vdc 0.3 A	12 Vdc 0.22 A 5 Vdc 0.35 A

Note: The high capacity drive is used in its high density, high speed mode of operation, giving a capacity (formatted: 15 sectors each 512 bytes/track) of 1.2 MB.

Figure 5.1 Flexible disk drive technical data

Power connections to the flexible disk drive are illustrated in Figure 5.2.

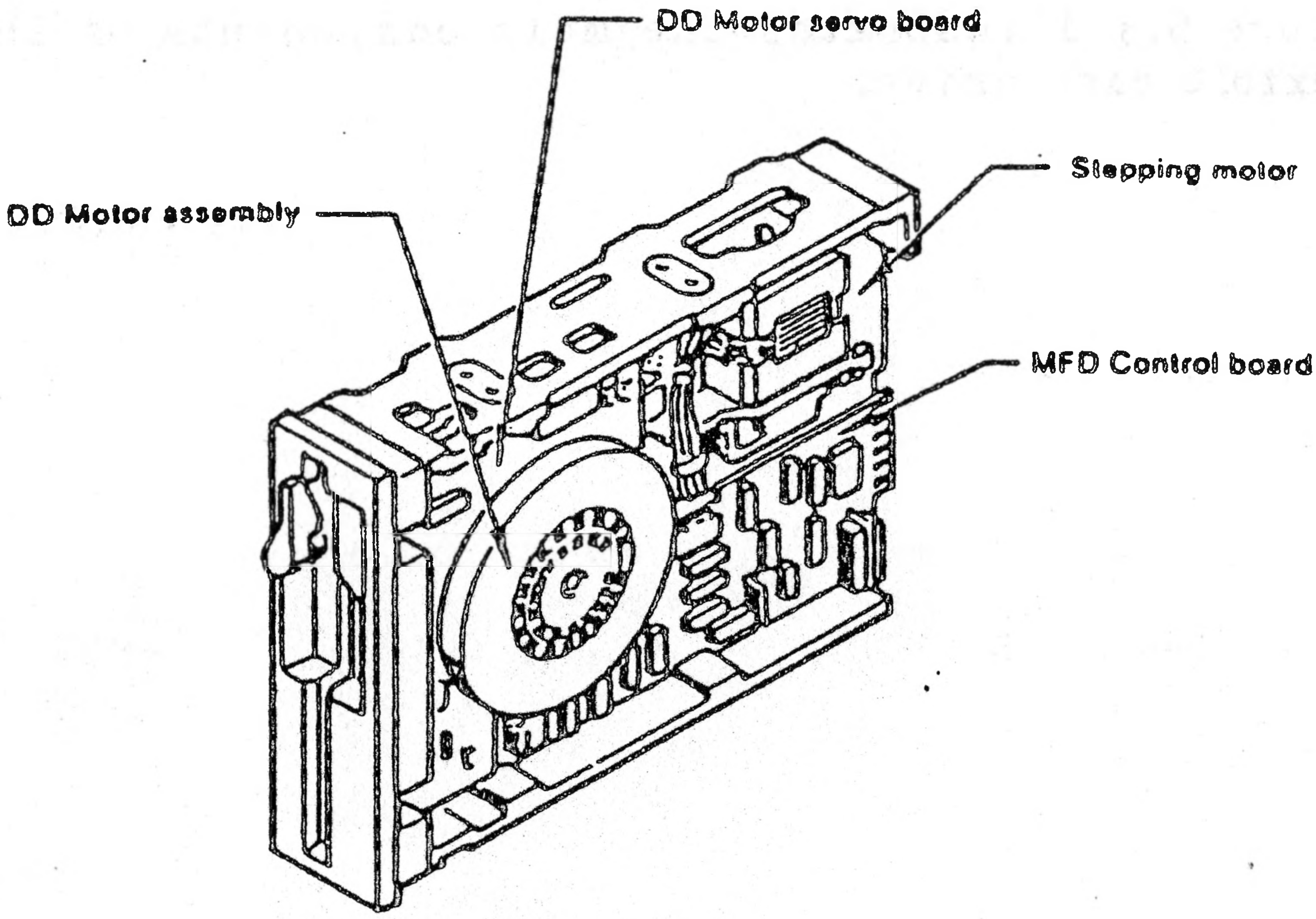


Pin	Voltage
1	+ 12 Vdc
2	Ground
3	Ground
4	+ 5 Vdc

Figure 5.2 Flexible disk drive power connections

The flexible disk drive contains sensors to detect the diskette index hole, the head at track 0, and whether the write protect notch is covered.

Figure 5.3 illustrates the main components of the flexible disk drive.



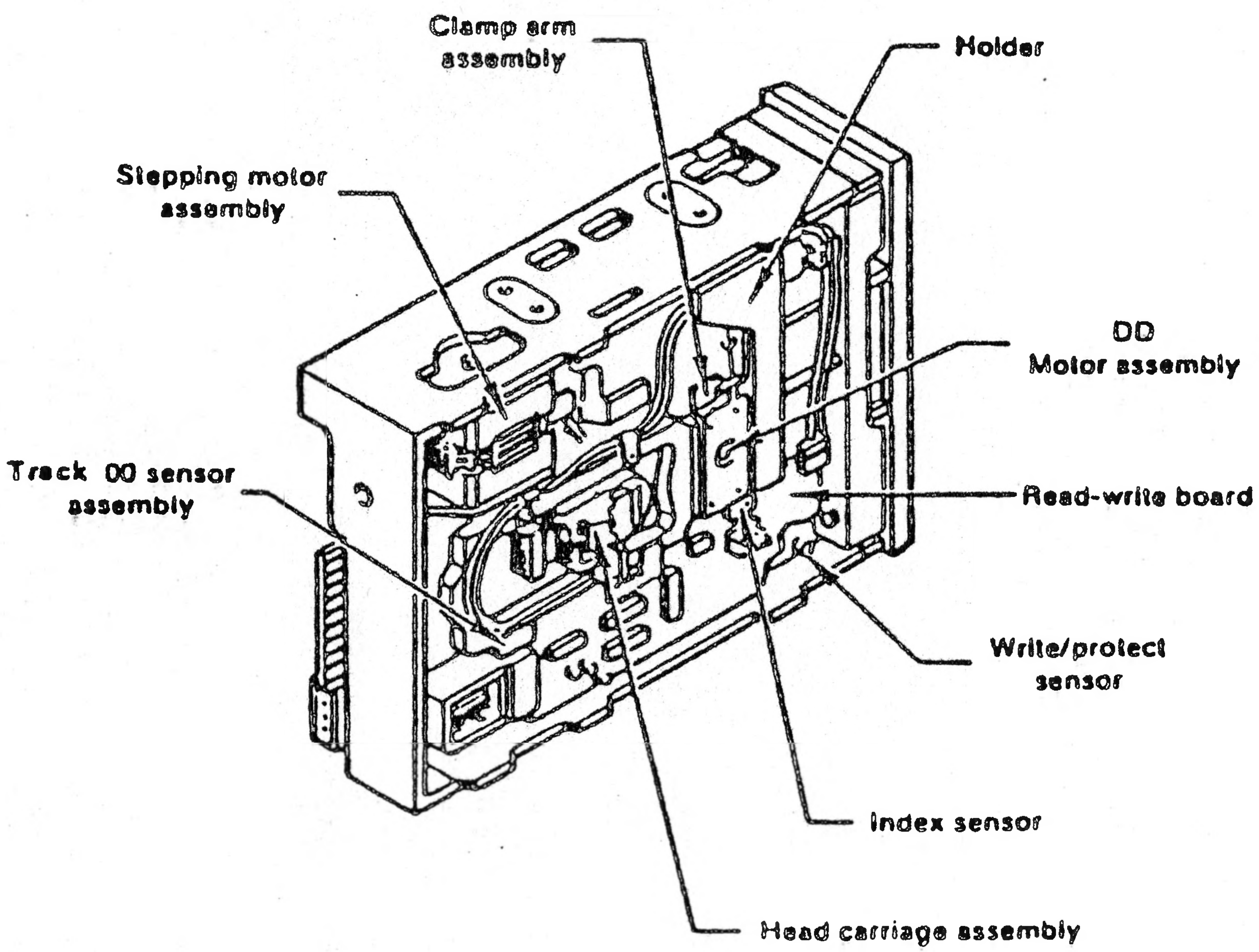
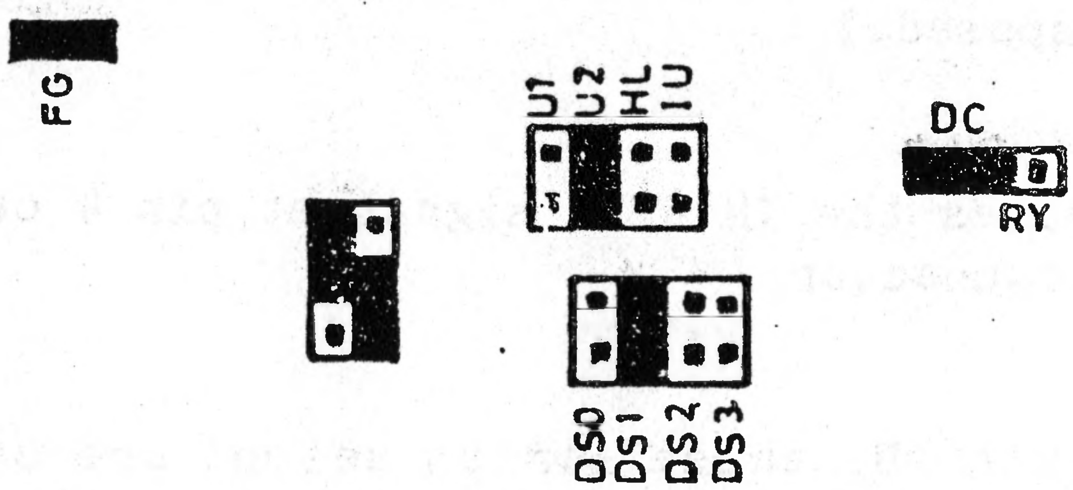


Figure 5.3 Flexible disk drive components

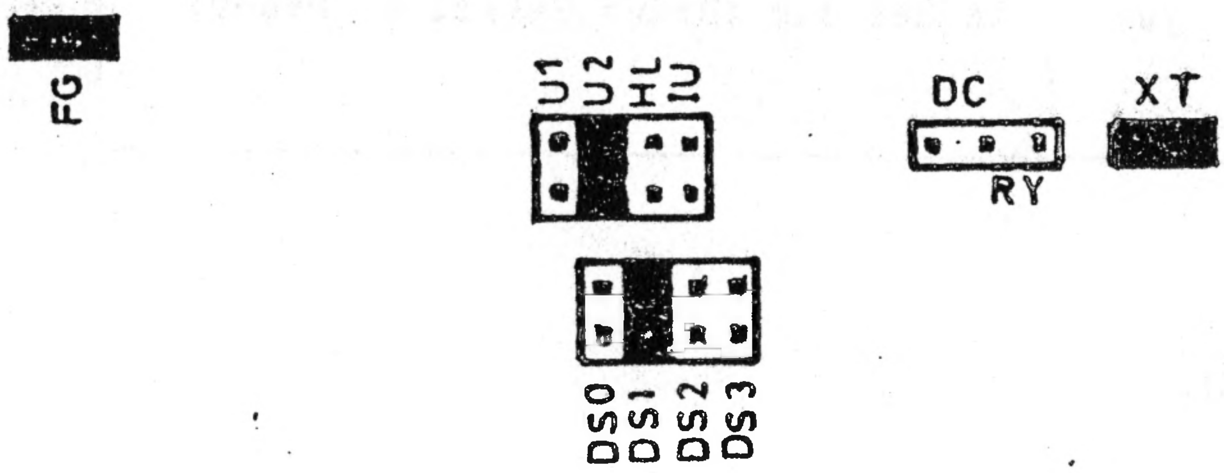
The flexible disk drive is strapped internally. Strap locations are shown in Figure 5.4.



= standard setting for NCR PERSONAL COMPUTER

High capacity drive

Figure 5.4 Flexible disk drive strapping (1 of 2)



= standard setting for NCR PERSONAL COMPUTER

Standard capacity drive

Figure 5.4 Flexible disk drive strapping (2 of 2)

DS1 - DS4
Address selection of the drive. For the NCR PERSONAL COMPUTER DS1 is to be selected, even if the drive being installed is the second in the system. (The

cable band from the first to the second connector has two DS lines transposed.)

IU
When closed, enables the IN USE/ signal at pin 4 of the control/data connector.

U1, U2
In conjunction with IU, these straps select one of five turn-on conditions for the drive indicator LED:

Strap installed			LED turn-on condition(s)
IU	U1	U2	
no	no	no	Drive Select
yes	no	no	Drive Select + In Use
yes	yes	no	In Use
no	yes	yes	Drive Select or Ready
yes	yes	yes	In Use and (Drive Select or Ready)

HL
Not used (open)

FG
Connects frame to 0 V.

LG, HG (high capacity only)
One of these straps must be installed:

Installed	Density Signal "Low" selects
LG	High density
HG	Low density

I, II (high capacity only)
One of these straps must be installed:

Installed	Density uses	Rot. Speed (r.p.m)
I	High	360
	Low	300
II	High	360
	Low	360

RY, DC (high capacity only)
One of these straps must be installed: pin 34 of the control/data connector provides Ready (RY installed) or Disk Change (DC installed) signal.

RY, XT (standard capacity only)
One of these straps must be installed: pin 34 of the control/data connector provides Ready signal (RY installed) or is low state of an open collector (XT installed).

MOTOR TURN-ON

The flexible disk drive motor starts rotating under one or more of the following conditions:

* Assertion of Motor On signal
* Diskette insertion
* Diskette removal (unless write-protected)

Motor rotation stops under one or more of the following conditions:

* Drive lever has been closed, the motor is rotating, and drive status has become Ready

* Approximately 10 seconds after diskette removal

* Diskette was inserted at the index-hole position and the lever has been open for approximately 10 seconds

CONTROL AND DATA SIGNALS

The flexible disk drives use the standard pin assignments as shown in Figure 5.5. Figure 5.6 shows the corresponding edge connector on the flexible disk drive.

The input and output signals to the disk drive are standard, industry-compatible signals. An overview of flexible disk control signals is provided in Figures 5.7 and 5.8. These signals are:

Ready or Disk Change (strap-selected)
Ready or Open (strap-selected)
The Ready signal is active when the following conditions are satisfied:

* there is power at the unit
* the diskette is installed
* Motor On is asserted
* Disk rotation is more than half nominal speed
* two Index pulses have been counted since disk rotation exceeded half nominal speed

Disk Change is active

* at power-on or diskette removal

Ready is inactive when

* a diskette is installed and a Step pulse is received while the Drive Select is active

Signal (active low)	Signal Pin	Signal Direction
Ready/ or Open/ (standard capacity)	34	OUT
Ready/ or Disk Change (high capacity)		
Side One Select/	32	IN
Read Data/	30	OUT
Write Protect/	28	OUT
Track 0/	26	OUT
Write Gate/	24	IN
Write Data/	22	IN
Step/	20	IN
Direction Select/	18	IN
Motor On /	16	IN
Drive Select 2/	14	IN
Drive Select 1/	12	IN
Drive Select 0/	10	IN
Index/	8	OUT
Drive Select 3/	6	IN
In Use/	4	IN

NOTE: All odd numbered pins are signal ground.

Figure 5.5 FDD Pin assignments

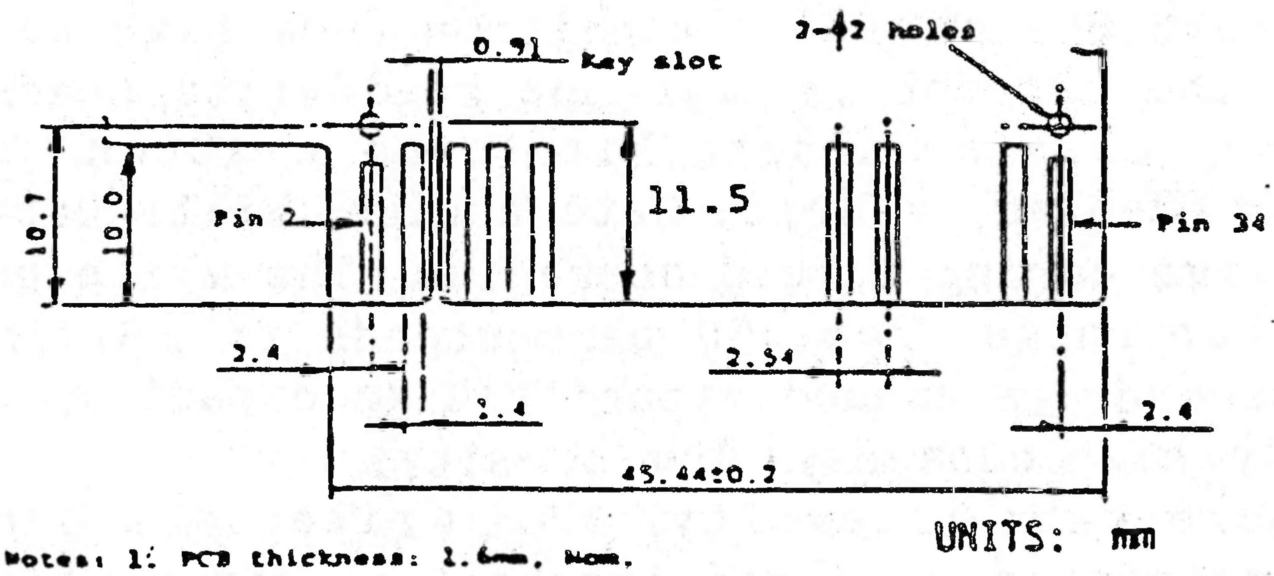


Figure 5.6 FDD Edge Connector.

Side One Select
Active = select side 1, inactive = select side 0.

Read Data
Output signal containing composite clock and data pulses.

Write Protect
Active low output signal to indicate when a write protected disk is installed in the drive. The drive inhibits writing and provides the write protect signal, irrespective of the state of the Write Data and Write Gate signals.

Track 00
Active low output signal to indicate when the read/write heads are positioned at track zero. Track 00 is not active when the read/write heads are not at track zero.

Write Gate
Active low input signal to enable data to be written on the diskette. Write Gate not active enables the stepper logic and read data logic.

Write Data
Input signal to provide the data to be written on the flexible disk. Each transition from high to low causes the current through the read/write heads to reverse, causing a data bit to be written. This line is enabled by Write Gate active. Write Data is not active during a read operation. The write pulse width can range from 150 nanoseconds to 2.5/1.1/2.1 microseconds (standard capacity/high capacity, high density/high capacity, low density).
To ensure data integrity, MFM write data can be pre-compensated on inner tracks (see signal timing Figures, below)

Step
Active low input signal to move the head in the direction specified by Direction Select. Each step pulse is delayed by at least 6ms (standard

capacity) or 3 ms (high capacity) from the preceding step.
Head movement to an adjacent track requires two steps in standard capacity drives.

Direction Select
Input signal to define the direction the heads move when the step line is pulsed. Low causes the head to move toward the center of the disk. High causes the head to move toward the outside of the disk.

Motor On
Active low input signal to turn the motor on. Time has to be allowed by the system before reading or writing to allow the motor to start. The time required is 400 ms (500 ms for high capacity, 360 r.p.m).

Drive Select (0,1,2,3)
Active low input signal to select one of two flexible disk drives (only 0 and 1 are used).

Index
Active low output signal which is at an active level each time the index hole is sensed. This signal is active for one pulse each disk revolution to indicate the beginning of a track. Index is held active when no flexible disk is inserted in the system.(The standard capacity drive also issues this signal when sector holes are detected on hard-sectored diskettes.)

In Use
If the IU strap is installed, this signal is active to indicate that all the daisy-chained flexible disk drives are in use under system control.

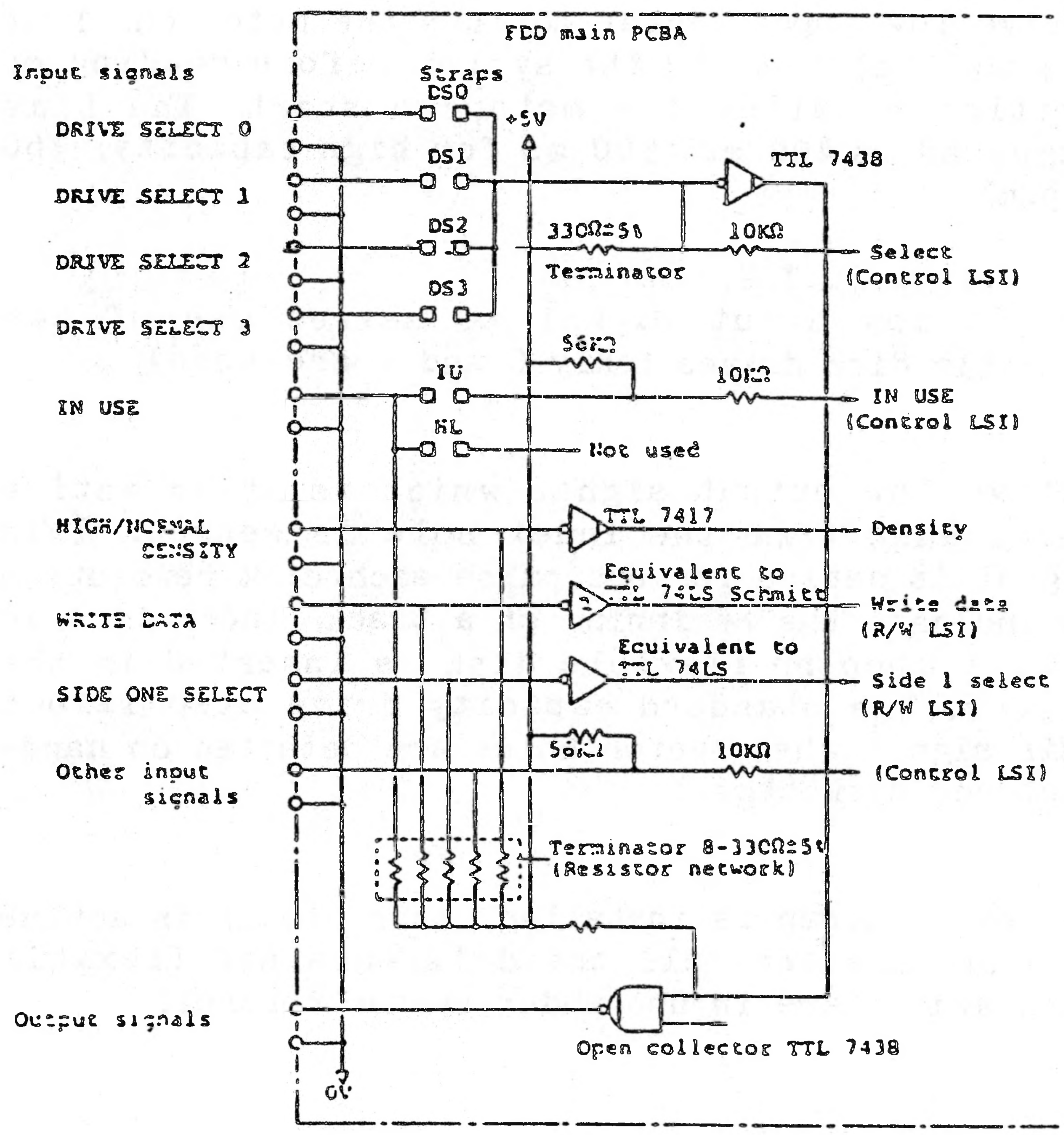


Figure 5.7 Flexible disk drive control (high capacity)

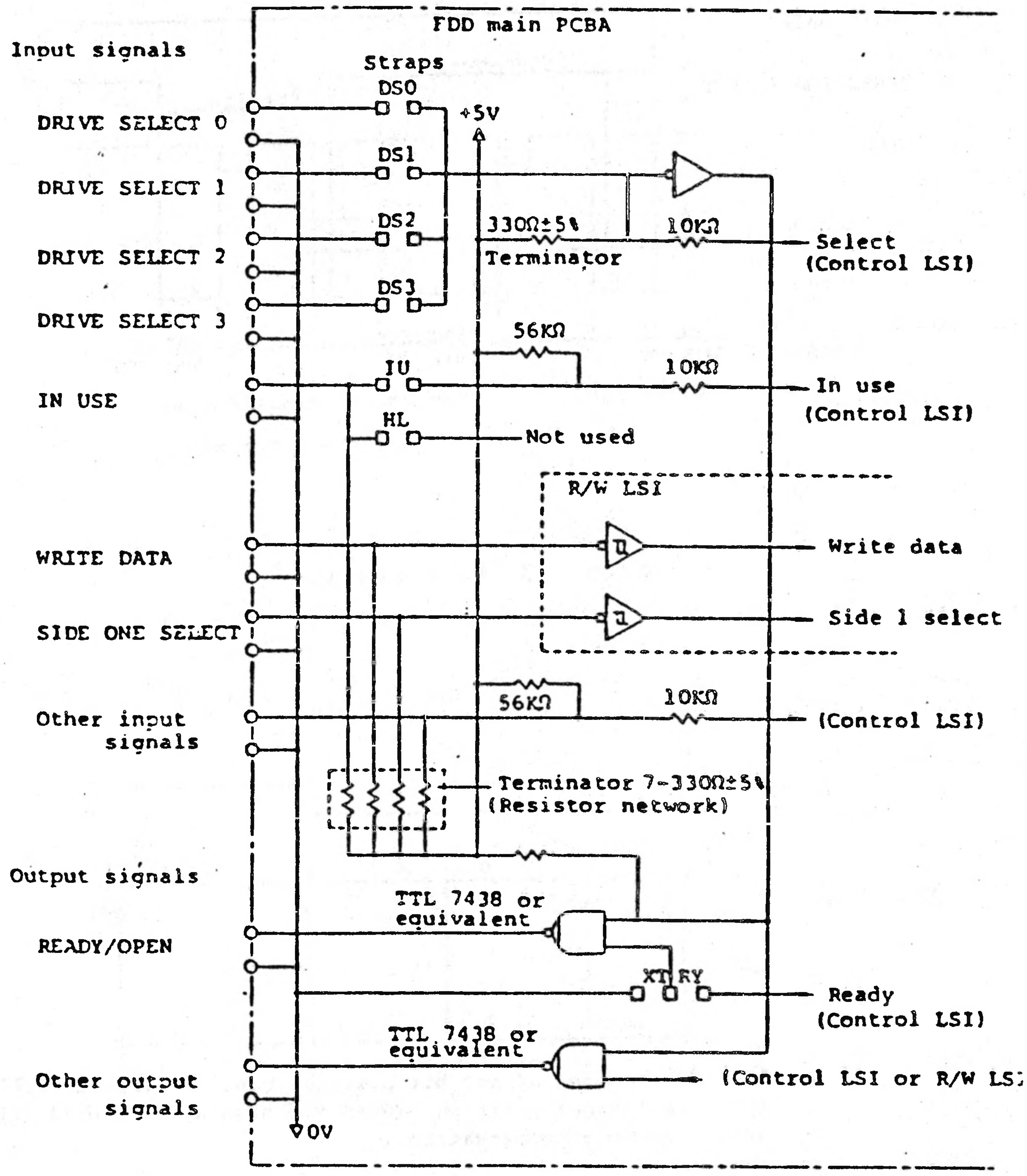


Figure 5.8 Flexible disk drive control (standard capacity)

Figures 5.9 - 5.12 illustrate signal timing.

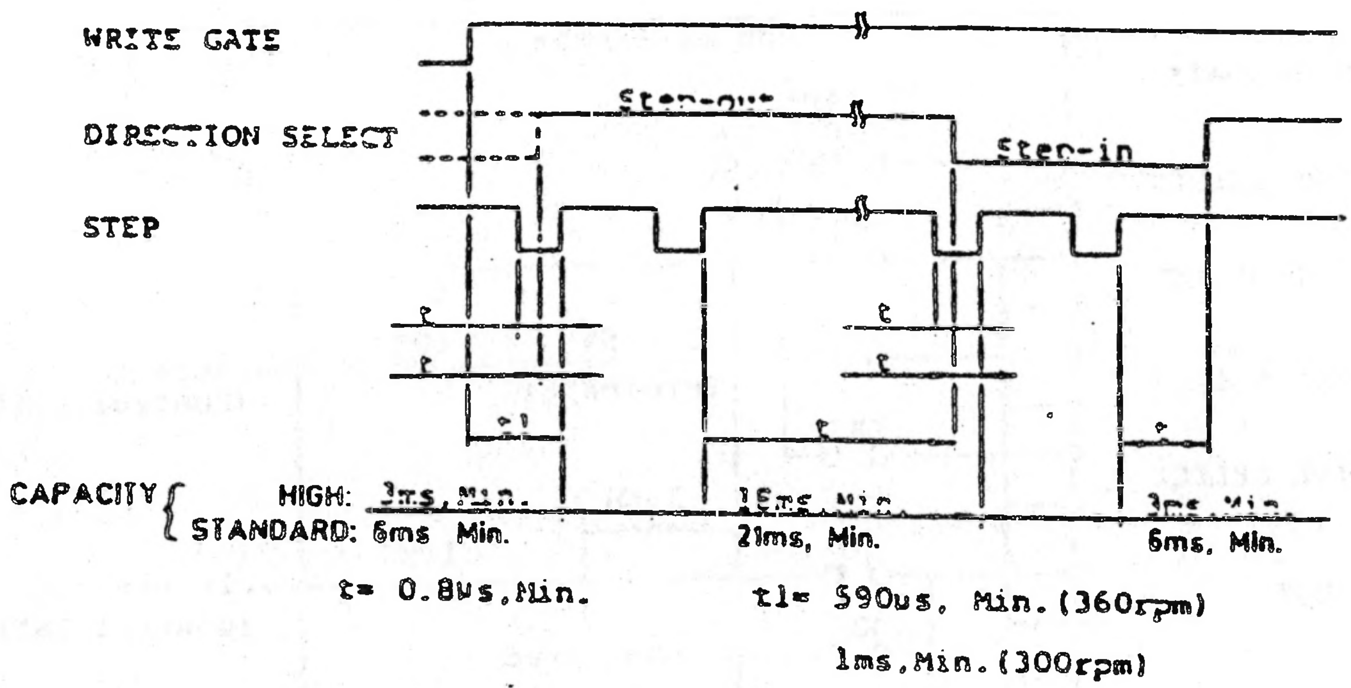
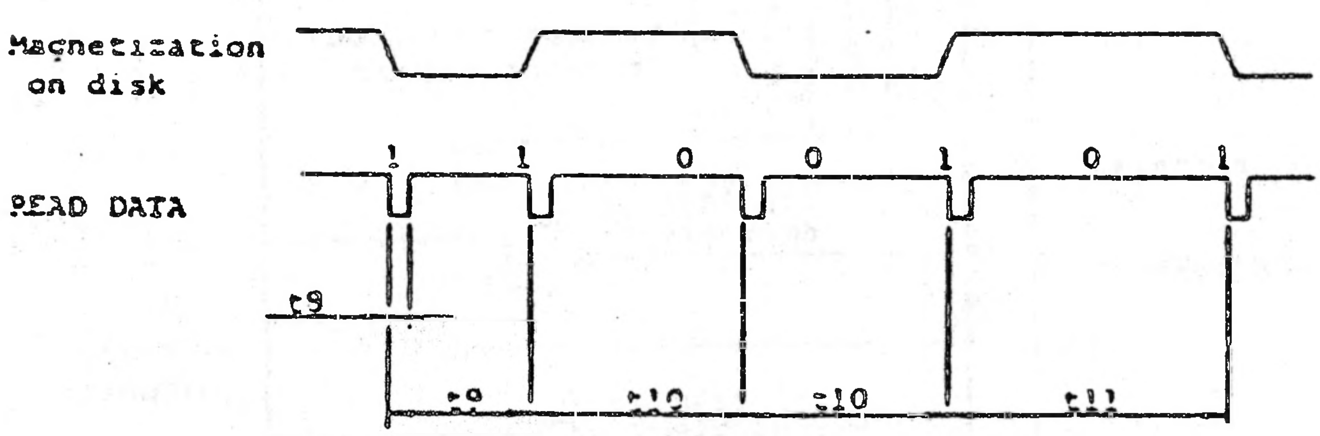


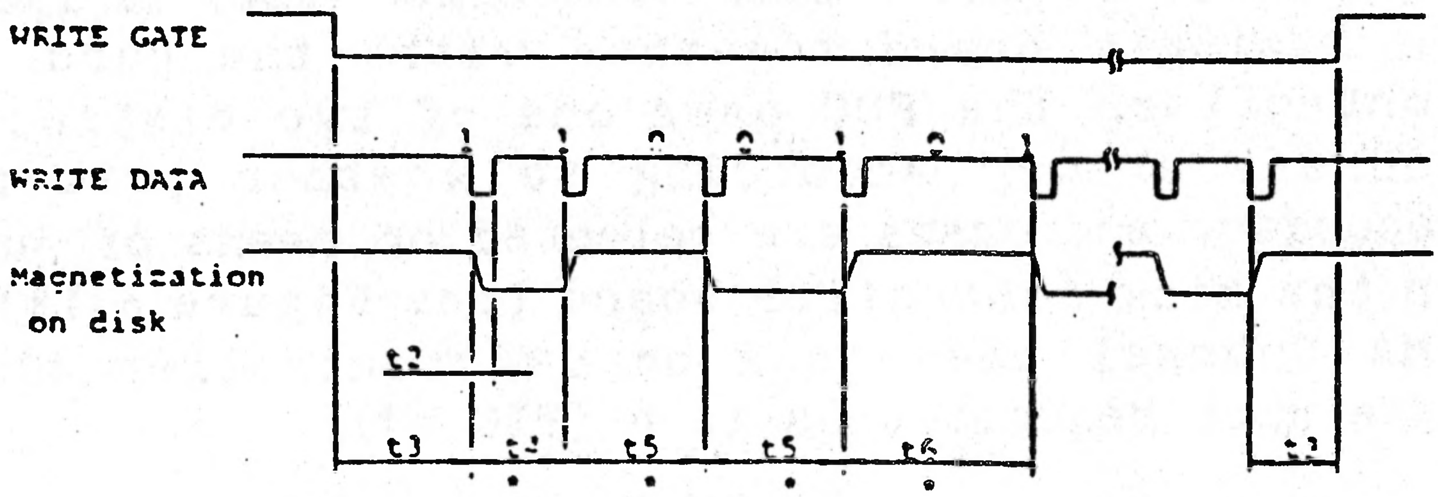
Figure 5.9 Step Timing



Note: The displacement of any bit position does not exceed "t12" from its nominal position. (When PLO separator is used with zero write pre-compensation.)

	Density & Disk speed	t8	t9	t10	t11	t12
HIGH CAPACITY	High, 360rpm	0.5±0.25us	2us,Nom.	3us,Nom.	4us,Nom.	±350ns
	Normal, 360rpm	0.5±0.25us	3.3us,Nom.	5us,Nom.	6.7us,Nom.	±580ns
	Normal, 300rpm	0.5±0.25us	4us,Nom.	6us,Nom.	8us,Nom.	±700ns
	STANDARD CAPACITY	1.0 ± 0.5 us	4 μs, Nom.	6 μs, Nom.	8 μs, Nom.	± 700 ns

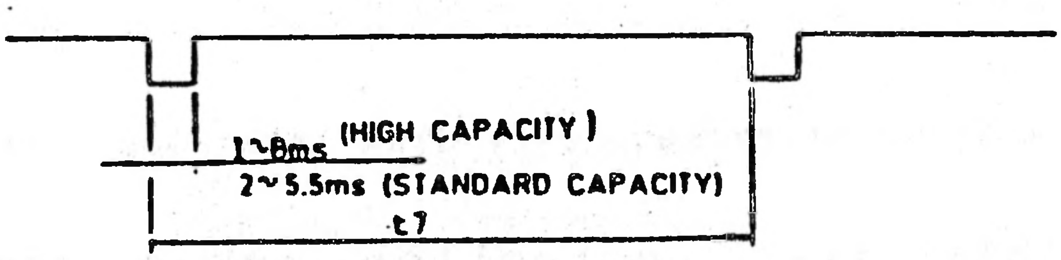
Figure 5.10 Read Data Timing (MFM)



*:±0.5%

Density & Disk Speed	t2	t3	t4	t5	t6
HIGH CAPACITY: High,360rpm	0.15~1.1us	4us,Max.	2us,Nom.	3us,Nom.	4us,Nom
HIGH CAPACITY: Normal,360rpm	0.15~2.1us	6.7us,Max	3.3us,Nom.	5us,Nom.	6.7us,Nom.
HIGH CAPACITY: Normal,300rpm	0.15~2.1us	8us,Max.	4us,Nom.	6us,Nom.	8us,Nom.
STANDARD CAPACITY	0.15 ~ 2.5 us	8 us, Max.	4 us , Nom.	6 us, Nom.	8 us , Nom.

Figure 5.11 Write Data Timing (MFM)



t7= 166.7±2.5ms (360rpm)

200±3ms (300rpm)

(Fig.106) INDEX timing

Figure 5.12 Index Timing

THE FLEXIBLE DISK CONTROLLER

The PD765A Flexible Disk Controller (FDC) is included on a single board together with the hard disk controller. The FDC uses one of two distinct I/O address areas, according to whether primary or secondary addresses are selected by means of jumpers on the disk controller board (see Figure 5.13). The DMA Channel used is 2 on DMA controller #1. The interrupt request used is 6 (PIC #1).

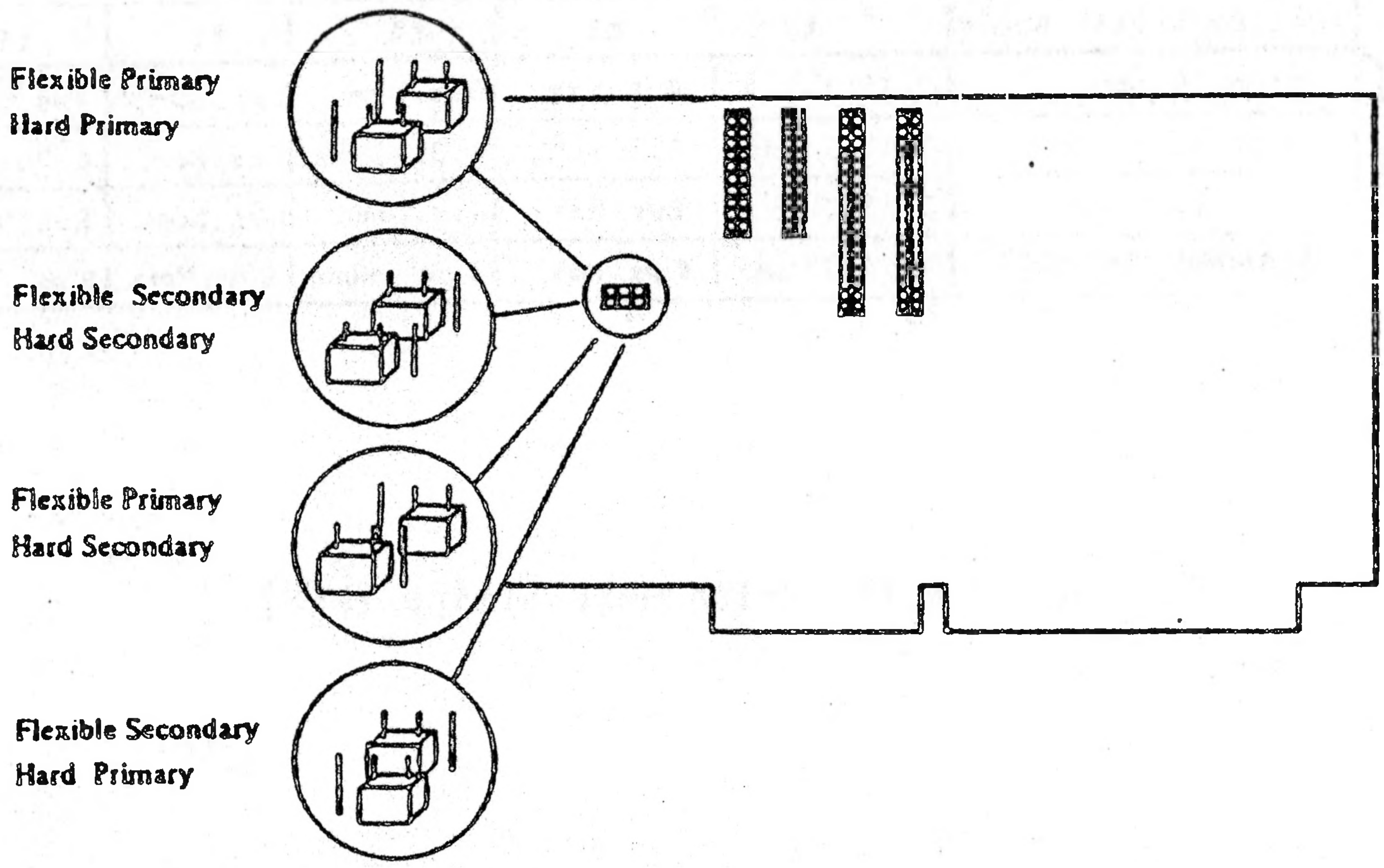


Figure 5.13 Primary/secondary disk interface selection.

The flexible disk controller makes use of the following primary interface ports to the microprocessor (secondary interface is given in parentheses):

OUT 3F2H (372H)	Drive select command output
IN 3F4H (374H)	Read the FDC's Main Status Register
OUT 3F5H (375H)	Output up to nine commands to the command stack

IN	3F5H (375H)	Input one of up to seven results, including up to four 8-bit status registers, from the result stack
OUT	3F7H (377H)	Diskette control register, used to control data transfer speed
IN	3F7H (377H)	A diagnostics register used by both flexible and hard disk drive(s). Bit 7 set denotes a diskette change

The FDC can perform several different operational commands, each initiated by the transfer of a byte of command identification and any parameters belonging to that command via port 3F5H. Each operation in the process of flexible disk control can be regarded as consisting of three phases:

* Command Phase

  During the Command Phase, the FDC receives commands and inherent parameters from the microprocessor.

* Execution Phase

  During this phase, the actual execution of the command takes place.

* Result Phase

  During this phase, useful operational status information can be read by the microprocessor via the Main Status Register and/or the other four status registers. If the operation involved microprocessor reading of flexible disk data, that data is made available.

The Main Status Register

Figure 5.14 indicates the status information which can be read via port 3F4H (374H).

Bits 6 (DIO) and 7 (RQM) of the Main Status Register are of particular importance for the transfer of information between FDC and microprocessor. Before writing a byte to the FDC, these bits must be 0 and 1, respectively. Reading a byte from the FDC requires both these bits to be 1.

The FDC in your NCR PERSONAL COMPUTER operates in DMA mode, with the result that interrupt detection before reading individual bytes is not required. In this mode, the FDC communicates with the DMA controller by means of an exchange of DRQ and DACK/ signals.

The significance of the FDC Main Status Register when identifying the three operational phases is as follows:

Command Phase.

Commands/data for operation are received from the microprocessor. During this phase, DIO and RQM must be 0 and 1, respectively.

Execution Phase

Performance of the requested operation. At the beginning of this phase, DIO and RQM go to 1 and zero, respectively.

Result Phase

Information available to the microprocessor, denoted by bits 6 and 7 of the Main Status Register being set.

Bit	Name	Symbol	Description
D0	FDD 0 Busy	D0B	FDD 0 is in the Seek mode
D1	FDD 1 Busy	D1B	FDD 1 is in the Seek mode
D2	FDD 2 Busy	D2B	FDD 2 ... not used
D3	FDD 3 Busy	D3B	FDD 3 ... not used
D4	FDC Busy	CB	A read or write command is in process
D5	Non-DMA mode	NDM	The FDC is in non-DMA mode. This bit is set only during execution phase in non-DMA mode Transition to zero indicates execution phase has ended
D6	Data Input /Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO is set, then transfer is from Data Register to the Processor. If DIO is zero, then transfer is from Processor to Data Register
D7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM can be used to perform handshaking functions of "ready" and "direction" to the processor

Figure 5.14 FDC Main Status Register

The Drive Select Register

The Drive Select Register is a write only register (Port 3F2H/372H) used to:

* Select disk drive units
* Control the motors of these units
* Enable controller interrupts and DMA requests

Figure 5.15 explains the significance of the individial bits of this register.

Bit	Significance
0	Bit zero selects drive 0, bit set selects drive 1
1	Not used
2	Bit set enables FDC (reset)
3	Bit set enables DMA request and FDC interrupts to be to I/O interface. Bit zero disables I/O interface drivers.
4	Turns motor of drive 0 on (bit set) or off (bit zero)
5	1
6	Not used
7	Not used

Figure 5.15 Drive select register

Diskette Control Register

This register is written to the controller in order to set data transfer speed. When this register has been written, the FDC should be reset (Drive Select Register bit 2).

Bit	Significance
0	} binary value specifying data transfer speed (KB/s):
1	} 00 = 500, 01 = 300, 10 = 250, 11 = 125 (FM)
2-7	Not used

Figure 5.16 Diskette control register

FDC Commands and their Parameters

Figure 5.17 presents a summary of commands and parameters transmitted via port 3F5H/375H. A command phase consists of up to 9 bytes. The tables comprising Figure 5.18 explain the abbreviations used in Figure 5.17.

A system interrupt (type 6) denotes that an execution phase is completed or prematurely terminated. Status information and/or data is then available for input at port 3F5H/375H. The sigificance of this result phase (consisting of up to 7 bytes) is also set out in Figure 5.17. The significance of the status information which can be read during the result phase is set out in detail in Figure 5.24. (This status information is not to be confused with the Main Status which can be read at any time via port 3F4H/37H.)

It is important that commands and their data are input in the correct order, and that return information is read completely, even if elements of this information are not required.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		READ DATA								
	W	MT	MFM	SK	0	0	1	1	0	Command Codes
C	W	0	0	0	0	0	HDS	DS1	DS0	
o	W	C								Sector ID info.
m	W	H								prior to Com-
m	W	R								mand execution
a	W	N								
n	W	EOT								
d	W	GPL								
	W	DTL								
E										Data transfer
x										between the FDD
e										and main system
	R	ST0								Status info
R	R	ST1								after Command
e	R	ST2								execution
s	R	C								
u	R	H								Sector ID info.
l	R	R								after Command
t	R	N								execution

Figure 5.17 FDC Command Summary (1 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		DATA BUS								
		READ DELETED DATA								
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID info. prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Exe										Data transfer between the FDD and main system
Result	R	ST0								Status info after Command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID info. after Command execution
	R	H								
	R	R								
	R	N								

Figure 5.17 FDC Command Summary (2 of 10)

WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID info. prior to Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Exe										Data transfer between the FDD and main system
Result	R				ST0					Status info after Command execution
	R				ST1					
	R				ST2					
	R				C					Sector ID info. after Command execution
	R				H					
	R				R					
	R				N					

Figure 5.17 FDC Command Summary (3 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					WRITE DELETED DATA					
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID info. prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Exe										Data transfer between the FDD and main system
Result	R					ST0				Status info after Command execution
	R					ST1				
	R					ST2				
	R					C				
	R					H				Sector ID info. after Command execution
	R					R				
	R					N				

Figure 5.17 FDC Command Summary (4 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
						READ A TRACK				
Command	W	MT	MFM	SK	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID info. prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Exe										Data transfer between the FDD and main system. FDC reads all of cylinder's contents from index hole to EOT
Result	R	ST0								Status info after Command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID info. after Command execution
	R	H								
	R	R								
	R	N								

Figure 5.17 FDC Command Summary (5 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		READ ID								
C	W	MT	MFM	0	0	1	0	1	0	Command Codes
m	W	0	0	0	0	0	HDS	DS1	DS0	
d										The first cor-
										rect ID info on
E										the Cylinder is
x										stored in Data
e										Register
	R	ST0								Status info
R	R	ST1								after Command
e	R	ST2								execution
s	R	C								
u	R	H								Sector ID info.
l	R	R								during Execution
t	R	N								Phase

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		FORMAT A TRACK								
	W	MT	MFM	0	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
C	W	N								Bytes/Sector
m	W	SC								Sectors/Cylinder
d	W	GPL								Gap 3
	W	D								Filler Byte
E										FDC formats an
x										entire cylinder
	R	ST0								Status info
R	R	ST1								after Command
e	R	ST2								execution
s	R	C								
u	R	H								In this case
l	R	R								the ID info has
t	R	N								no meaning

Figure 5.17 FDC Command Summary (6 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID info.
	W	H								prior to Com-
	W	R								mand execution
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Exe										Data compared between the FDD and main system
Result	R	ST0								Status info
	R	ST1								after Command
	R	ST2								execution
	R	C								
	R	H								Sector ID info.
	R	R								after Command
	R	N								execution

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
SEEK										
Cmd	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Exe										Head positioned over proper Cylinder on Diskette

Figure 5.17 FDC Command Summary (7 of 10)

<table>
<tr><th rowspan="2">PHASE</th><th rowspan="2">R/W</th><th colspan="8">DATA BUS</th><th rowspan="2">REMARKS</th></tr>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><th colspan="11">SCAN LOW OR EQUAL</th></tr>
<tr><td></td><td>W</td><td>MT</td><td>MFM</td><td>SK</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Command Codes</td></tr>
<tr><td>C</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>HDS</td><td>DS1</td><td>DS0</td><td></td></tr>
<tr><td>o</td><td>W</td><td colspan="8">C</td><td>Sector ID info.</td></tr>
<tr><td>m</td><td>W</td><td colspan="8">H</td><td>prior to Com-</td></tr>
<tr><td>m</td><td>W</td><td colspan="8">R</td><td>mand execution</td></tr>
<tr><td>a</td><td>W</td><td colspan="8">N</td><td></td></tr>
<tr><td>n</td><td>W</td><td colspan="8">EOT</td><td></td></tr>
<tr><td>d</td><td>W</td><td colspan="8">GPL</td><td></td></tr>
<tr><td></td><td>W</td><td colspan="8">STP</td><td></td></tr>
<tr><td>E</td><td></td><td colspan="8"></td><td>Data compared</td></tr>
<tr><td>x</td><td></td><td colspan="8"></td><td>between the FDD</td></tr>
<tr><td>e</td><td></td><td colspan="8"></td><td>and main system</td></tr>
<tr><td></td><td>R</td><td colspan="8">ST0</td><td>Status info</td></tr>
<tr><td>R</td><td>R</td><td colspan="8">ST1</td><td>after Command</td></tr>
<tr><td>e</td><td>R</td><td colspan="8">ST2</td><td>execution</td></tr>
<tr><td>s</td><td>R</td><td colspan="8">C</td><td></td></tr>
<tr><td>u</td><td>R</td><td colspan="8">H</td><td>Sector ID info.</td></tr>
<tr><td>l</td><td>R</td><td colspan="8">R</td><td>after Command</td></tr>
<tr><td>t</td><td>R</td><td colspan="8">N</td><td>execution</td></tr>
</table>

Figure 5.17 FDC Command Summary (8 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		SCAN HIGH OR EQUAL								
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID info. prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Exe										Data compared between the FDD and main system
Result	R	ST0								Status info after Command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID info. after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		RECALIBRATE								
C	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
E										Head retracted to Track 0

Figure 5.17 FDC Command Summary (9 of 10)

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
SENSE INTERRUPT STATUS										
C	W	0	0	0	0	1	0	0	0	Command Codes
Res	R	STO								Status info. at the the end of each seek operation about FDC
	R	PCN								

SPECIFY TIME										
Com	W	0	0	0	0	0	0	1	1	Command Codes
	W	— SRT —>				<— HUT —				
	W	— HLT ——>							ND	

SENSE DRIVE STATUS										
C	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
R	R	ST3								Status info about FDD

INVALID										
C	W	Invalid Codes								Invalid Command Codes [NoOp-FDC goes into Stand-by Status]
R	R	STO								STO = 80

Figure 5.17 FDC Command Summary. [10 of 10]

SYMBOL	NAME	DESCRIPTION
A0	Address Line 0	A0 controls selection of Main Status Register (A0 = 0) or Data Register (A0 = 1)
C	Cylinder No.	C stands for the current selected Cylinder number
D	Data	D stands for the data pattern for writing to a Sector
D7-D0	Data Bus	8-bit Data Bus where D7 is the most significant bit, and D0 is the least significant bit
DS0, DS1	Drive Select	DS stands for a selected drive number 0 or 1
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out of, or write into the Sector. Otherwise, DTL should be 0FFH
EOT	End of Track	EOT stands for the final Sector number of a Cylinder
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync Field)
H	Head Address	H stands for head number 0 or 1, as specified in ID field
HDS	Head Select	HDS stands for a selected head number 0 or 1 (H = HDS in all command words)

Figure 5.18 Abbreviations used in FDC Command Summary (1 of 3)

SYMBOL	NAME	DESCRIPTION
HLT	Head Load Time	HLT stands for the head load time in the FDD (High Capacity: 2 to 256 ms in 2 ms increments. Standard Capacity: 4 to 512 ms in 4 ms increments)
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (High Capacity: 0 to 240 ms in 16 ms. Standard Capacity: 0 to 480 ms in 32 ms increments
MFM	FM or MFM Mode	0 = select FM mode, 1 = select MFM mode
MT	Multi-Track	If MT is set, a multi-track read or write operation is performed (both tracks of cyl.)
N	Number	N stands for the number of data bytes written in a Sector
NCN	New Cylinder Number	NCN stands for new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head
ND	Non-DMA Mode	ND = operation in non-DMA mode
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Head position at present time
R	Record	R stands for the Sector number which will be read or written

Figure 5.18 Abbreviations used in FDC Command Summary (2 of 3)

SYMBOL	NAME	DESCRIPTION
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal
SC	Sector	SC indicates the number of Sectors per Cylinder
SK	Skip	SK stands for Skip Deleted Data Address Mark
SRT	Step Rate Time	SRT = 2's complement of Step Rate incremental units. One unit is 1 ms (High capacity) or 2 ms (Standard Capacity)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-3 stands for one of four registers storing the status information after a command has been executed. This info is available during the result phase after command execution. These registers are not to be confused with the main status register (selected by A0 = 0). ST0-3 may be read only after a command has been executed. They contain information relevant to that particular command.
STP	Scan Test	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2 , then alternate sectors are read and compared

Figure 5.18 Abbreviations used in FDC Command Summary (3 of 3)

Notes concerning individual FDC commands (the status registers referred to here are described in the subsequent section):

READ DATA
After head location and settling time, the requested sector is located by means of the ID marks and ID fields on the located track. The FDC then outputs the data from the flexible disk data field one byte at a time. This operation is a multi-sector read, that is, sectors are output by the FDC until the DMA issues a TC (terminal count signal). If there are sectors remaining on the track, these are read, but only a Cyclic Reduncancy Check is performed; they are not output to the data bus. Figure 5.19 states factors affecting transfer capacity of a single read command.

MT	MFM	Byte/ Sector N	Max.Transfer Capacity [Bytes/Sector] [Number of Sectors]	Final Sector Read from Diskette
0	0	00	[128][26] = 3,328	26 at Side 0
0	1	01	[256][26] = 6,656	or 26 at Side 1
1	0	00	[128][52] = 6,656	26 at Side 1
1	1	01	[256][52] = 13,312	26 at Side 1
0	0	01	[256][15] = 3,840	15 at Side 0
0	1	02	[512][15] = 7,680	or 15 at Side 1
1	0	01	[256][30] = 7,680	15 at Side 1
1	1	02	[512][30] = 15,360	15 at Side 1
0	0	02	[512] [8] = 4,096	8 at Side 0
0	1	03	[1024] [8] = 8,192	or 8 at Side 1
1	0	02	[512][16] = 8,192	8 at Side 1
1	1	03	[1024][16] = 16,384	8 at Side 1

Figure 5.19 Transfer Capacity

If the MT bit is set, data is read from both sides of the diskette (that is, the entire cylinder), starting with side 0, sector 1, and finishing with the last sector on side 1.
If N is 0, the data length of each sector is defined by DTL. If there are more bytes actually in the sector, the excess bytes are subjected to CRC but do not appear on the data bus.
After accessing the sector(s), there is normally a head unload interval. However, this interval does not apply if the FDC has already detected a subsequent command entailing an access operation. This can save time when accessing large amounts of data.
Note that if you are transferring data from FDC to the microprocessor, the FDC requires microprocessor attention every 27 (FM mode) or 13 (MFM mode) microseconds. Failing this, OR in Status Register 1 (see below) is set.

Possible error conditions:
Failure to find the specified sector sets the ND flag in Status Register 1. In Status Register 0, bit 6 is set and bit 7 is zero, and the command is terminated.
CRC failure sets the DE flag in Status Register 1, and terminates the command. In addition, bit 6 in Status Register 0 is set, bit 7 is zero. If the CRC failure lies in the Data rather than the ID field, the DD flag in Status Register 2 is also set.
External termination (TC signal) influences the C, H, R, and N information. This information further depends on the MT and EOT values given in the command (see Figure 5.20), and can be read in the Result Phase.

READ ONE TRACK

All Data Fields on a track are read, even if CRC failure is encountered. In this case, the NDR flag in Status Register 1 is set. Failure to find an ID Address Mark sets the MA flag in Status Rgister 1 and terminates the command.

MT	EOT	Final Sector Transferred to Processor	ID Info at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0				
	0F	Sector 1 to 14 at Side 0	NC	NC	R+1	NC
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0				
	0F	Sector 15 at Side 0	C+1	NC	R=01	NC
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1				
	0F	Sector 1 to 14 at Side 1	NC	NC	R+1	NC
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1				
	0F	Sector 15 at Side 1	C+1	NC	R=01	NC
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0				
	0F	Sector 1 to 14 at Side 0	NC	NC	R+1	NC
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0				
	0F	Sector 15 at Side 0	NC	LSB	R=01	NC
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1				
	0F	Sector 1 to 14 at Side 1	NC	NC	R+1	NC
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1				
	0F	Sector 15 at Side 1	C+1	LSB	R=01	NC
	08	Sector 8 at Side 1				

Notes: 1. NC (No Change): Same value as at beginning of command execution.

2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Figure 5.20 Status at External Termination

READ DELETED DATA

As READ DATA, exept that upon encountering a Deleted Data Address Mark at the beginning of a Data field, and assuming that SK was zero when the command was issued, the data in the sector is transmitted, the CM flag in Status Register 2 is set, and the command is terminated.

WRITE DATA

When the sector R has been found, the FDC accepts data from the data bus for that sector. Upon occurrence of a TC (Terminal Count) signal, the remainder of the data field currently being written is filled with zeros. CRC failure in an ID field sets the DE flag in Status Register 1 and terminates the command. Other details as in READ DATA.

WRITE DELETED DATA

As WRITE DATA, except that a Deleted Data Address Mark is written at the beginning of the Data field.

READ ID

This command returns the current head position by means of the first ID field the FDC can read. Failure to find an ID Address Mark sets the MA flag in Status Register 1. If there is no data, ND is set in the same register.

FORMAT ONE TRACK

The format is determined by the values specified for N, SC, GPL, and D in the command. The sector is located by means of the C, H, R, and N values. The R value is incremented automatically, until index hole detection indicates the end of the track.
If an error situation arises, the EC flag in Status Register 0 is set, and the command is terminated. The N, SC and GPL values for MFM recording are shown in Figure 5.21.

Sector Size	N	SC	GPL 1	GPL 2
256	01	12	0A	0C
256	01	10	20	32
512	02	08	2A	50
1024	03	04	80	F0
2048	04	02	C8	FF
4096	05	01	C8	FF

Figure 5.21 Sector Size Variables

GPL 1 values given avoid splicing between data field and ID field of contiguous sections. GPL 2 figures are for formatting purposes.

SCAN ONE TRACK

Data read by the FDC from disk is compared byte by byte with data on the data bus (supplied by DMA controller or microprocessor). The comparative condition can be =, <=, or >=, using one's complement arithmetic. The operation is carried out for the specified track, with automatic incrementing of R until the condition is fulfilled, end of track is reached, or a TC signal occurs.
If the scan condition is fulfilled, the SH bit in Status Register 2 is set; SN set Status Register 2 indicates non-fulfilment. Figure 5.22 shows the possible conditions of comparison and the status of SH and SN (FDD = data read from disk, Bus = data read from data bus).

If a Deleted Data Address Mark is encountered and SK was issued in the scan command as a zero bit, this is regarded as the last sector and CM in Status Register 2 is set. If SK was issued set, CM is likewise set to indicate that the deletion mark was detected, but the scan process skips that sector and continues to scan the remainder of the track.

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	D FDD= D Bus
	1	0	D FDD<>D Bus
	0	1	D FDD= D Bus
Scan Low or Equal	0	0	D FDD< D Bus
	1	0	D FDD> D Bus
	0	1	D FDD= D Bus
Scan High or Equal	0	0	D FDD> D Bus
	1	0	D FDD< D Bus

Figure 5.22 Scan Status Codes

SEEK

The present cylinder number (PCN) is compared with the new cylinder number to be located (NCN). If PCN < NCN, the Direction line to the flexible disk drive is set high; if PCN > NCN, this line is low. When the cylinder has been located, SE in Status Register 0 is set and the command terminated.
If the disk drive is not ready, the NR flag in Status Register 0 is set and the command terminated. This command does not include a result phase. However, the termination of the command is effected by means of the Sense Interrupt Status command.

NOTE: FDC read and write commands affect the track/cylinder at which the head is currently positioned. To locate the track/cylinder itself, an explicit SEEK command must be issued.

RECALIBRATE

With the Direction line high, the read/write head retracts 77 step pulses or to track 0, whichever occurs first. The SE flag in Status Register 0 is set high. If the Track 0 signal is still low, the EC flag in Status Register 0 is also set high. This command does not include a result phase. However, the termination of the command is effected by means of the Sense Interrupt Status command.

SENSE INTERRUPT STATUS

An interrupt signal occurs upon entering the result phase of one of the above commands (or upon termination of SEEK or RECALIBRATE), or the Ready line changes state, or during execution in non-DMA mode. Figure 5.23 shows the significance of the three interrupt status bits affected in Status Regiser 0. It is important to check this interrupt status before attempting to read the information resulting from an FDC command.

Seek End	Interrupt Code		Cause
Bit 5	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Figure 5.23 Sense Interrupt Status

SPECIFY TIME

Sets Head Load Time (HLT), Head Unload Time (HUT), and Step Rate Time (SRT). In addition, non-DMA mode is determined by bit ND being zero.

SENSE DRIVE STATUS

Returns information in Status Register 3.
If the FDC does not recognize a valid a command, no interrupt is generated, but DIO and RQM in the Main Status Register are set (as during a normal result phase). Status Register 0, containing 80H, must be read before a command can be issued to the FDC.

FDC Status

The Main Status Register is accessed via port 3F4H/374H. In addition, there are four status registers which can be read via port 3F5H/375H. Remember, it is imperative that all status registers affected by a particular command (see Figure 5.17) are actually read during the result phase in the specified order, even if the information they yield is not required.

Figure 5.24 summarizes the four Status Registers.

Bit No.	Bit Name	Bit Symbol	Description
			Status Register 0
D7	Interrupt Code	IC	D7 = 0 and D6 = 0. Normal Termination of Command, (NT). Command was properly executed
D6			D7 = 0 and D6 = 1. Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed
			D7 = 1 and D6 = 0. Invalid Command issue, (IC). Command issued was never started
			D7 = 1 and D6 = 1. Abnormal Termination because during Command execution the Ready Signal from FDD changed state
D5	Seek End	SE	When the FDC completes the Seek Command, this flag is set to 1 (high)
D4	Equipment Check	EC	If a fault Signal is received from the FDD, or the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set

Figure 5.24 Status Registers (1 of 6)

Bit No.	Bit Name	Bit Symbol	Description
			Status Register 0
D3	Not Ready	NR	When the FDD is in Not-Ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to Side 1 of a single sided drive, then this flag is set
D2	Head Address	HD	This flag is used to indicate the state of the head at interrupt
D1	Unit Select 1	US1	These flags are used to indicate a Drive Unit number at interrupt
D0	Unit Select 0	US0	

Figure 5.24 Status Register (2 of 6)

Bit No.	Bit Name	Bit Symbol	Description
			Status Register 1
D7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set
D6			Not used. This bit is always 0
D5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set
D4	Over Run	OR	If the FDC is not serviced by the main system during data transfers, within a certain time interval, this flag is set
D3			Not used. This bit is always 0 (low)
D2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or Scan Command this flag is set if the FDC cannot find the Sector specified in the ID Register
			This flag is set when FDC cannot read the ID field without error when executing READ ID command
			Flag is set if starting sector is not found during execution of READ A Cylinder command

Figure 5.24 Status Registers (3 of 6)

Bit No.	Bit Name	Bit Symbol	Description
Status Register 1			
D1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT a Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set
D0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also, at the same time the MD (Missing Address Mark in Data Field) of Status Register 2 is set

Figure 5.24 Status Registers (4 of 6)

Bit No.	Bit Name	Bit Symbol	Description
	Status Register 2		
D7			Bit not used, is always 0 (low)
D6	Control Mark	CM	Flag is set when FDC encounters a sector containing a Deleted Data Address Mark when executing READ DATA or SCAN Command
D5	Data Error in Data Field	DD	Flag is set when FDC detects a CRC error in the data field
D4	Wrong Cylinder	WC	This bit is related to ND bit; flag is set when contents of C differs from that of ID reg.
D3	Scan Equal Hit	SH	Flag is set when condition "equal" is satisfied upon Scan
D2	Scan Not Satisfied	SN	Flag is set when FDC cannot find a sector during Scan meeting the condition
D1	Bad Cylinder	BC	This bit is related to ND bit; flag is set when contents of C is 0FFH and differs from the contents stored in ID register
D0	Missing Address Mark in Data Field	MD	Flag is set when during Read the FDC cannot find a Data Address Mark or a Deleted Data Address Mark

Figure 5.24 Status Registers (5 of 6)

Bit No.	Bit Name	Bit Symbol	Description
Status Register 3			
D7	Fault	FT	Bit indicates status of Fault signal from the FDD
D6	Write Protected	WP	Bit indicates status of Write Protected signal from the FDD
D5	Ready	RDY	Bit indicates status of Ready signal from the FDD
D4	Track 0	T0	Bit indicates status of Track-0 signal from the FDD
D3	Two Side	TS	Bit indicates status of Two-Side signal from the FDD
D2	Head	HD	Bit indicates status of Side Select signal to the FDD
D1	Unit Select 1	US1	Bit indicates status of Unit Select 1 signal to the FDD
D0	Unit Select 1	US0	Bit indicates status of Unit Select 0 signal to the FDD

Figure 5.24 Status Registers (6 of 6)

MINIMUM FORMAT REQUIREMENTS

Figure 5.25 illustrates index requirements and tolerances for flexible disk formatting.

Post-Index
Before initial recording of data upon a selected track, a gap is required to allow for drive-to-drive adjustment tolerances. This is the gap (Gap 1) from

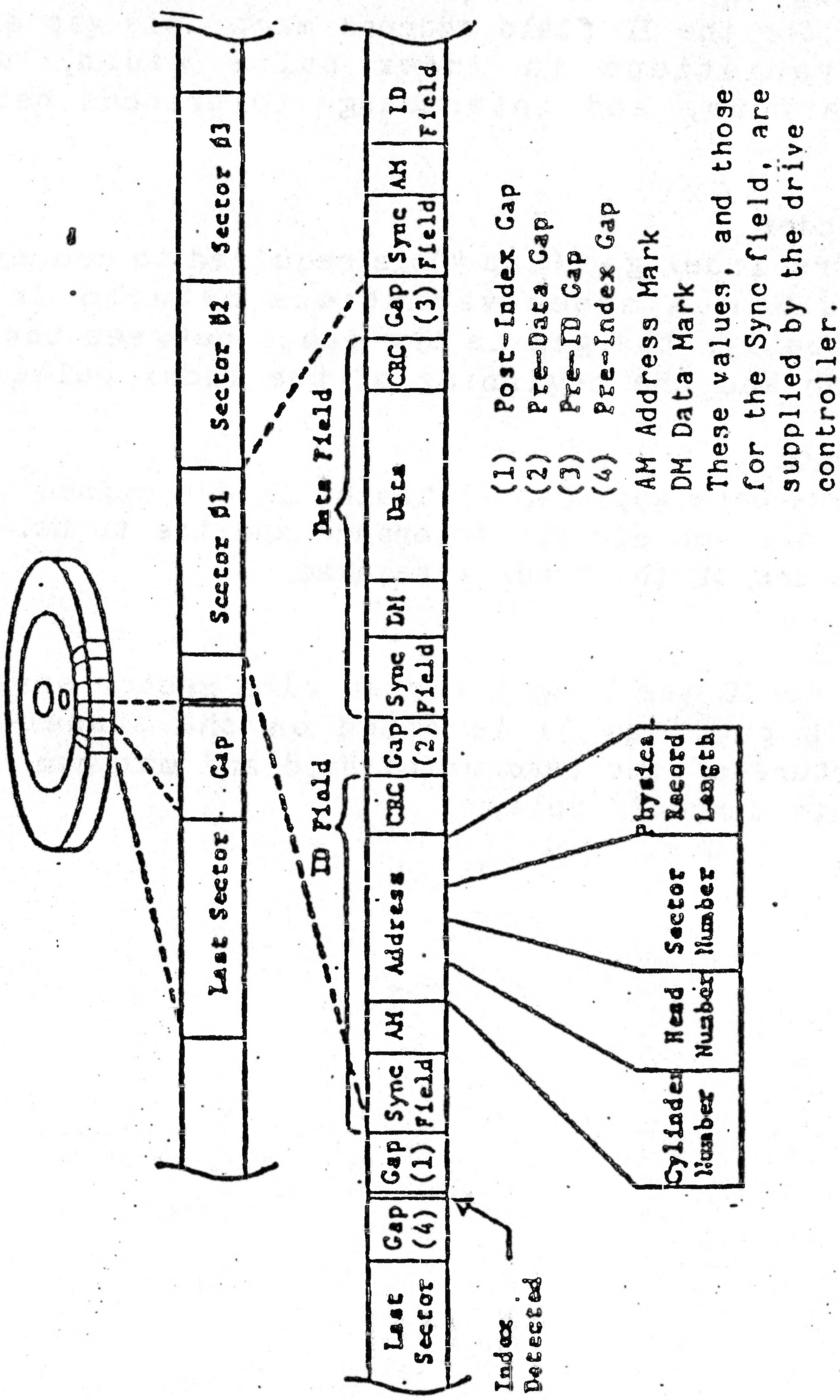


Figure 5.25 Flexible disk format

the edge of the index pulse to the beginning Sync Field for the ID field address mark. This gap allows for variations in Index pulse width, speed variations, and interchange tolerances between drives.

Pre-Index
The Pre-Index gap (Gap 4) is required to compensate for maximum speed variations between drives. Physically, the gap is the space between the last sector and the beginning of the index pulse.

Pre-Data
The Pre-Data gap (Gap 2) timing is determined by the erase turn-on circuit tolerance and the tunnel-erase structure of the read/write head.

Pre-ID
The Pre-ID gap length varies with sector size. The Pre-ID gap (Gap 3) is based on the tunnel-erase structure of the read/write head and maximum erase-circuit turn-off delay.

THE HARD (WINCHESTER) DISK DRIVE

The Winchester disk drive uses a non-removable 5 1/4-inch disk as storage media. The unit contains two disks and uses three recording surfaces, each of which is served by two heads. The total formatted capacity is 20M bytes. The disk controller interfaces the disk drive to the host processor. All necessary buffers and receivers/ drivers are included on the Winchester disk controller board to allow direct connection to the drive. Power requirements for the hard disk drive are given in Figure 5.26, pin assignments for the DC power connector are illustrated in Figure 5.27.

Voltage	Current
+12 Vdc	1.8 A typical, 2.2 A max. [4.0 A starting peek]
+ 5 Vdc	0.7 A typical, 1.4 A max. [1.4 A starting peek]

Figure 5.26 Power requirements

Pin	Connection
1	+ 12 Vdc
2	+ 12 V return
3	+ 5 V return
4	+ 5 Vdc

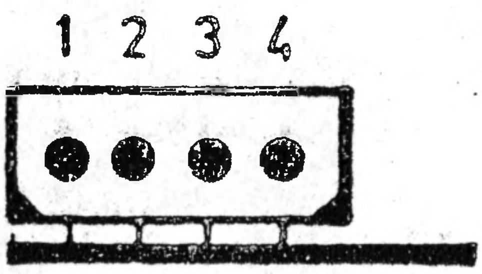


Figure 5.27 DC power connector

The NCR PERSONAL COMPUTER can use one or two hard disk drives in a daisy chain configuration. A terminator resistor pack must be installed in the end unit.

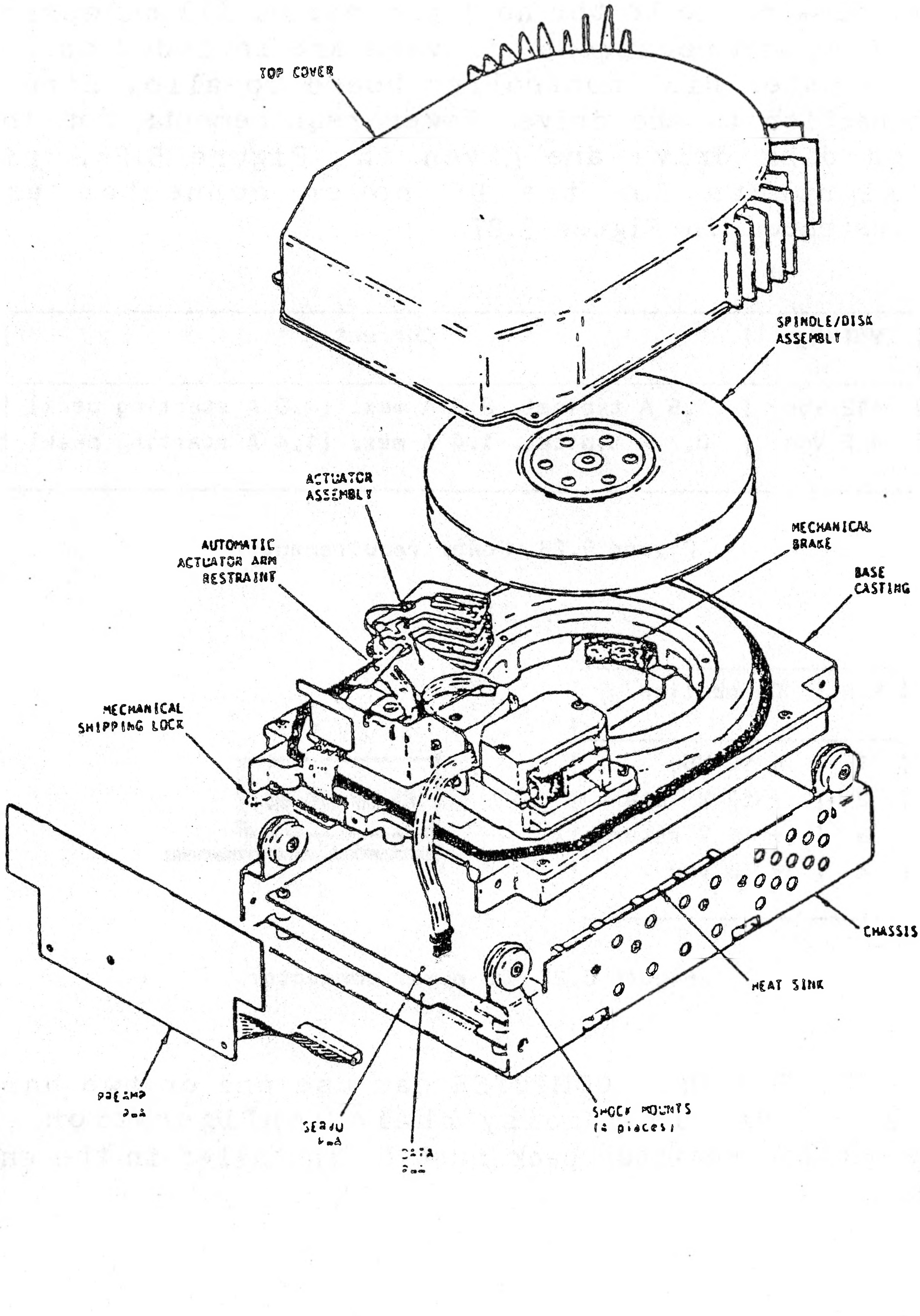


Figure 5.28 Fixed disk drive components

MBytes per unit (unformatted)	21.78
Tracks per inch	800
Tracks per surface	697
Bytes per track (unformatted)	10416
Bits per inch (MFM)	9550
Motor rotation speed	3600 rpm
Motor start time	< 35 s
Head movement:	
Average Seek	40 ms
Maximum Seek	90 ms
Average Latency	8.33 ms
Optimum step pulse rate	80 microsecs
Data transfer time	5M bits/sec

Figure 5.29 Technical data

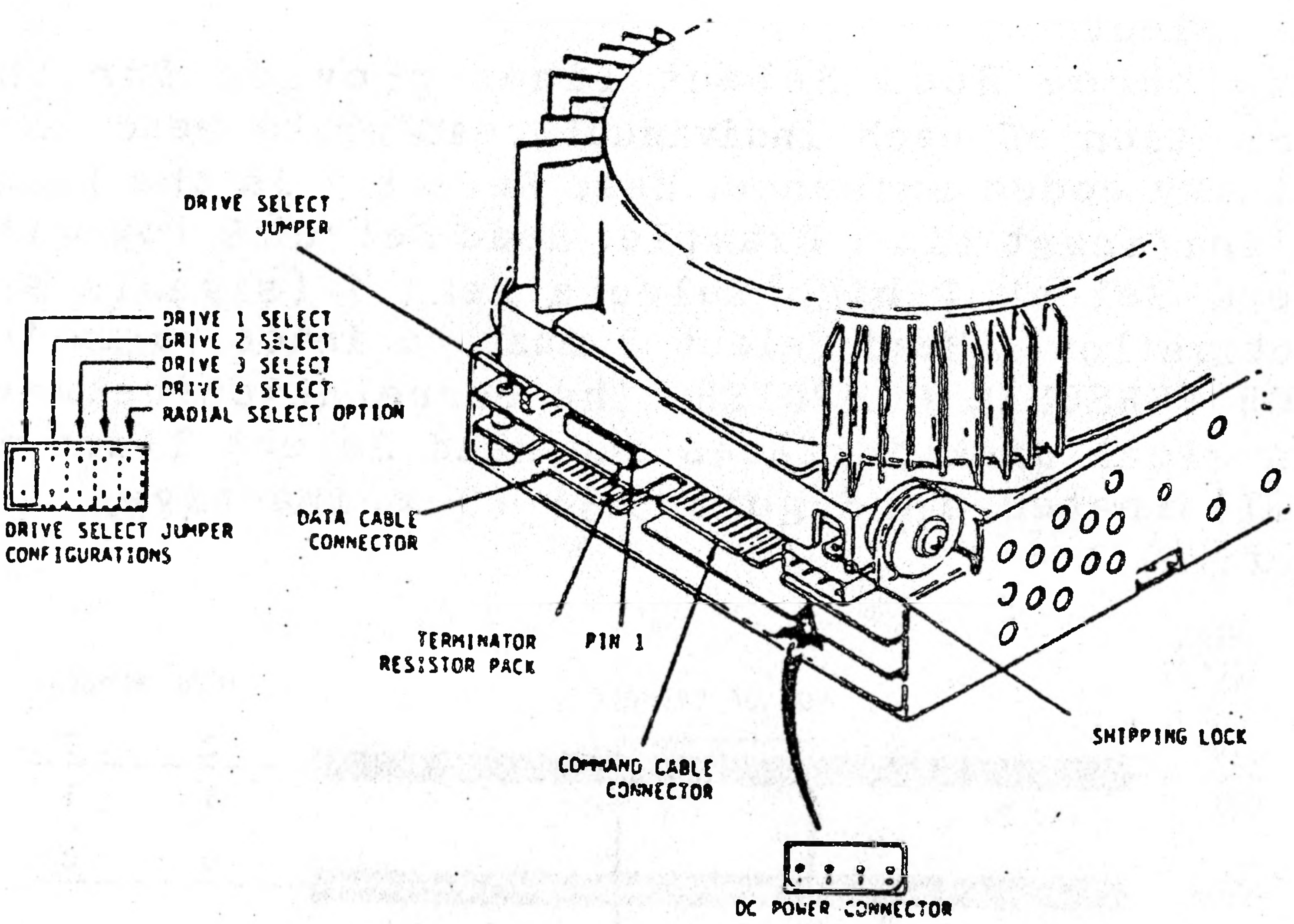


Figure 5.30 Connections and jumpers

CONTROL AND DATA SIGNALS

Figure 5.32 specifies the pin assignments of the control signal interface between controller and the drive. The corresponding edge connector is shown in Figure 5.33. Data in MFM format is transferred by means of a separate cable, for which pin assignments and edge connector are illustrated in Figures 5.34 and 5.35.

The input and output signals for the drive are:

Write Gate

The active state of this signal enables data to be written on the disk. If the Head Select is invalid, activation of this signal will cause an error. The inactive state of this signal enables data to be transferred from the drive.

This line must be inactive during the transmission nof step pulses.

Head select

The three Head Select lines provide for the selection of each individual read/write head in a binary coded sequence. Head Select 0 is the least significant line. Example: Head Select 0 low with Head Select 1 high selects head 1 (signals are active low). Head Select 2 must be inactive in the NCR PERSONAL COMPUTER. The correlation between physical disk durfaces and Head Select lines is illustrated in Figure 5.31 (0 = inactive, 1 = active).

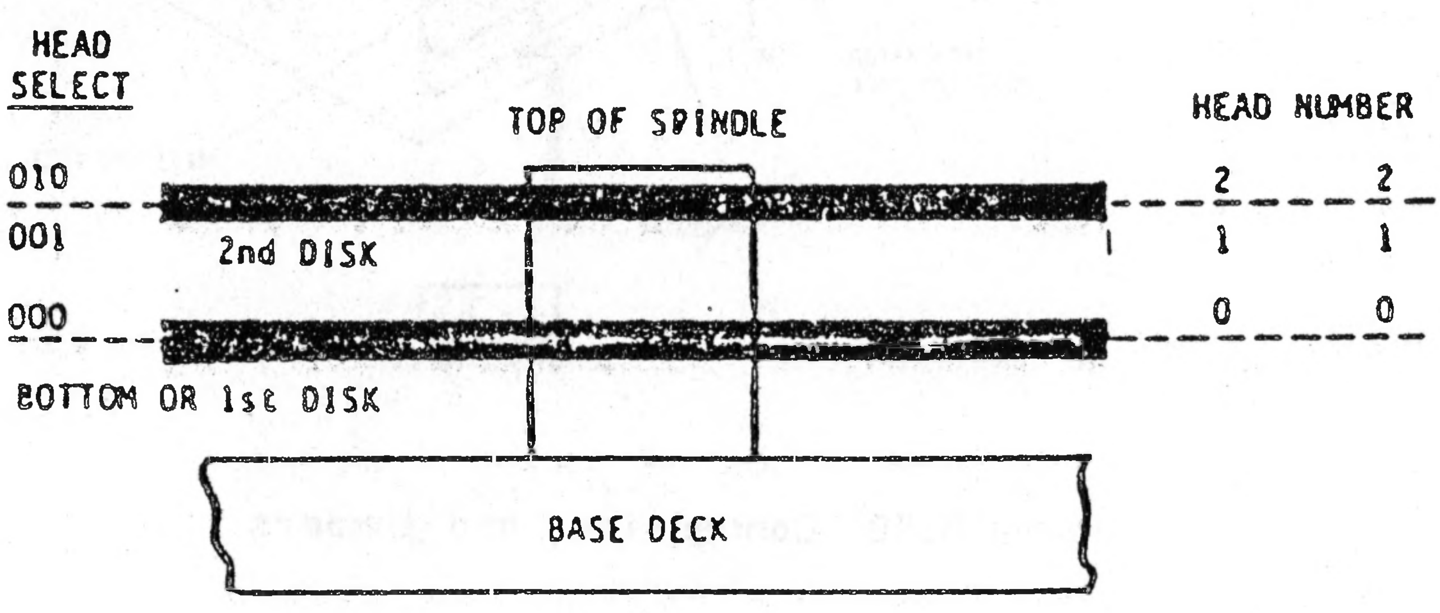


Figure 5.31 Hard disk head selection

Signal	Signal Pin	Signal Direction
REDUCED WRITE CURRENT or HEAD SELECT 3 (software selectable)	2	OUT
HEAD SELECT 2/	4	OUT
WRITE GATE/	6	OUT
SEEK COMPLETE/	8	IN
TRACK 0/	10	IN
WRITE FAULT/	12	IN
HEAD SELECT 0/	14	OUT
Connected internally to data pin 7	16	
HEAD SELECT 1/	18	OUT
INDEX/	20	IN
READY/	22	IN
STEP/	24	OUT
DRIVE SELECT 1/	26	OUT
DRIVE SELECT 2/	28	OUT
DRIVE SELECT 3/	30	OUT
DRIVE SELECT 4/	32	OUT
DIRECTION IN/	34	OUT
Odd numbered connections are Ground		

Figure 5.32 Hard disk controller/drive control signals

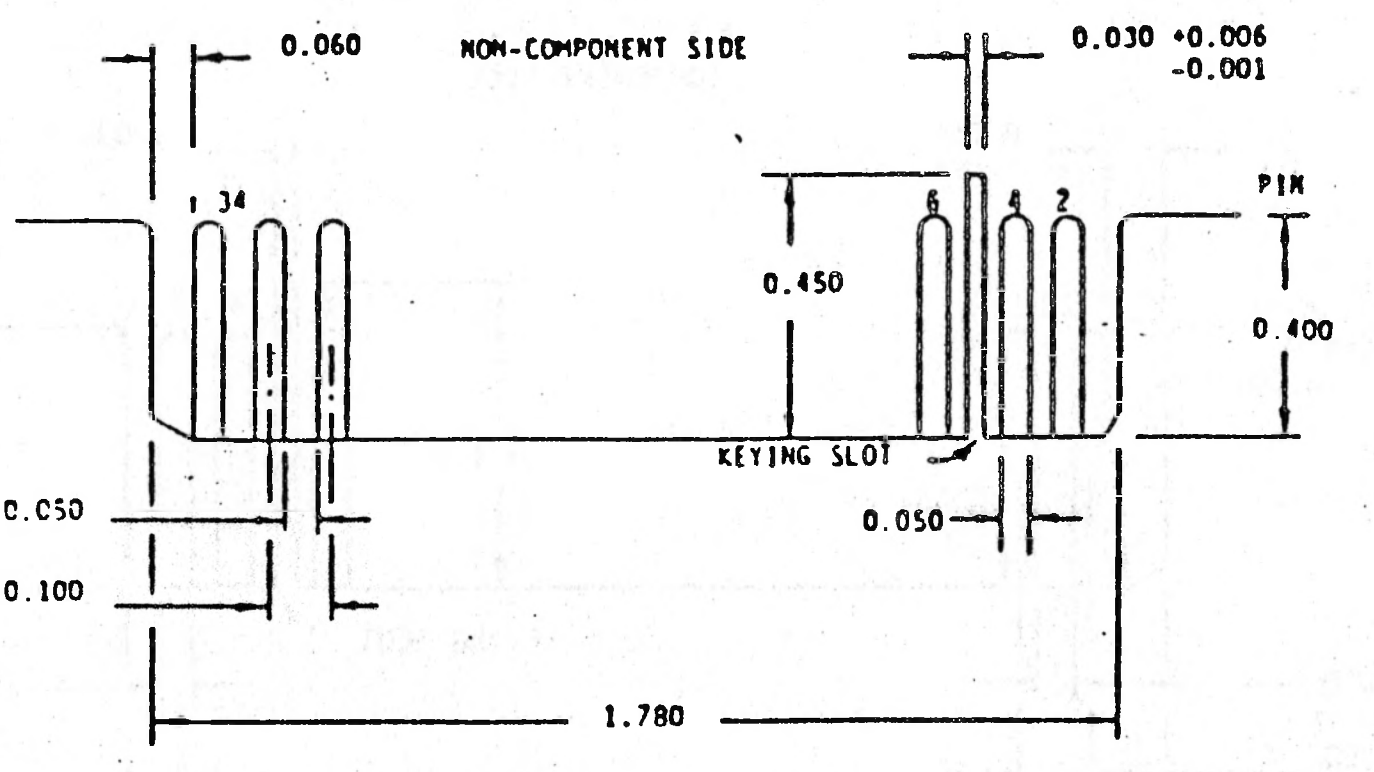


Figure 5.33 Hard disk: edge connector for control signals

Signal	Signal Pin
SELECTED/	1
Reserved	3
Reserved	5
Connected internally to control pin 16	7
Reserved	9
Reserved	11
GND	
GND	
MFM WRITE DATA	13
MFM WRITE DATA/	14
GND	
GND	
MFM READ DATA	17
MFM READ DATA/	18
GND	
GND	
Other connections are Ground	

Figure 5.34 Hard disk controller/drive data signals

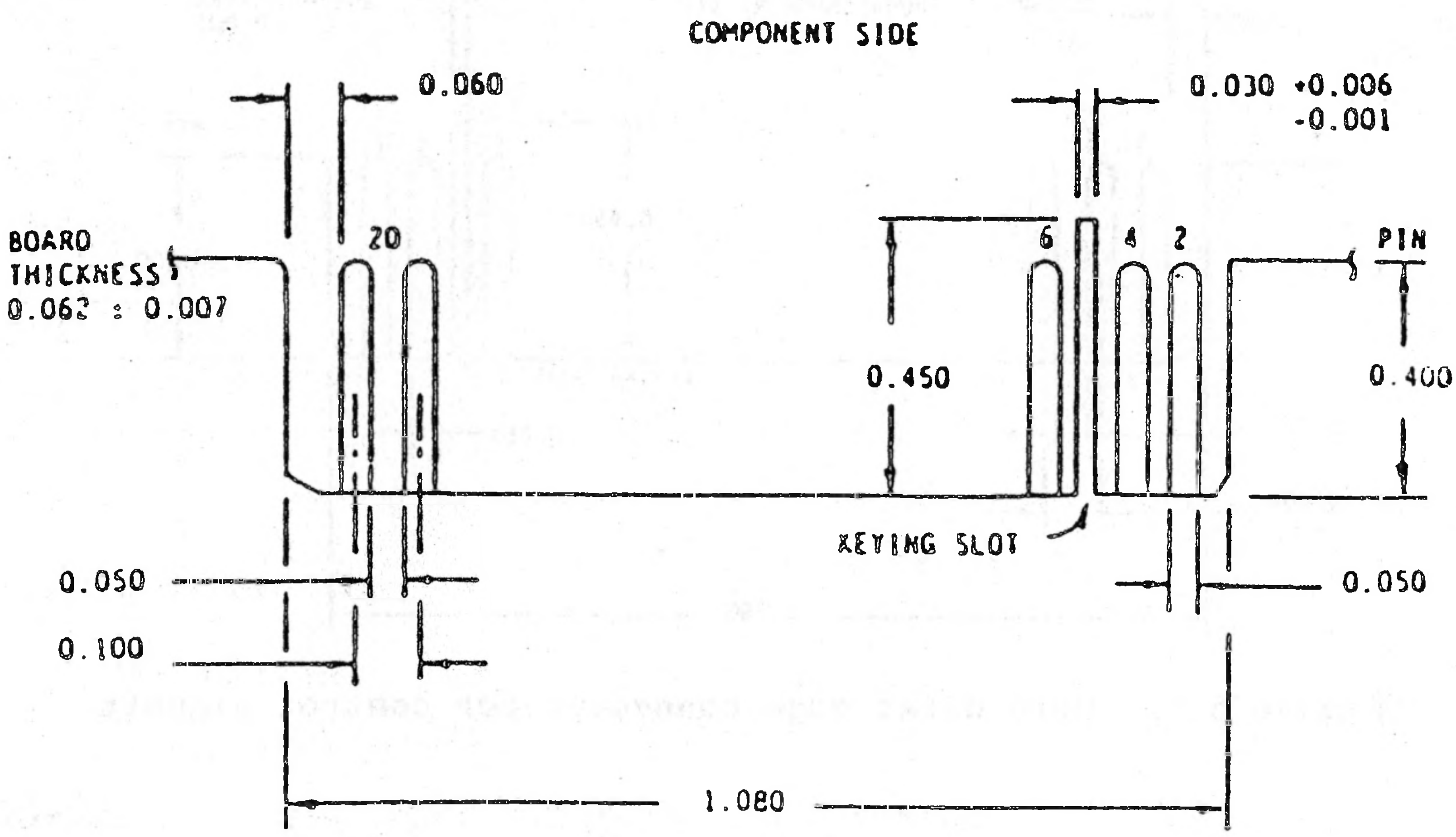


Figure 5.35 Hard disk: edge connector for data signals

Direction In

This signal defines direction of motion of the R/W head when the Step line is pulsed. Signal high defines the direction as "out" and if a pulse is applied to the Step line, the R/W head moves away from the center of the disk towards track 0. If this line is signal low, the direction of motion is defined as "in" and the R/W head moves toward the center of the disk. Direction must not change during step time.

Step

This interface line is a control signal which causes the R/W head to move with the direction of motion defined by the Direction In line. Any change in the Direction In line must be made at least 100 ns before the leading edge of the step pulse.

The drive accepts step pulses from the controller in one of two possible modes, track-to-track or buffered. Track-to-track mode is possible when the interval between step pulses is 3 ms or greater. In buffered mode, steps are accumulated and then issued at a rate between 8 and 200 microseconds. Note that the acceptance of track-to-track stepping is provided for compatibility purposes only. The actual stepping mode used by the drive is always buffered.

An attempt to position the head outside the recording zone will result in a re-positioning at Track 0.

Drive Select 1 - 3

Drive Select, when active, connects the drive interface to the control lines. Jumpers are provided on the drive which are set in a specified pattern so as to determine which unique select line on the interface will activate that particular drive (see Figure 5.30).

Seek Complete

This line will go from inactive to active when the R/W heads have settled on the final track at the

end of a seek. Reading or writing should not be attempted when Seek Complete is inactive.
Seek Complete must go inactive for any of the following cases:

1. A recalibration sequence is initiated by drive logic, e.g. as the result of stepping outside the recording zone
2. Within 500 ns after the leading edge of a step pulse or series of step pulses
3. At power on or after a power interruption

Track 0
This interface signal is active only when the drive's R/W heads are positioned at track 0 (the outermost data track).

Write Fault
This signal indicates that a condition exists at the drive that would cause improper writing on the disk. When this line is active, further writing is inhibited at the drive until the condition is corrected. Once corrected, this line can be reset by de-activating the Write Gate or deselecting the drive.
There are four conditions which can cause Write Fault to be activated:

* Write current malfunction:
  Write current in a head without Write Gate active
  or
  Write Gate and Drive Select active with no write current in a head
* A drive malfunction causing more than, or less than, one head to be selected, or a malfunction causing a head to be selected for read during write or for write during read
* DC voltages are grossly out of tolerance.
* Write Gate and an inactive condition on Seek Complete

Index

This interface signal is provided for 200 microseconds by the drive once each revolution (nominally 16.67 ms) to indicate the beginning of the track. This signal is normally inactive and makes the transition to active to indicate Index.

Ready

This interface signal, when active together with Seek Complete, indicates that the drive is ready to read, write, or seek and that the I/O signals are valid. When this line is inactive, all writing, reading, and seeking is inhibited. Ready should be inactive only as a result of and during recovery from a power off condition: Ready is normally asserted no later than 35 seconds after power on.

MFM Write Data

This is a differential pair that defines the transitions to be written on the track. The transition of +MFM Write Data line going more positive than the -MFM Write Data will cause a flux reversal on the track, provided Write Gate is active. This signal must be driven to an inactive state (+MFM Write Data more negative than -MFM Write Data) by the host system when in a read mode. Integrity of data writing, especially on inner tracks, is ensured by pre-compensation being active. Data patterns which cause a large amount of bit shift have appropriate data bits shifted early or late with respect to the nominal bit cell position. Bit shift compensation, whether early or late with respect to the nominal bit cell position, is 12ns.

MFM Read Data

The data recovered by reading a pre-recorded track is transmitted to the host system via a differential pair of MFM Read Data lines. The (pre-compensated) transition of the +MFM Read Data line going more positive than the -MFM Read Data line represents a flux reversal on the track of the selected head.

Figures 5.36 to 5.40 illustrate timing considerations.

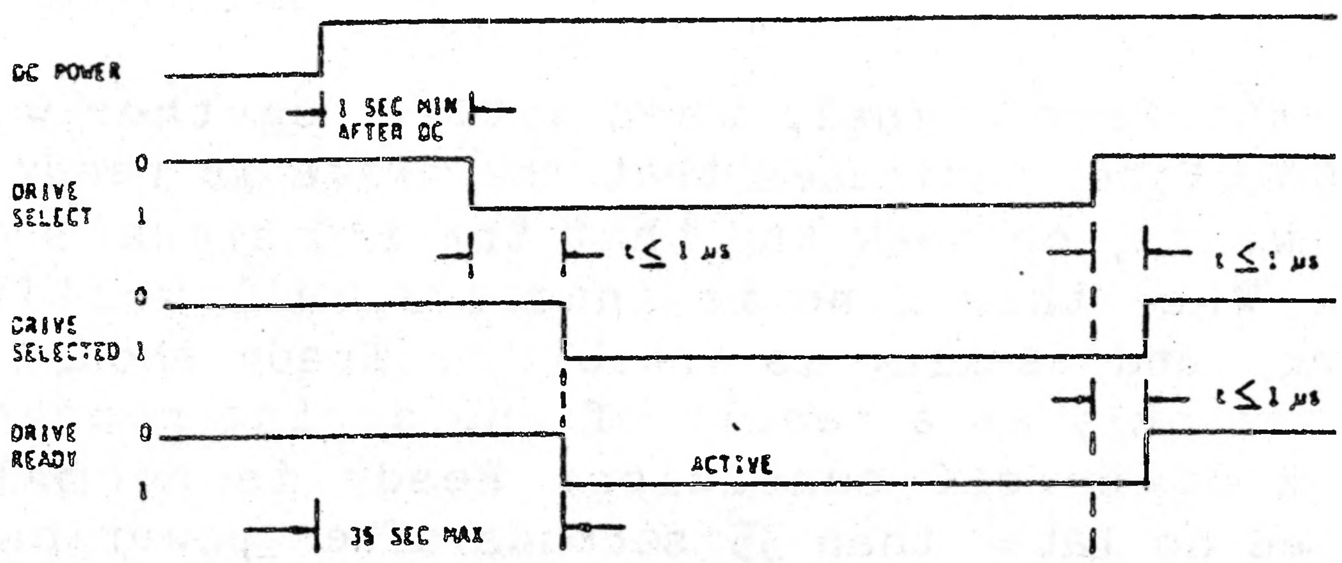


Figure 5.36 Power-on and drive select timing

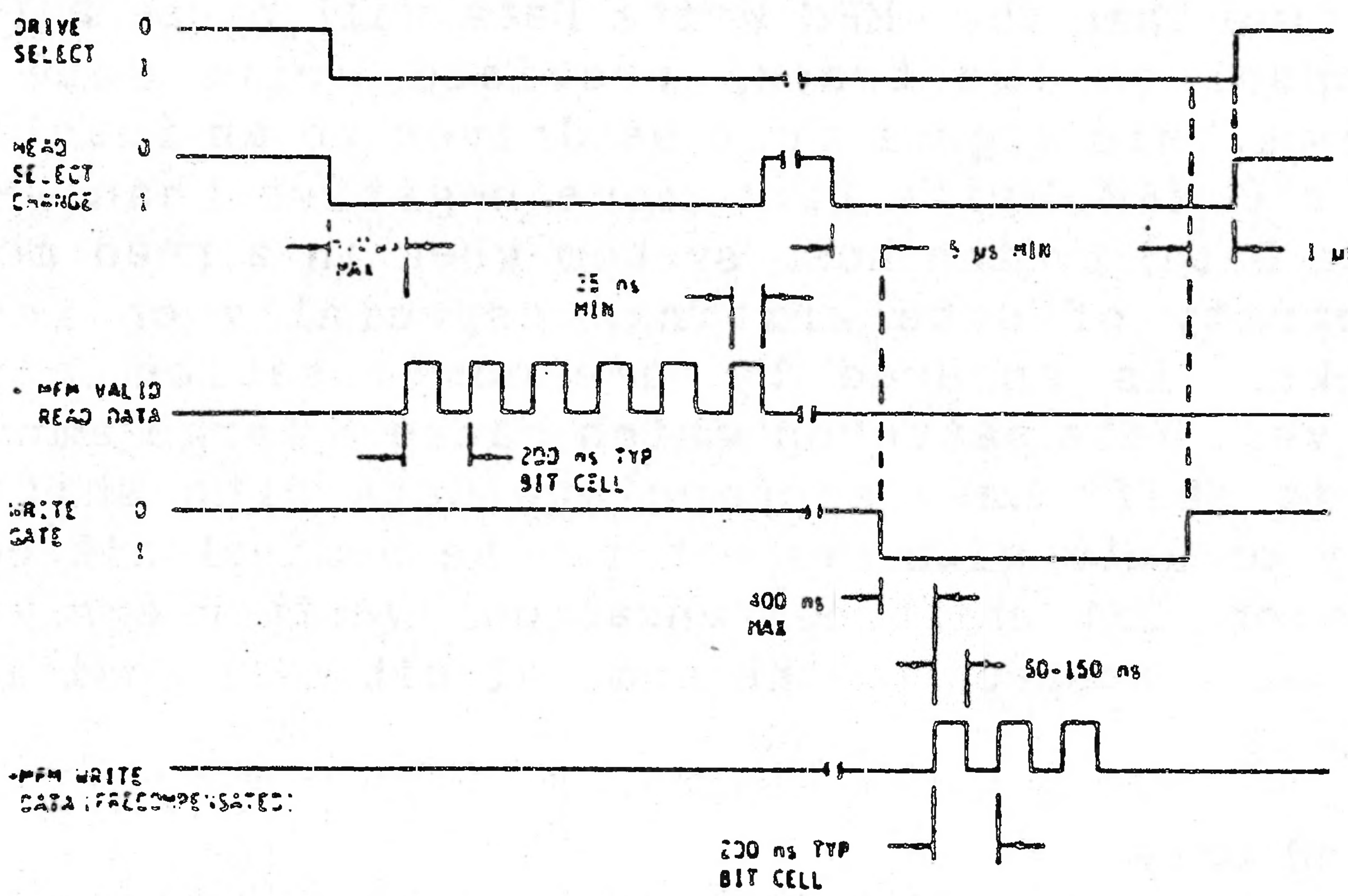


Figure 5.37 Head select timing

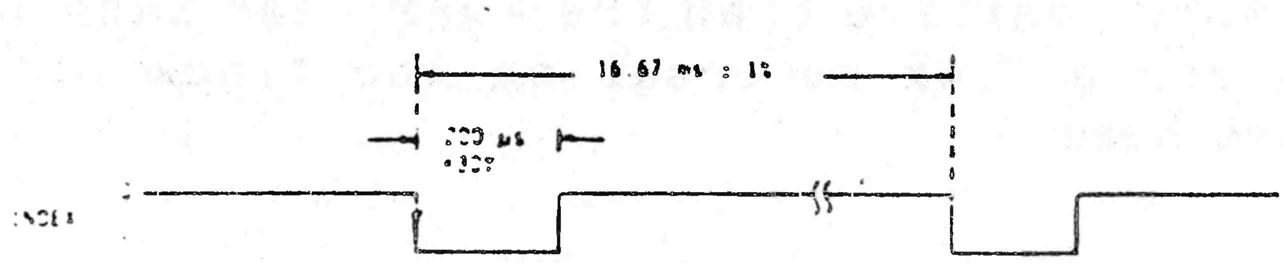


Figure 5.38 Index timing

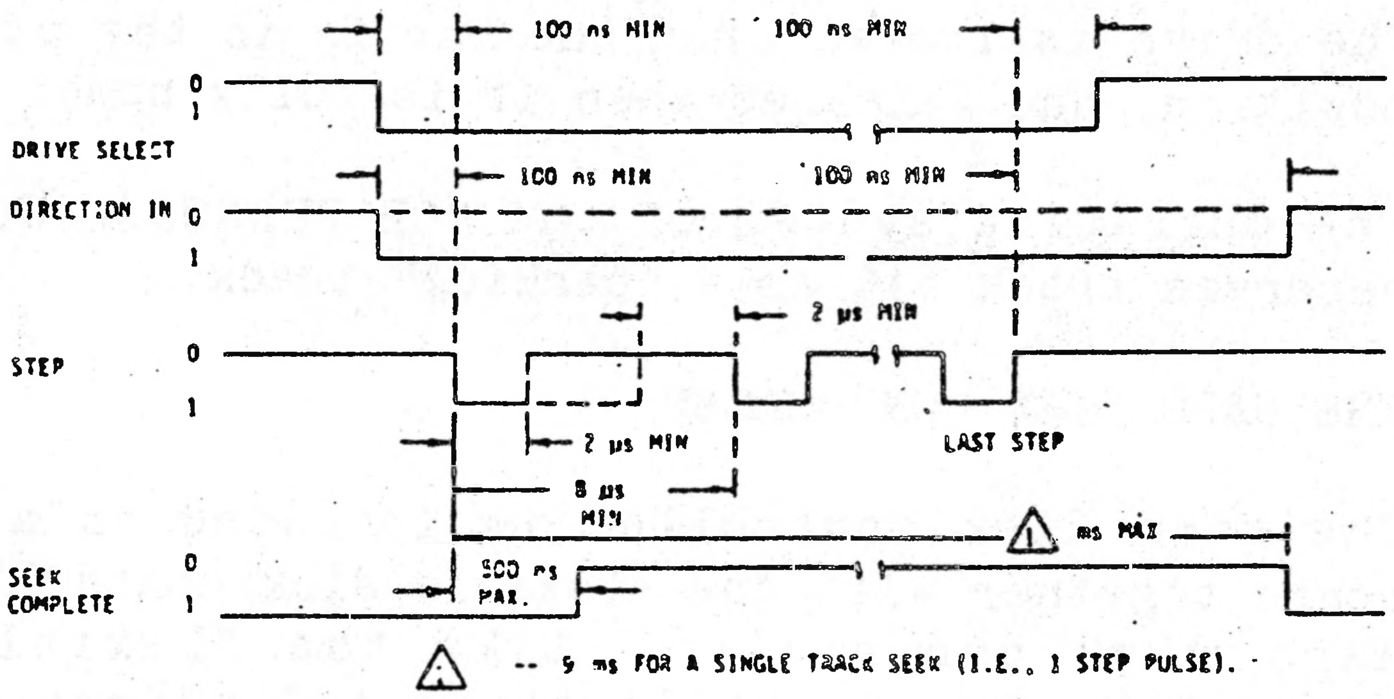


Figure 5.39 Track access timing

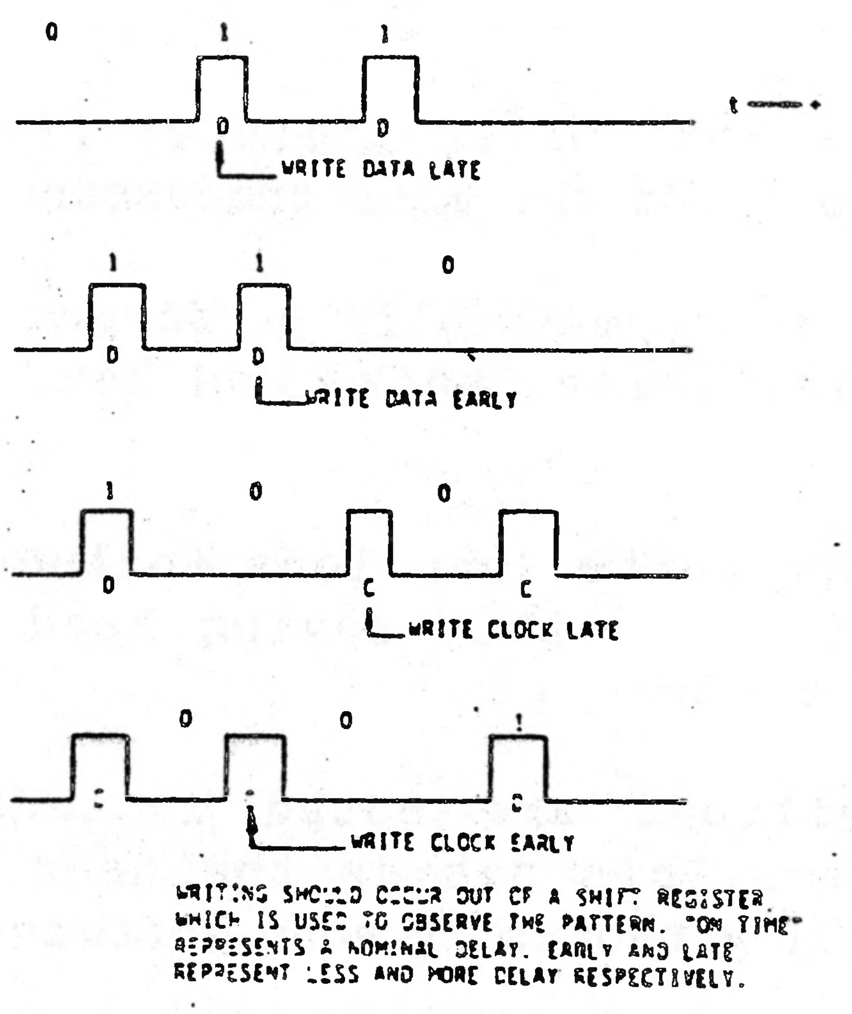


Figure 5.40 Write pre-compensation

TRANSIT PRECAUTIONS

A metal bar is included in the drive housing, providing a shipping lock to prevent transit damage to the drive. The location of this bar is illustrated in Figure 5.30.

The drive is locked when the bar is in the withdrawn position, and released when it is fully home.

The operating system of the NCR PERSONAL COMPUTER reserves track 615 as a "parking" track.

THE HARD DISK CONTROLLER

The hard disk controller is included on a single board together with the flexible disk controller. The hard disk controller, like the flexible disk controller, uses two distinct I/O address areas, according to whether primary or secondary addresses are selected by means of jumpers on the disk controller board (see Figure 5.13). Hard disk controller activity uses interrupt request 0EH (IR6 of PIC #2).

The hard disk controller includes features which considerably offload the microprocessor:

* Retries are automatically performed, even on ECC (Polynomial Error Check) and head positioning errors

* Basic read/write functions include an implied seek operation, thus saving head positioning control software

* Head positions are noted internally by the controller. This avoids the need to maintain corresponding tables in your software

* Data reading and writing is buffered internally, thus facilitating interruption

* Multiple sector reading and writing

The interface between controller and the system is via ports with read/write I/O addresses in the range 1F0H to 1F7H (primary) or 170H to 177H (secondary):

1F0H/170H	Data register
1F1H/171H	Read: error register Write: write pre-compensation
1F2H/172H	Sector count
1F3H/173H	Sector number
1F4H/174H	Cylinder low
1F5H/175H	Cylinder high
1F6H/176H	Size/Drive/Head
1F7H/177H	Read: status register Write: command register

Status Register

Figure 5.41 sets out the significance of the status bits read via port 1F7H/177H. Reading the status register clears the controller's interrupt request. If bit 7 is set, other bits in the register are undefined.

Status bit	Description
0	1 = an error has occurred and the Error Register should be inspected; multi-sector operations are terminated. Bit is reset upon issue of a command
1	Index signal set as long as the Index pulse is active
2	1 = data was successfully corrected by ECC (this does not terminate multi-sector operations)
3	1 = sector buffer is expecting a (further) read or write operation
4	Seek Complete signal 1 = completed seek operation
5	Write Fault signal 1 = read/write/seek inhibited
6	Drive Ready signal 1 = drive can read/write/seek, provided that bit 4 is set 0 = read/write/seek inhibited
7	1 = controller busy: access to registers is not possible (any read attempt defaults to Status register) 0 = registers can be read/written

Figure 5.41 Status Register

Command Register

Eight commands can be issued by the controller via port 1F7H/177H. For a comand to be issued, the Status Register (read at port 1F7H/177H) must indicate that the drive is not busy, the Drive Ready and Seek Complete signals must be active, Write Fault must not be active. Issuing a command resets the hard disk controller interrupt request to the system.

Valid hard disk controller commands:

Restore heads to track 0
Seek
Read Sector
Write Sector
Format Track
Verify
Diagnose
Set Drive Parameters

The format of these commands is summarized in Figure 5.42. Any invalid format written to port 1F7H/177H will cause the "Aborted Command" error bit to be set in the Error Register.

A number of commands involve implied Seek operations. The stepping rate used is as most recently set by the Restore or Seek command, or the default value of 7.5 ms following a Diagnose command or controller reset.

The 4-bit stepping rate value included in the Restore and Seek commands is as follows:

0000 = 35 microseconds

0001 to 1111 =
0.5 to 7.5 ms in increments of 0.5 ms

The L bit included in some commands determines whether the data transfer is to be "long", that is, including the four ECC bytes (bit set), or whether data without ECC bytes is to be transferred (bit zero).

Command	Bit: 7	6	5	4	3	2	1	0
Restore	0	0	0	1	< Stepping Rate >			
Seek	0	1	1	1	< Stepping Rate >			
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

Figure 5.42 Command summary

Setting the T bit limits the number of retries to one. Otherwise, the drive performs retries up to the following maximum:

10 retries, followed by

drive recalibration, followed by

10 retries

This maximum is drive-specific, and cannot be infuenced by the hard disk controller.

For commands requiring disk location information (drive, cylinder, track, sector), it is necessary to have previously supplied this information by means of the appropriate controller registers.

RESTORE
Moves the heads outwards until the Track 0 signal becomes active. The cylinder registers are reset. An interrupt is then issued.

SEEK
Positions the heads at the specified cylinder, and then issues an interrupt.

READ SECTOR
Reads the specified sector from the hard disk drive. This command includes an implied Seek. A Restore to Track 0 is not implicit, so that no track-to-track head movement is required if the head is currently positioned over the right track.
An intrrupt indicates that data is available for reading from the Data Register.
If the L bit is set, no error checking is performed.

WRITE SECTOR
Writes data already placed in the Data Register to the specified sector. This command includes an implied Seek. A Restore to Track 0 is not implicit, so that no track-to-track head movement is required if the head is currently positioned over the right track.
An interrupt indicates that the command has been carried out.
If the L bit is set, no error checking is performed.

FORMAT TRACK
Delinates data fields and writes identification fields on the specified track using the interleave table already in the sector buffer (written via the Data Register). The interleave table written to the sector buffer consists of two bytes for each sector:

First byte -	00 (80H for bad block)
Second byte -	logical sector no. for the first physical sector
Third byte -	00 (80H for bad block)
Fourth byte -	logical sector no. for the second physical sector

an so on

The remaining bytes of the 512-byte sector buffer should also be written. The hard disk format utility of the NCR-DOS operating system uses an interleave jump of 3.

The actual number of sectors to be formatted on the track is determined by the Sector Count Register. Note that this register must be written separately for each track formatted.

VERIFY
Performs a verification of a previous write to the sector(s) specified. Upon completion of the single-sector or multi-sector verify, an interrupt is issued. Status should then be checked for errors. The command aborts in the event of an error.

DIAGNOSE
Controller performs internal diagnostics, issues an interrupt, and reports any errors in the Error Register.

SET PARAMETERS
This command must be issued so that the drive can perform multi-sector operations. The following parameters must be deposited in other controller registers before this command is issued:

Max. head no. in specified drive	in Size/Drive/Head Register
No. of sectors per track	in Sector Count Register

Data Register

The Data Register provides 16-bit access to the 512-byte sector buffer on the disk controller board. However, ECC information (transferred in "long" read/write operations) must be read or written byte by byte, allowing 2 microseconds between transfers, and the DRQ signal must be active.

Error Register

The significance of the Error Register bits differs according to whether the controller is diagnostic or or normal mode.

Diagnostic mode applies at power-on, or when the Diagnose command is being executed. In diagnostic mode, only the 3 LSBs are significant: value 1 = no error, value 3 = sector buffer error, values 2, 4, 5 = other error.

In the normal mode of operation, the Error Register bits are used as stated in Figure 5.43.

Error bit	Description (bit set)
0	Data address mark not found during Read operation
1	Track 0 signal did not become active during a Restore command
2	An invalid command was issued or A command was issued although drive was not Ready or A command was issued while Write Fault was asserted
3	Not used
4	Sector ID could not be found or CRC error in ID field. This bit is set, and remains set, even if the error is recovered during a retry. If error is unrecoverable, the Status Register is also affected (bit 0)
5	Not used
6	ECC data field error. This bit is set, and remains set, even if the error is recovered by a retry. If the error is recoverable, Status Register bit 2 is set, otherwise Status Register bit 0 is set
7	ID field contains a "bad block" mark

Figure 5.43 Error Register

Pre-compensation Register

An 8-bit register specifying the number of the cylinder, divided by 4, from where write pre-compensation is to be applied.

Size/Drive/Head Register

This register is made up as shown in Figure 5.44.

Bit:	7	6	5	4	3	2	1	0
	1	0	1	DRIVE	<—— HEADS ——>			

Figure 5.44 Side/Drive/Head Register

DRIVE is zero for first hard disk drive, set for the second hard disk drive.

HEADS is a binary value for the maximum number of heads in the drive.

Cylinder High and Low Registers

A 16-bit value specifying a cylinder number. The controller notes internally its current cylinder position. By comparing its internal note with the value specified in these two registers, it can determine the direction in which stepping must take place.

Sector Number Register

In single-sector operations, this is the sector to be accessed. In multi-sector operations, this register specifies the first sector to be accessed. The controller updates this register as it read/writes sectors.

Sector Count Register

The controller automatically decrements this register each time a sector is accessed. If you specify a value of 1, the subsequent operation is single-sector; otherwise a multi-sector operation is performed, even across cylinder boundaries (value 0 specifies 256 sectors).

Hard Disk Register

A write-only register is located at port adresses 3F6H/376H. Using this register, additional control information can be written to the hard disk controller. Only bits 1-3 are significant:

Bit 1 controls interrupt request 0EH:

0 = interrupt request enabled
1 = disabled

Bit 2 controls drive reset:

0 = normal operation
1 = perform reset

Bit 3 controls use of pin 2 of the drive control connector:

0 = pin is Reduced Write Current
1 = Head Select 3

Signal Status

Reading port 3F7H/377H yields information about the current state of a number of control lines to the hard disk drive(s). This is set out in Figure 5.45. Note that bit 7 is used by the flexible disk controller to indicate a diskette change.

Bit	Signal	
0	Drive Select 0	
1	Drive Select 1	
2	Head Select 0	
3	Head Select 1	
4	Head Select 2	
5	Head Select 3 or Reduced Write Current	selected via port 3F6H/376H
6	Write Gate	
7	Diskette change	

Figure 5.45 Signal status

Hard Disk Format

The sector format is illustrated in Figure 5.46.

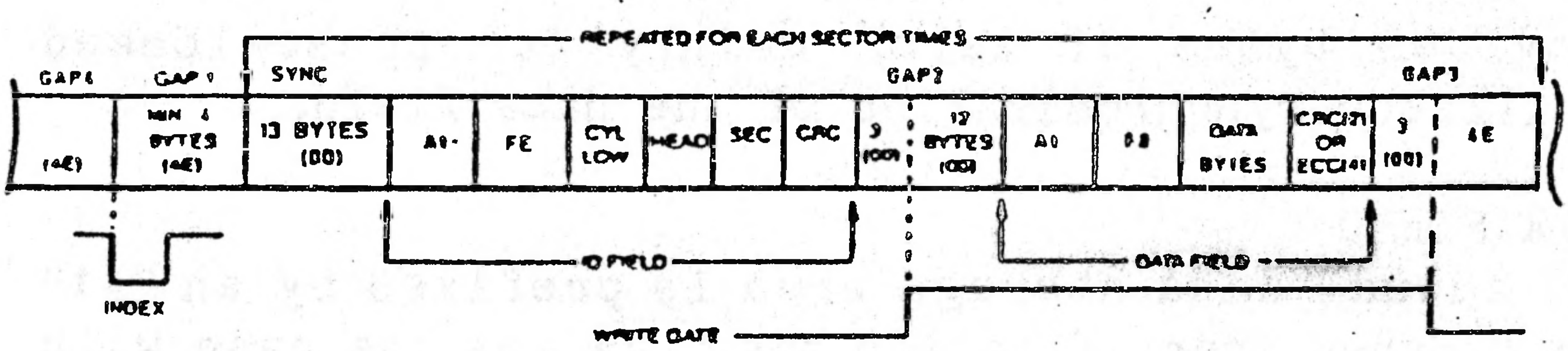


Figure 5.46 Hard disk format

GAP 1
Provides a head switching recovery period and controller decision making period so that that when switching from one track to another, sequential sectors can be read without waiting the entire rotational latency time (the controller can read the last sector of a track, perform a head change, and read the first sector of a new track).
The minimum Gap 1 is 4 bytes, but 16 are usual.

SYNC
Allows the controller's phase-locked oscillator to become phase and frequency synchronized with MFM flux reversals. This is necessary so that clock and data bits can be distinguished from one another.

ID FIELD
Identifies track and sector. The address mark (AM) is a unique MFM encoded data pattern indicating the start of the ID field and synchronizing with the ensuing bit stream. The "A1" byte is made unique by the controller by omitting one clock bit. This is followed by a single identification byte.
CYL LOW contains the 8 LSBs of the cylinder number.
HEAD contains the upper bits of the cyliner number in bits 0-6. Bit 7 denotes whether the sector is good (zero) or defective (set).
SEC contains the sector number.
Then follow 2 bytes for ID CRC checking.

GAP 2
Provides bytes of zero, mainly for phase-locked oscillator synchronization of the data field.

DATA FIELD
The actual data storage area is prefixed by an "A1" and further identification byte, as was the case with the ID field.
The data field is concluded by four ECC bytes.

GAP 3
The zero bytes allow time for ECC checking. The ensuing "4E" bytes allow for variations of spindle

speed between formatting and writing. The number of these bytes depends on nominal motor speed.

GAP4

Provides a speed tolerance gap for the entire track. This gap, like Gap 3, can vary according to rotational speed.

The Loudspeaker

HARDWARE CHARACTERISTICS

The NCR PERSONAL COMPUTER MODEL contains a small loudspeaker, mainly used to attract operator attention in application programs. The loudspeaker is driven by a TTL signal, amplified by a transistor.

The driving signal is a square wave derived from output line OUT2 of the 8254 programmable interval timer (sse Chapter 2). The actual frequency is determined by the value loaded in the counter for that timer output.

The output from the timer to the loudspeaker amplification and volume control circuitry is AND gated with a latch responding to data line 1 when I/O address 61H is selected. Therefore, sound is turned on and off by writing to port 61H with data bit 1 set or zero.

That the CPU does not have to directly pulse the loudspeaker in relation to the desired frequency means that sound effects can take place while other instructions are being processed.

PROGRAMMING MUSIC

If you wish to program music, you will find the table of frequencies and their respective notes in musical notation useful (Figure 6.1).

To obtain timer counter 2 values to produce one of these frequencies, it is necessary to perform jumbo arithmetic: place the frequency in Hz in CX. The value 1234DCH in DX-AX is then divided by CX to yield a 16-bit result in AX. This value is then output to the counter, low byte then high (a division remainder can be ignored).

Note	Frequency (Hz)	Note	Frequency (Hz)
A	220	F#	740
A#	233	G	784
B	247	G#	830
C	262	A	880
C#	277.2	A#	930
D	293.6	B	987.8
D#	311.6	C	1046.4
E	329.6	C#	1106
F	349.2	D	1174.6
F#	370	D#	1244
G	392	E	1318.6
G#	416	F	1397
A	440	F#	1480
A#	466	G	1568
B	493.2	G#	1660
Middle C	523.2	A	1760
C#	554.8	A#	1864
D	587.4	B	1975.6
D#	622	C	2093
E	659.2	C#	2217.4
F	698.4	D	2349.4

Figure 6.1 Music frequencies

Display Control

The 3299-K201 graphic display adapter supplied with the NCR 3295-2010 Color Monitor supports "all points addressable" graphics and contains a 32 KB memory.

The 32 KB memory of the graphic display adapter can be upgraded to 64 KB (3299-K202), thus providing high resolution (640 x 400 pixels!) color capability.

The display adapter uses a 6845 controller. A dual port configuration is used so that CPU access and CRT controller can access video RAM independently of one another. All video RAM lies within the CPU "read address" area.

It is important that you install the display adapter supplied with the monitor. This is because the frequency characteristics differ from one type of monitor to another.

CAUTION: Before connecting an external monitor, you must ensure that it is truly TTL compatible. A number of monitors available claim to conform to this norm, but in fact drain excessive current from the adapter.

ADAPTER CONNECTION

A 9-pin D-shell connector interfaces to the external monitor. Figure 7.1 shows the pin connections of the 3299-K201 display adapter. Figure 7.2 illustrates the signals for the light pen connector.

Pin	Signal
1	VIDEO-LO
2	HSYNCP
3	RED/
4	GREEN/
5	BLUE/
6	INTENSITY/
7	VSYNC/
8	HSYNC/
9	GROUND

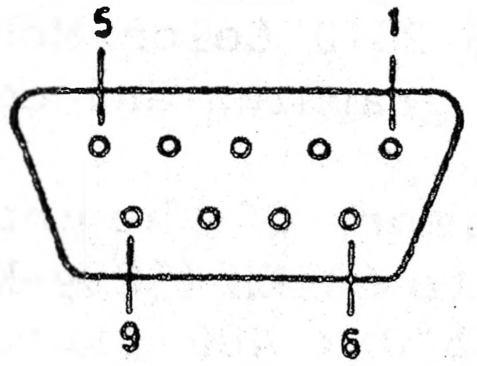


Figure 7.1 D-connector pin assignments

Pin	Signal
1	LPENINPUT/
3	LPENSW/
4	LGRD
5	+5V
6	+12V

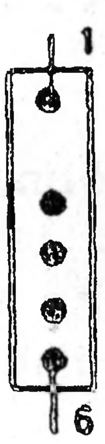


Figure 7.2 Light pen connector

CHARACTER DISPLAY

THE CHARACTER SET

The NCR PERSONAL COMPUTER draws upon two character sets. In the character mode of display a set of 256 characters can be displayed on the screen. This character set, for the most part consisting of 6 (horizontal) x 9 pixel patterns in 8 x 16 matrices, is produced by a character generator which is not accessible to software. If your application requires the pixel patterns of this character set (for example, for character magnification), you can load a corresponding graphic table into user memory by means of the GRAFTABL utility under your NCR-DOS operating system. This table is required, for example, for the 640 by 400 pixel graphic resolution of GW-BASIC.

The lower part of this graphic table (that is, for character codes 0 to 7FH) is held in read only memory, starting at the machine address 0D800H offset to the beginning of the ROM at paragraph 0F000H in the normal machine memory map (the ROM is not switched), and extending over 2048 bytes (128 characters each of 16 bytes). This lower part is, therefore, always available for program reading.

The higher part (character codes 80H to 0FFH) is loaded with the NCR-DOS executable file GRAFTABL into user memory. Assuming that you specify high resolution in response to the GRAFTABL menu, this higher part of the table is retained in user memory even after the return to the parent process (using the NCR-DOS function call "Terminate but Keep Process"). The exact location of the first 16 x 8 pattern byte (that is, for the character with code 80H) is the byte with a positive offset of 400H to the Code Segment + Instruction Pointer value held in the CPU interrupt vector entry for interrupt type 1FH. This entry is set by the GRAFTABL program. Example: if the four bytes starting at machine address 7CH (= vector entry for interrupt type 1FH) are 03H-01H (IP) 91H-06H (CS) in that order (the CS value can vary according to the program segment set up by NCR-DOS), the beginning of this higher part graphics table is located at the hexadecimal paragraph:offset address 0691:0503, and the top 8-pixel line for the graphics character with code 81H is stored in the byte 0691:0513.

The pixel patterns for this 16 x 8 character set are illustrated in Figure 7.3.

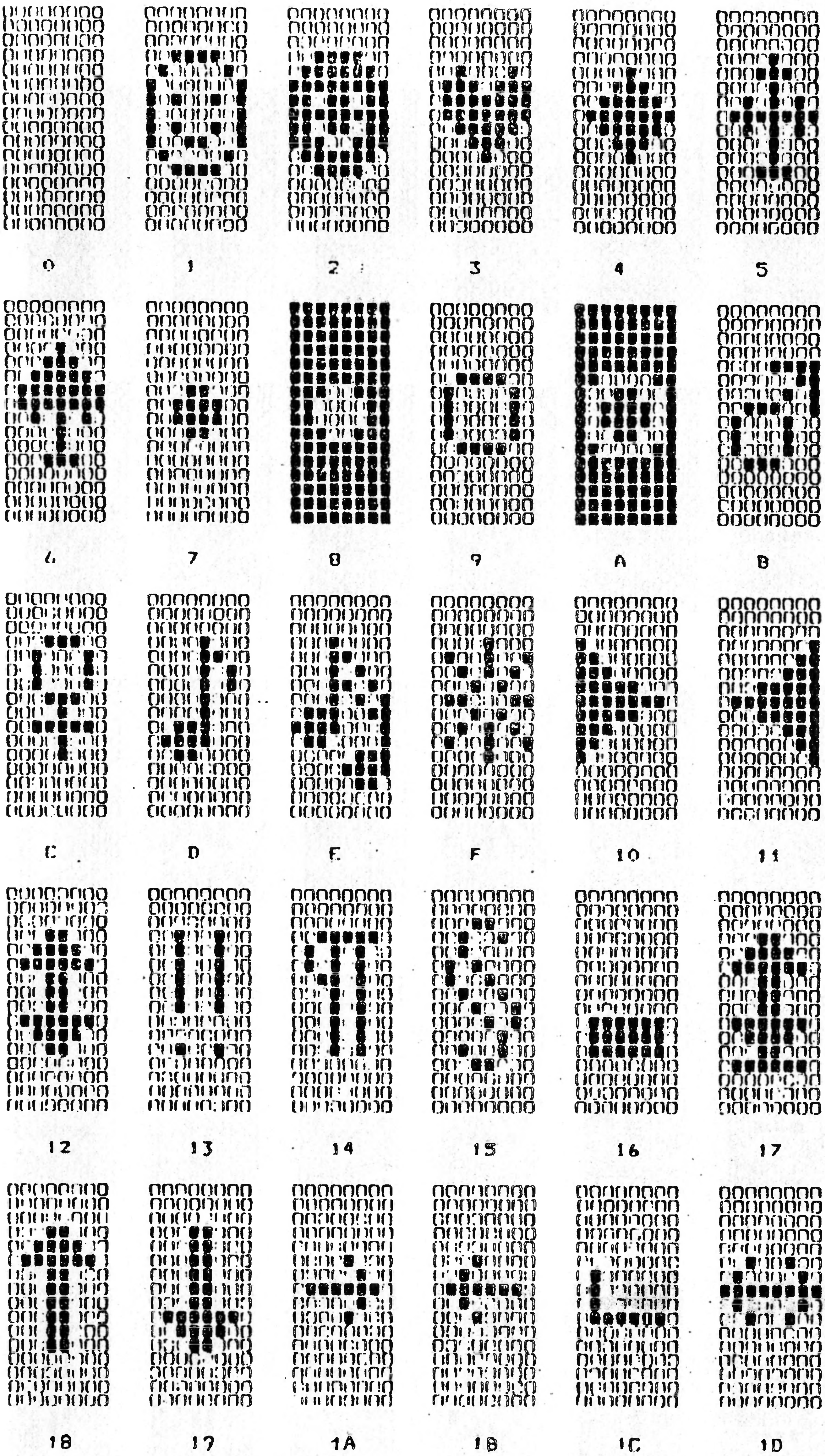


Figure 7.3 The main character set [1 of 9]

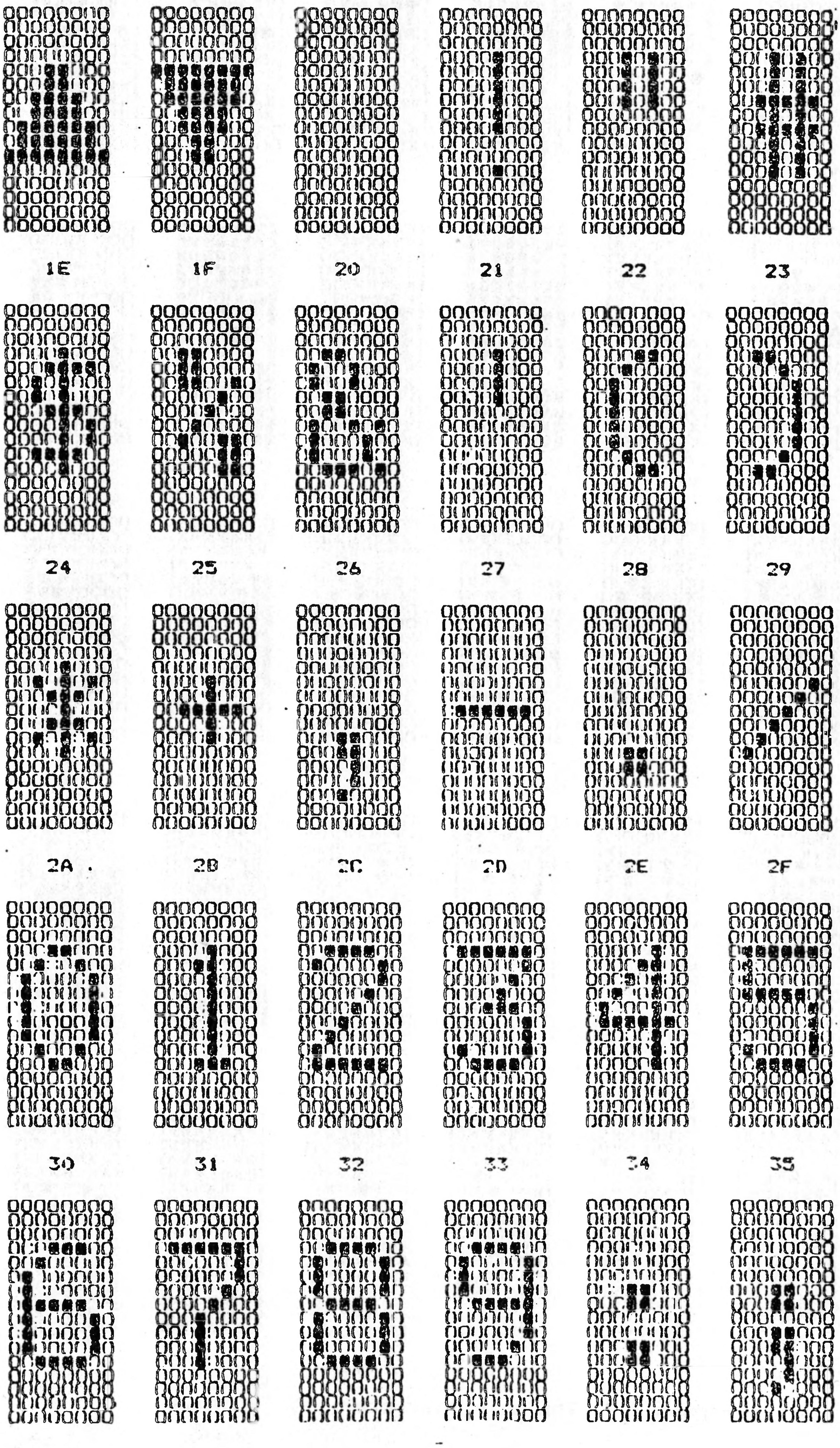


Figure 7.3 The main character set (2 of 9)

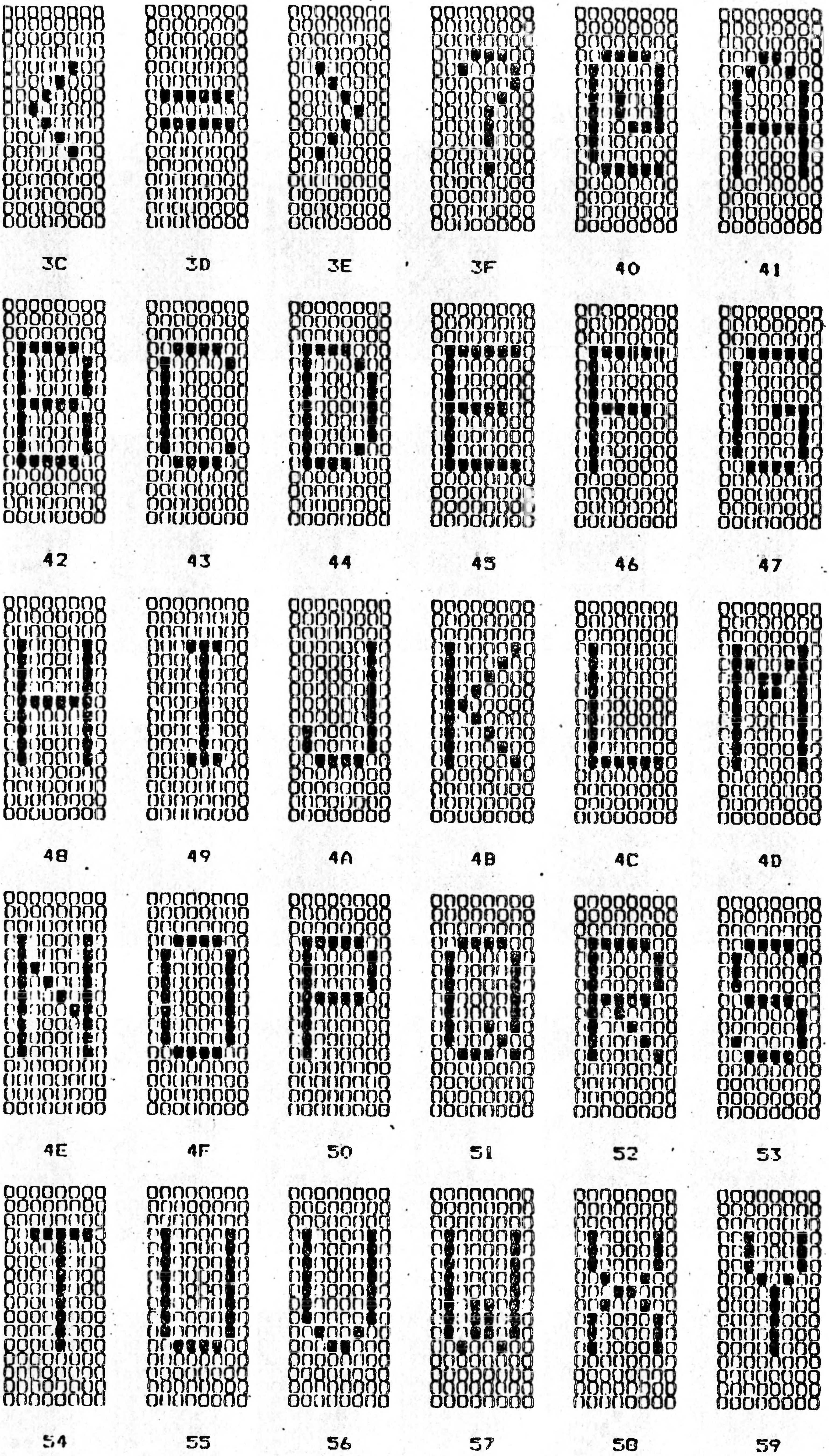


Figure 7.3 The main character set (3 of 9)

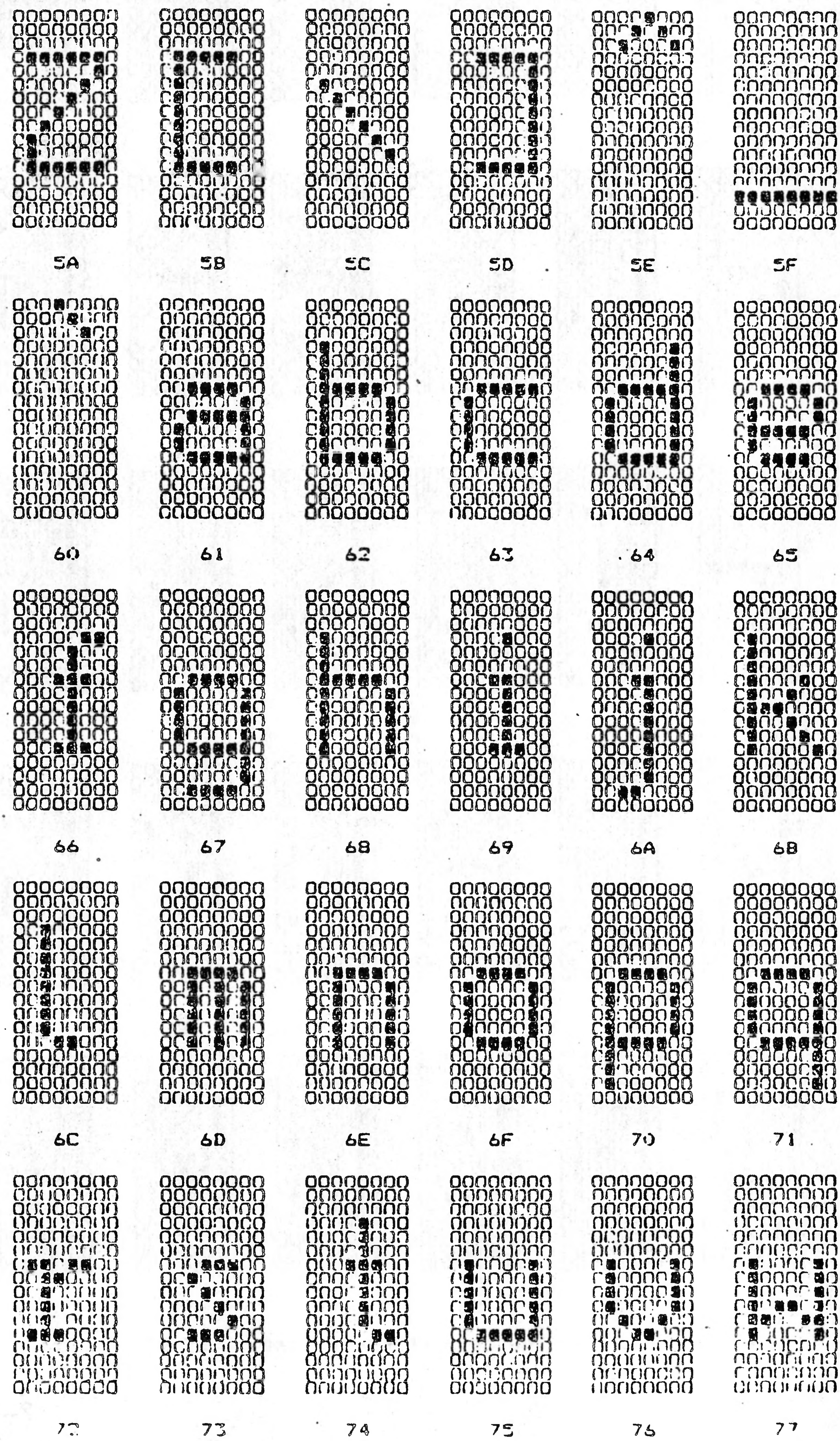


Figure 7.3 The main character set (4 of 9)

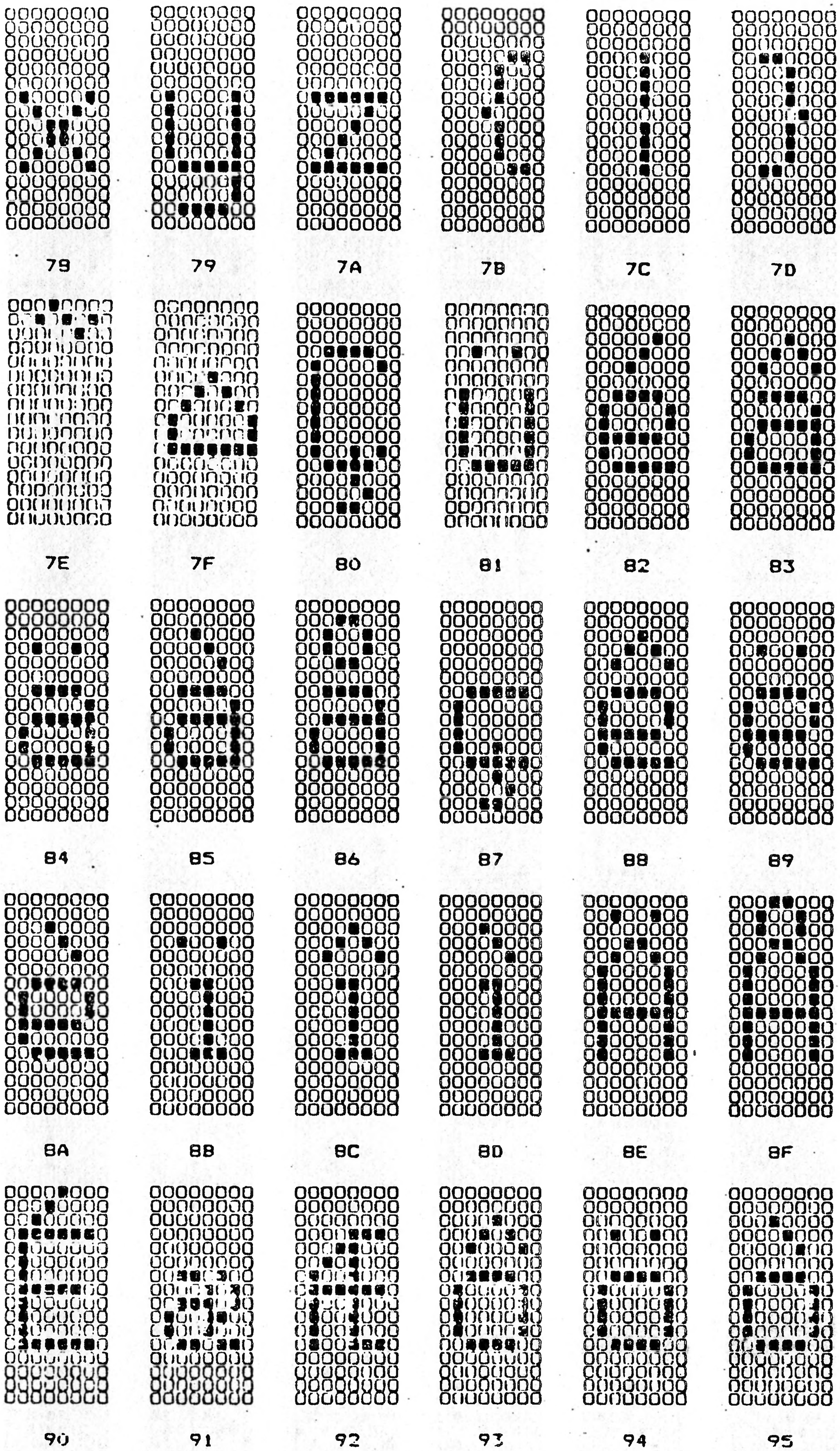


Figure 7.3 The main character set (5 of 9)

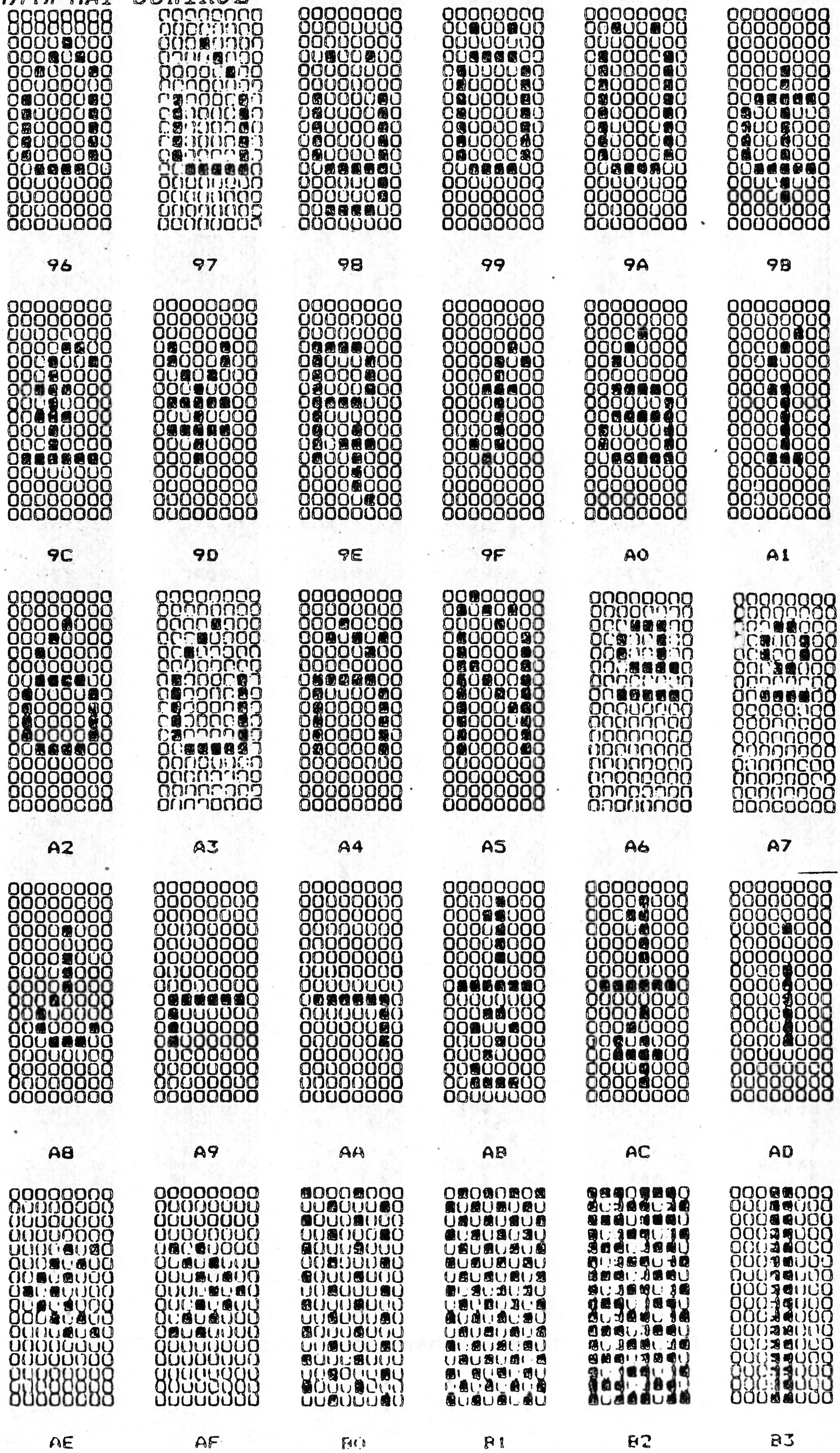


Figure 7.3 The main character set (6 of 9)

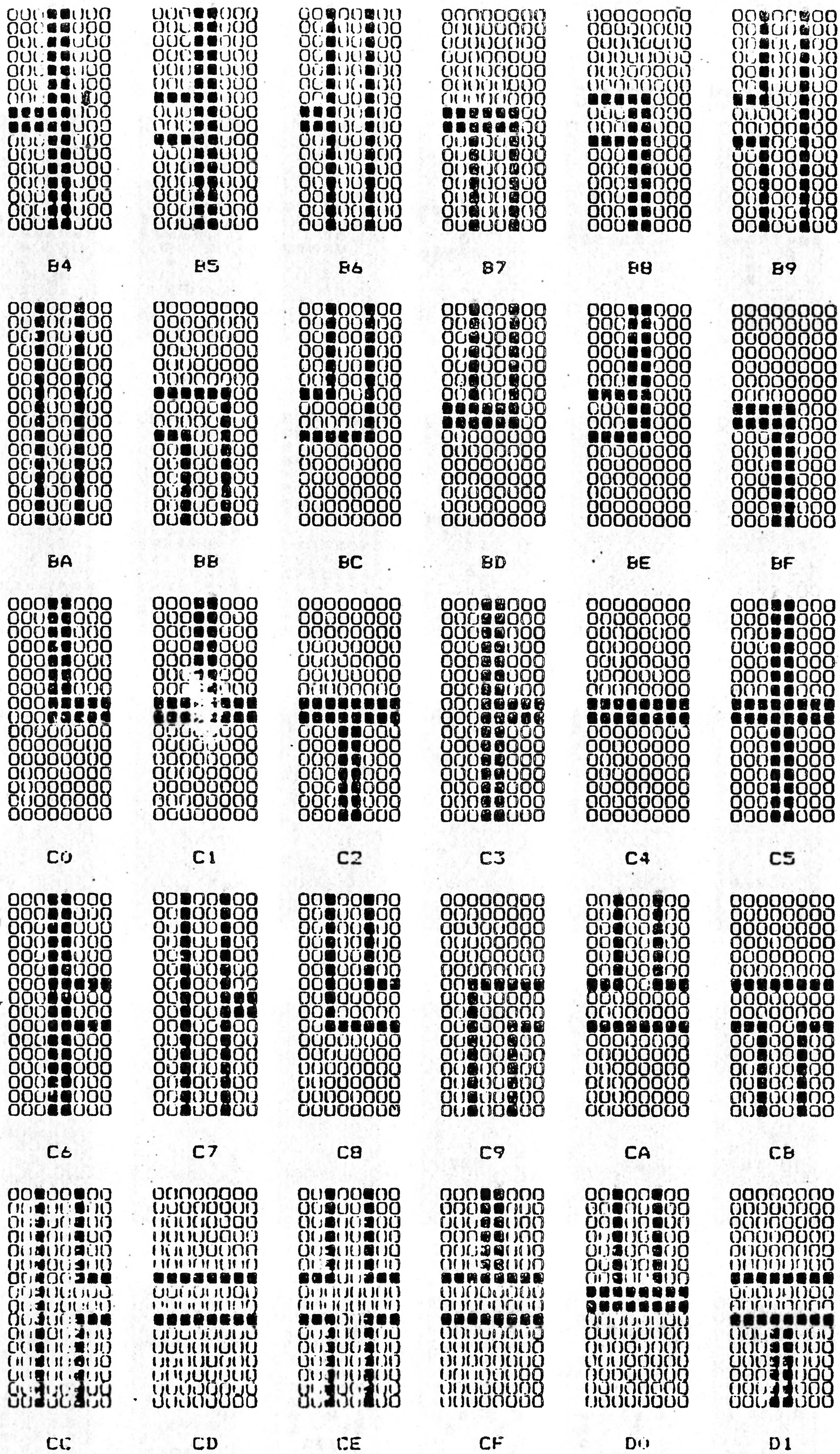


Figure 7.3 The main character set (7 of 9)

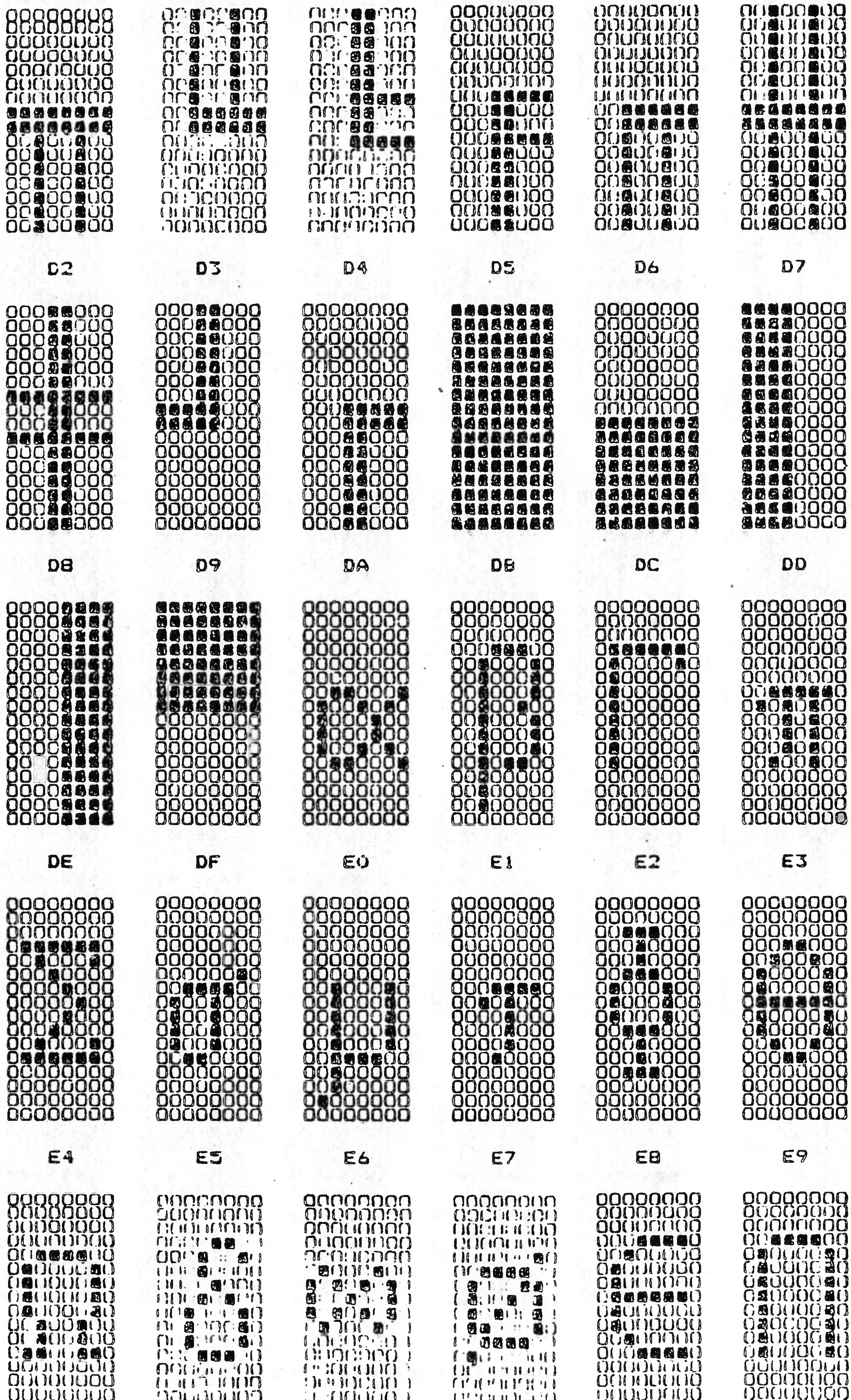


Figure 7.3 The main character set (8 of 9)

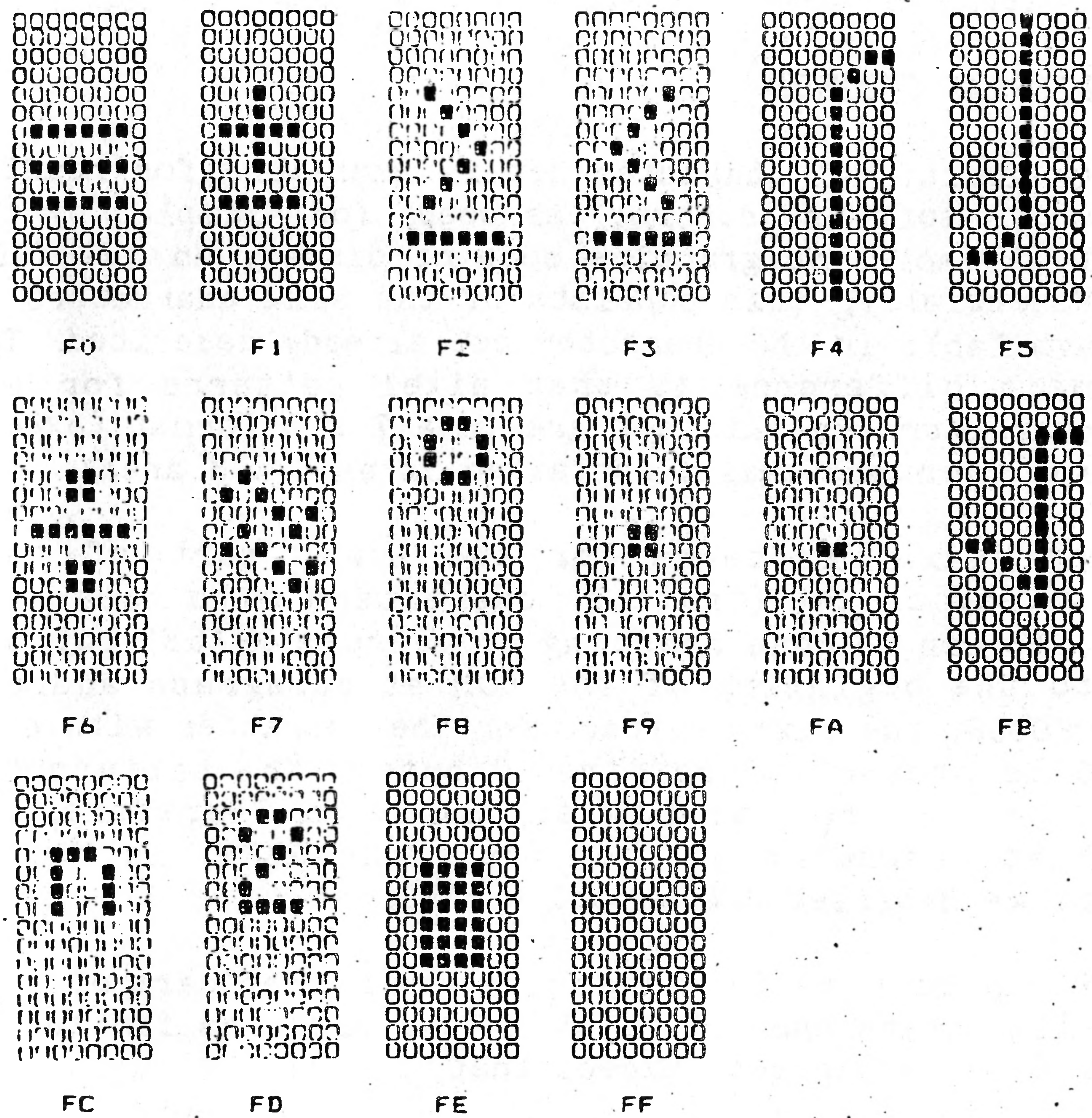


Figure 7.3 The main character set (9 of 9)

An additional character set is available for reading under software control, as used, for example, by the low resolution graphics mode of display in GW-BASIC. Essentially, this consists of the same characters as available in the character set already described. The main difference is that pixel patterns for the characters in this set are in a 7 x 7 format (except for downward tails) contained in an 8 x 8 area.

The pixel patterns for the lower part of this character set (that is, characters with codes 0 - 7FH) can be read starting at address 0FA6EH, offset to the beginning of the ROM at paragraph address 0F000H: the pixel pattern for the character with code 0 is stored in the first 8 bytes, the pattern for code 1 in the next 8 bytes, and so on. Therefore, the last character pattern (for code 07FH) is stored between offset 0FE66H and 0FE6DH.

The procedure for accessing the higher part of this alternative character set is the sames as for the 16 x 8 character set, except that

* You may specify either low/medium or high resolution in response to the GRAFTABL menu.

* The pixel pattern for any character occupies only 8 bytes of memory.

* The beginning of the character table is at a positive offset of 1 byte to the location pointed to by the interrupt vector.

This character set is not implemented in the hardware character generator.

Figure 7.4 illustrates the pixel patterns of the 8 x 8 character set.

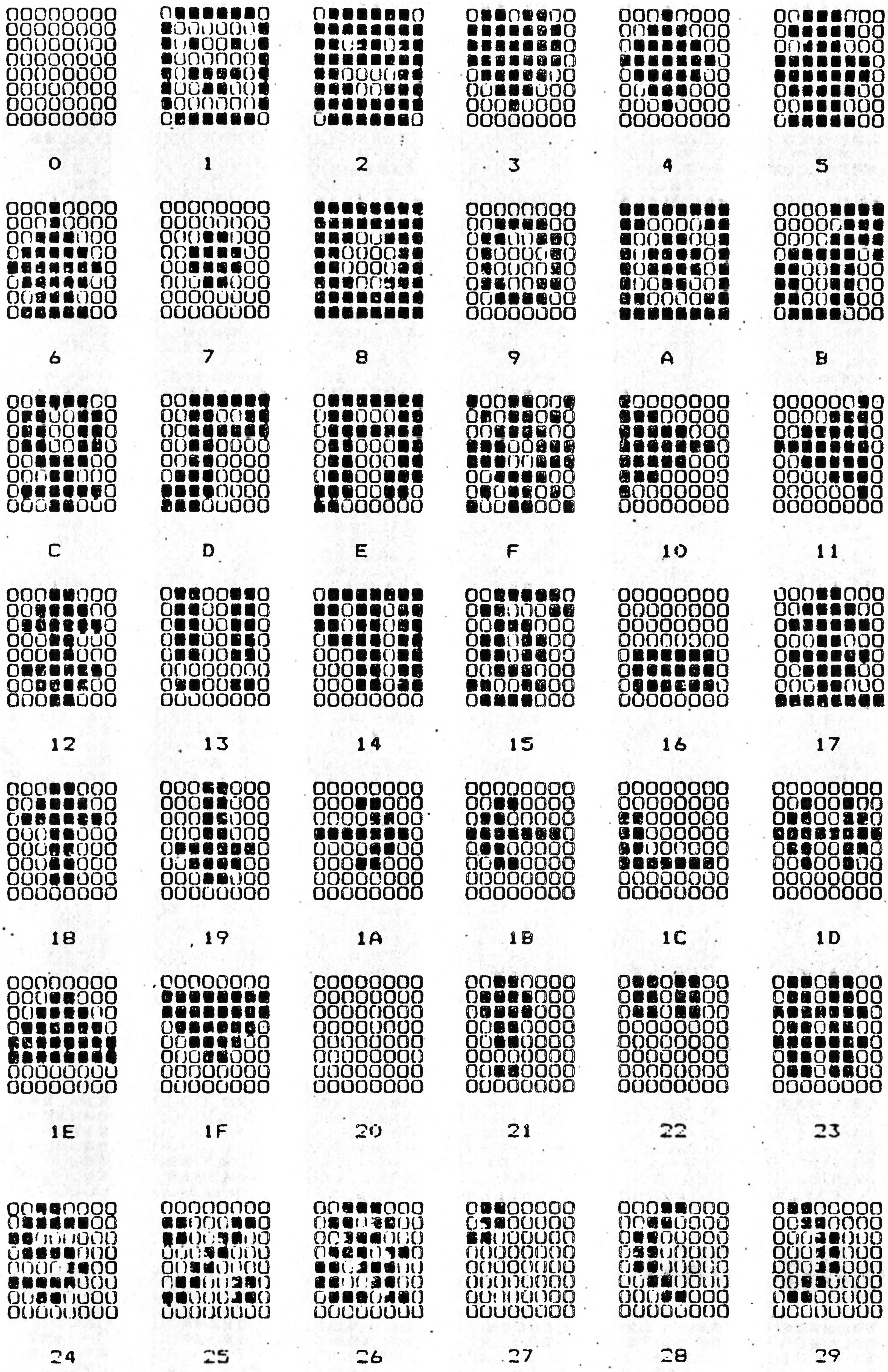


Figure 7.4 The alternative character set (1 of 7)

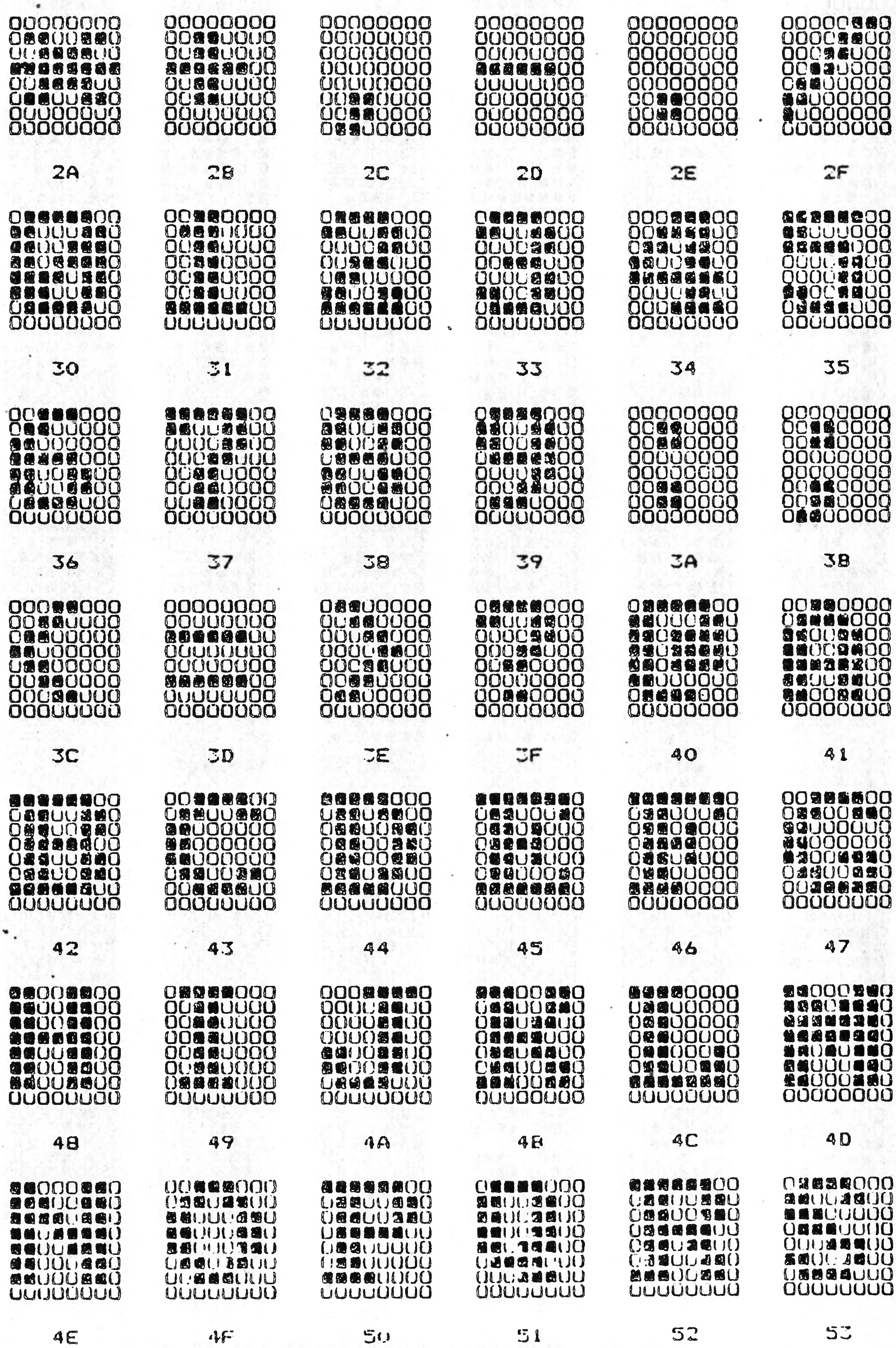


Figure 7.4 The alternative character set (2 of 7)

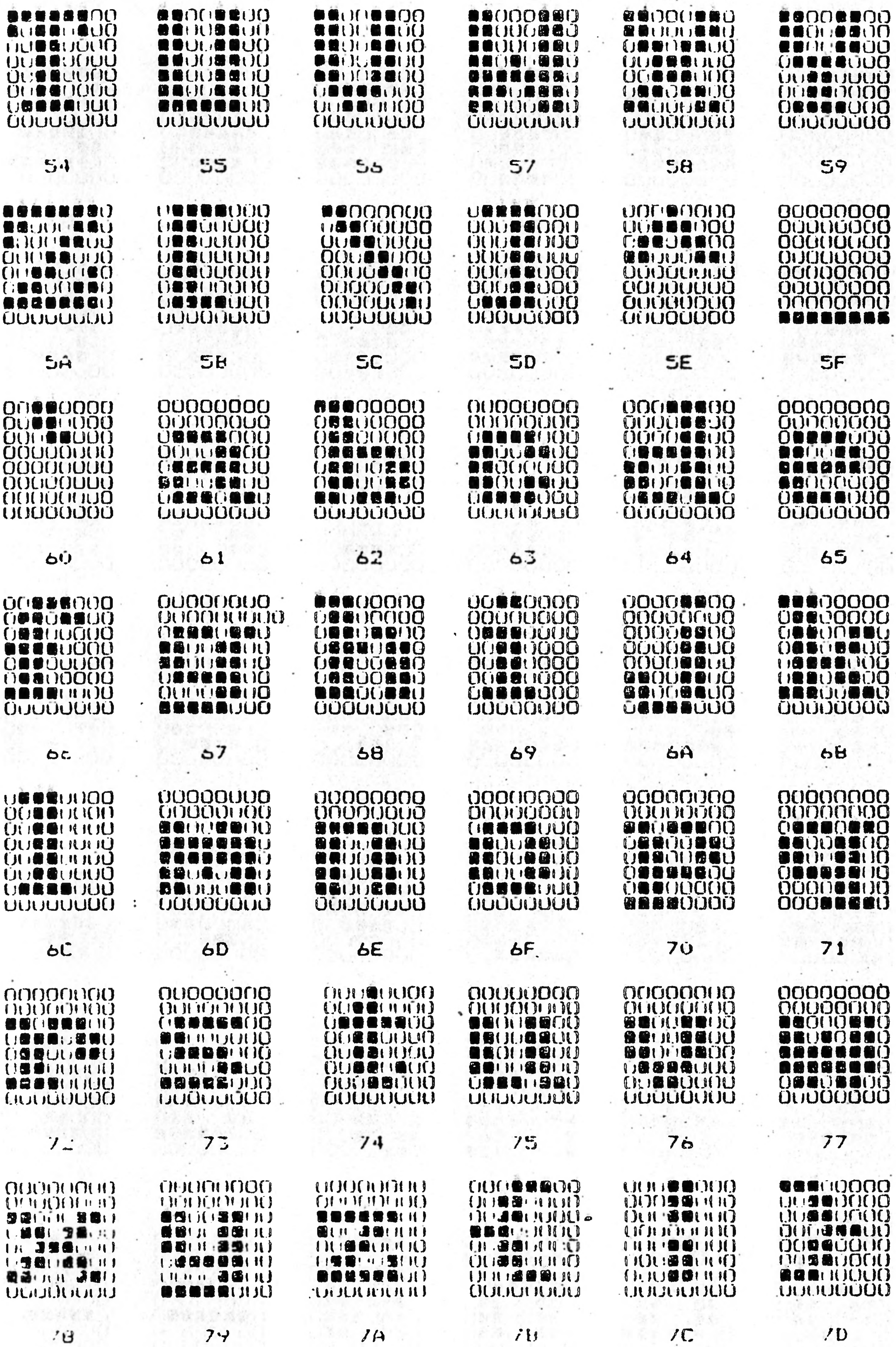


Figure 7.4 The alternative character set (3 of 7)

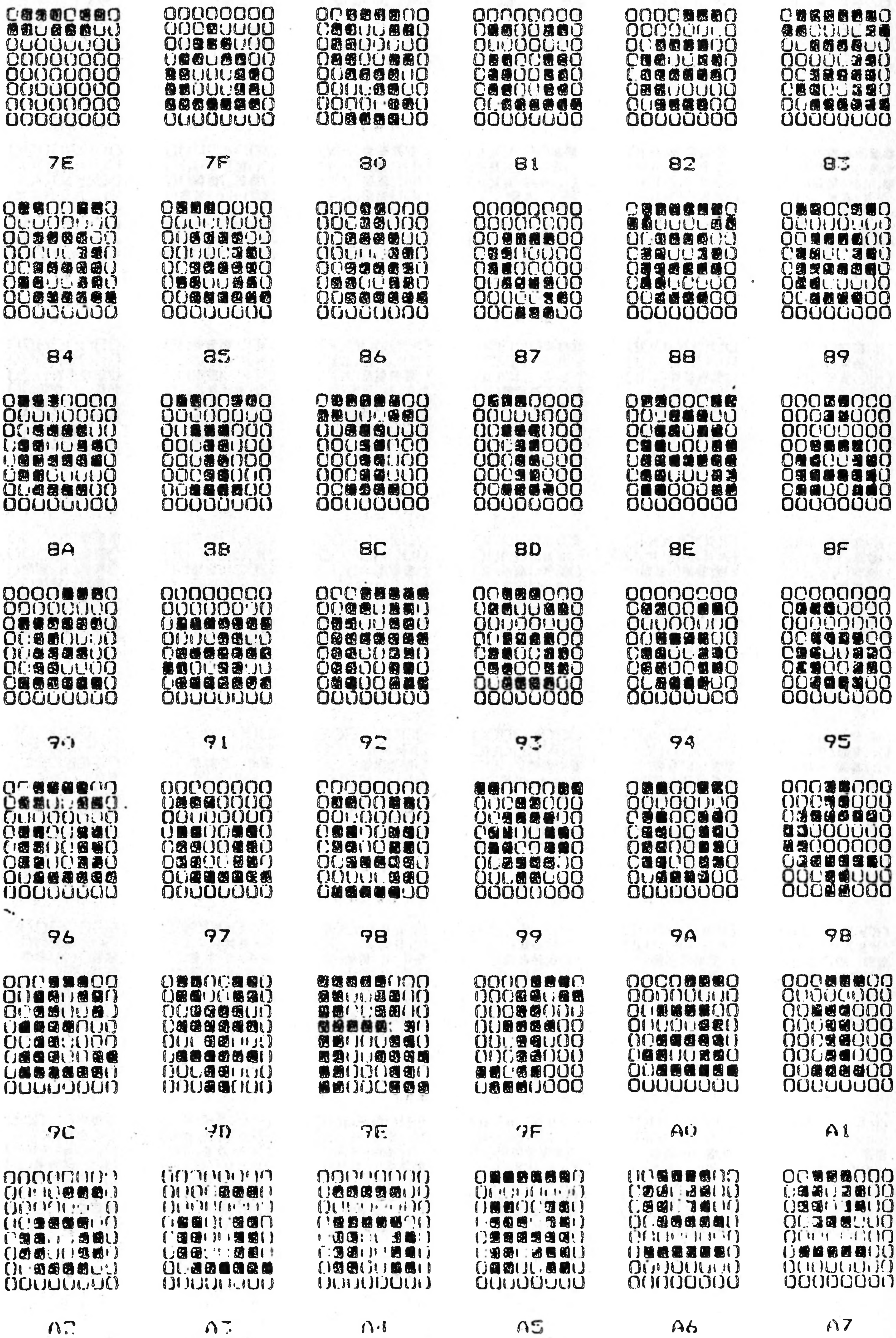


Figure 7.4 The alternative character set (4 of 7)

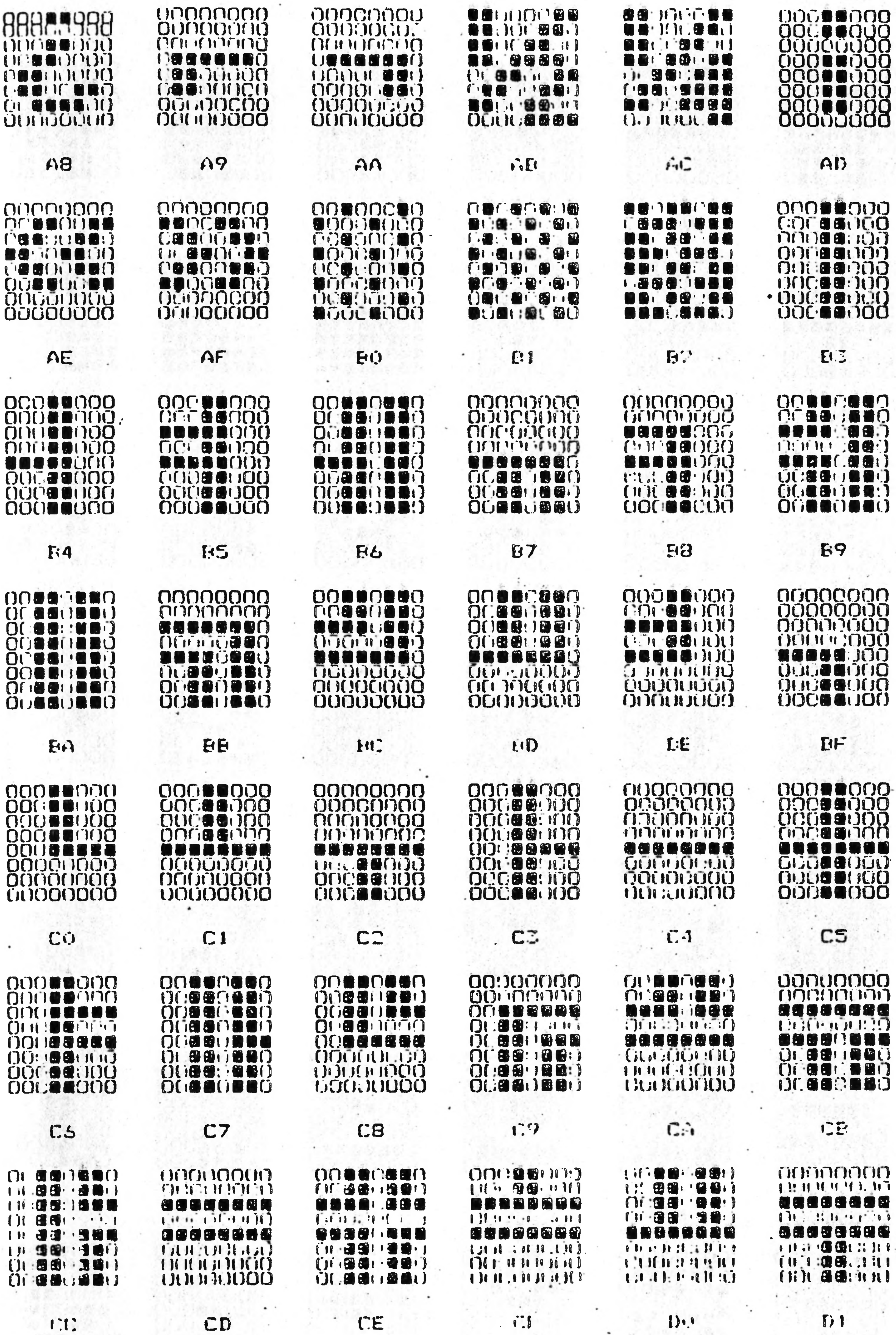


Figure 7.4 The alternative character set (5 of 7)

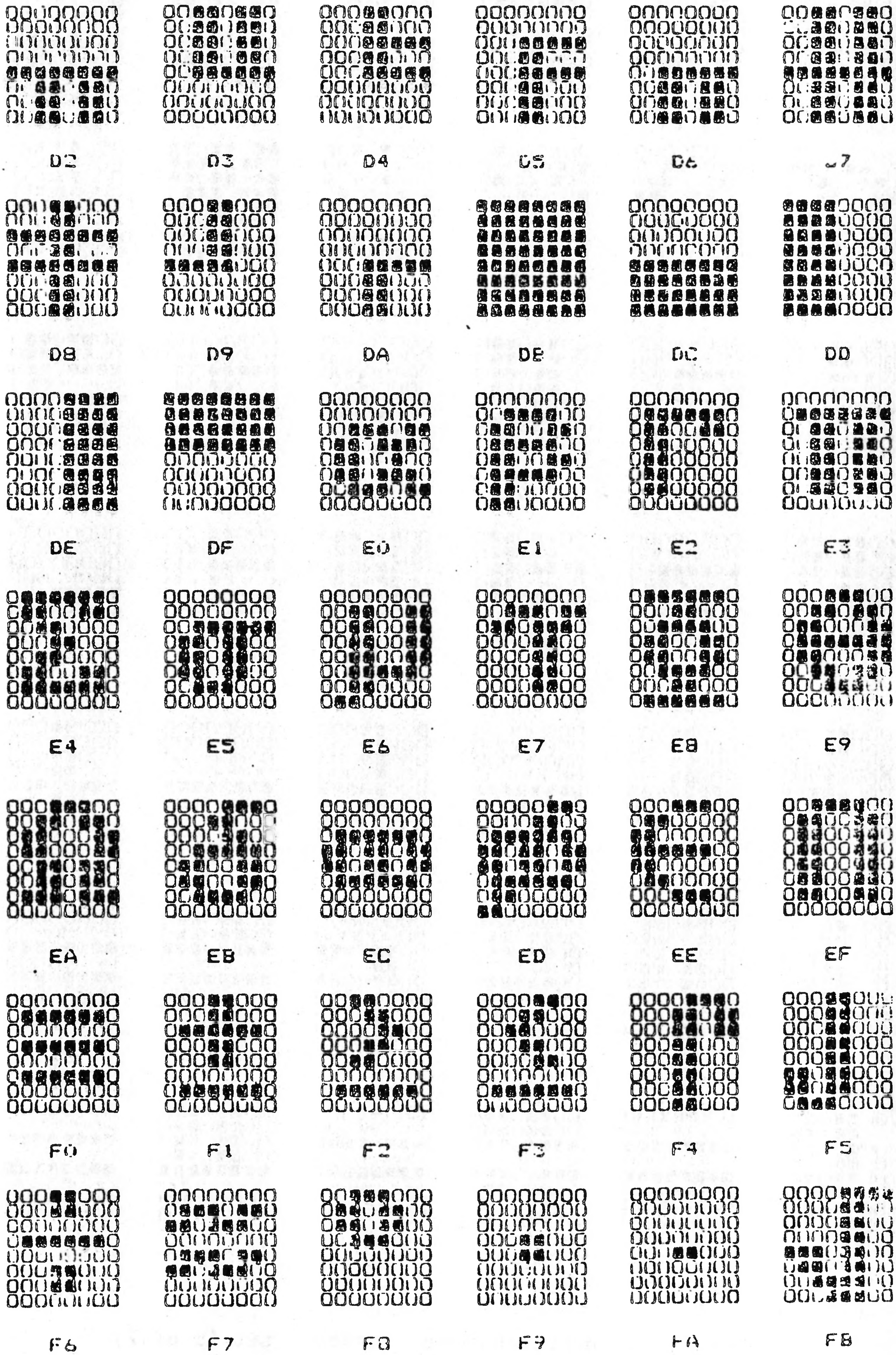


Figure 7.4 The alternative character set (6 of 7)

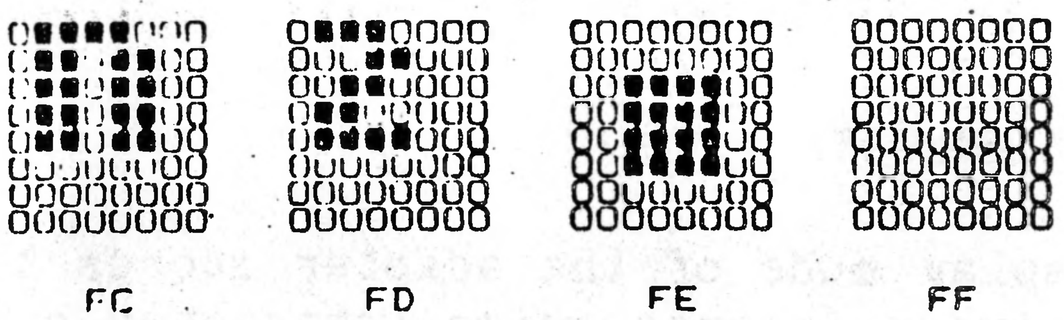


Figure 7.4 The alternative character set (7 of 7)

CHARACTER DISPLAY MEMORY

The character display mode of the adapter stores the character screen image in byte pairs (character code - attribute) in 4 KB of read/write memory, starting at CPU memory address 0B8000H. The even address of each pair stores the character code in the range 0 to 0FFH, the odd address immediately above it stores the attribute byte. The CPU/monitor access is synchronized with the character clock. Therefore, each CPU access to video memory is accompanied by at least one processor WAIT state. Alternatively, video memory can be accessed by DMA.

The significance of the attribute byte is set out in Figure 7.5.

Color	Background bits			Writing bits		
	6	5	4	2	1	0
Black	0	0	0	0	0	0
Red	1	0	0	1	0	0
Green	0	1	0	0	1	0
Blue	0	0	1	0	0	1
Cyan	0	1	1	0	1	1
Magenta	1	0	1	1	0	1
Brown	1	1	0	1	1	0
White	1	1	1	1	1	1

Figure 7.5 The character display attribute byte (color)

Notes:

Bits 7 and 3 set blinking and increased intensity, respectively. When blinking is disabled (see mode select register - port 3D8H), bit 7 controls background intensity.

The character display memory requires 4 KB. Additional memory can be used for further screen "pages" which can be selected by the 6845 controller.

CHARACTER DISPLAY CONTROL

Because video data can be written to and read from read/write memory with CPU MOVE instructions, programming the 6845 is required only in order to initialize the character display and for certain changes of the display mode. These programming steps are described in this section.

The following hexadecimal port addresses are dedicated to the 6845 controller:

3D4 - Controller Index Register (value output via this port points to one of eighteen 6845 internal registers)

3D5 - Data Register (value output to register selected via port 3D4)

3D8 - Mode Control (write only). The effects of the individual bits, when set, are as follows:

- 0 - select fast CRT-controller clock (necessary for 80 x 25 character mode and 640 x 400 graphics mode)
- 1 - select graphics mode; zero selects character mode
- 2 - activate video signals for monochrome display; otherwise, a color display is assumed
- 3 - enable video signal
- 4 - select monochrome graphics (640 x 200 or 640 x 400)
- 5 - enable blinking function
- 6 - select 400 lines display
- 7 - select page: zero = page 1 or 2, set = page 3 or 4

DISPLAY CONTROL

3D9 - Color Selection (write only). The effects of the individual bits, when set, are as follows:

0, 1, 2 - activate blue, green, and red guns, respectively for border color (character mode); in graphics modes, this color setting applies to the background color. The border color in character mode is a software convention; it is not actually displayed
3 - set high intensity for color selected by bits 0,1,2, provided these bits apply to character mode border or 320 x 200 graphics.
4 - set high intensity for background color in character display
5- palette selection in color graphics through activation and de-activation of the CRT blue gun
6,7 - not used

3DA - Status (read only). The significance of the individual bits, when set:

0- display enabled (controller not reading display memory at the moment)
1 - light pen trigger set
2 - light pen switch closed
3 - vertical retrace in progress

3DB Clear light pen latch

3DC - Preset light pen latch

Critical settings of the Mode Control Register (port 3D8H) for character display are given in Figure 7.6.

Bit 7	6	5	4	3	2	1	0	Character Display Mode
0	0	1	0	1	1	0	0	40 x 25 monochrome
0	0	1	0	1	0	0	0	40 x 25 color
0	0	1	0	1	1	0	1	80 x 25 monochrome
0	0	1	0	1	0	0	1	80 x 25 color

Figure 7.6 Character mode control on color/graphics adapter

The controller register selected via port 03D4H can be one of those given in Figure 7.7. These controller registers are write only, except:

0EH, 0FH - read/write 10H, 11H - read only

Registers 0CH and 0DH are of special interest: when set to zero, they address the first character of the 4 KB screen page starting at CPU address 0B8000H as the top left corner of the screen. Changing this value, you can displace characters on the physical screen without having to transfer them within screen memory.

Reg.	Function/Value via Port 3D5
0	Horizontal synchronization period: the number of displayed characters plus the number of non-display characters (retrace time) minus 1.
1	Number of displayed characters per line (must be less than number specified in register 0).
2	Horizontal Sync position: defines horizontal sync and scan delays. Increasing this value shifts the display to the left, decreasing this value shifts the display to the right.
3	Sync width: the value of the vertical sync pulse and the horizontal sync pulse width.
4	Elapsed time of the vertical scan: the integer number of physically displayable character lines, minus 1.
5	Elapsed time of vertical scan: lines not involved with display of video memory image (for vertical adjustment).
6	Number of displayed character row times (must be less than value in register 4).
7	Vertical Sync Position: increasing this value shifts the display up, decreasing this value shifts the display down.

Figure 7.7 The controller registers (1 of 2)

Reg.	Function/Value via Port 3B5
8	Interlace Mode and Skew: combined value in bits 0,1: 0 or 2 = non interlace 1 = interlace synch 3 = interlace synch and video 4,5: 0 = no skew 1 = 1 character skew 2 = 2 character skew 6,7: 0 = no cursor skew 1 = 1 character cursor skew 2 = 2 character cursor skew
9	Number of scan lines per character row, minus 1.
0AH	Cursor definition: combined value in bits 0-3 = start scan line of cursor in character block; combined value in bits 5 and 6: 0 = slow blinking 1 = no cursor display 3 = fast blinking
0BH	Cursor definition: combined value in bits 0-3 = last scan line of cursor in character block.
0CH 0DH	First address output by CRT controller. The initial value is 0, thus addressing the beginning of video memory. In the case of the character display, this represents the CPU address 0B8000H. The most significant bits of this address are in 0CH.
0EH 0FH	Cursor position in read/write memory (most significant bits in 0FH).
10H 11H	Light Pen address (most significant bits in 10H).

Figure 7.7 The control registers (2 of 2)

Control registers OAH-11H can be manipulated in accordance with the requirements of the individual application. The other registers are set as shown in Figure 7.8.

Register	Value - hex 40 x 25	Value - hex 80 x 25	Register	Value - hex 40 x 25	Value - hex 80 x 25
0	34	69	5	0	0
1	28	50	6	19	19
2	2C	58	7	19	19
3	5	0A	8	0	0
4	1A	1A	9	0F	0F

Figure 7.8 Control registers for color character display

THE CHARACTER CURSOR

The character display mode cursor of the NCR PERSONAL COMPUTER consists of up to 16 scan lines. In order to maintain compatibility with applications which assume a cursor of lower definition, a small PROM intercepts data to control registers OAH and OBH (via port 3B5H) before they reach the 6845 controller. The following conversions are performed:

* The value 2 is added to cursor start and end values between 8 and 13 inclusive. As a result, scan lines 8 and 9 are not accessible.

* Start and end values 14 and 15 are both interpreted as value 15.

Scan lines 0 to 7 are passed to the controller without intervening conversion. The scan line number specified for the cursor start must not be greater than that specified for the end scan line.

GRAPHICS DISPLAY

The graphics display adapter supports display of the set of 256 characters in an 80 (horizontal) x 25 format. In addition, all points addressable graphics can be implemented in three degrees of resolution.

GRAPHICS DISPLAY MEMORY

The graphic display adapter has as much as 64 KB of read/write memory at its disposal, according to the amount of memory on the display adapter.This memory resides in the CPU address areas 0B8000H - 0BFFFFH and 0A8000H - 0AFFFFH (lower 32 KB if video memory extension 3299-K202 installed). The use of these memory areas varies according to the display mode selected, and is therefore given for each mode separately. The video memory is dual ported, so that the CPU can access it at any time. To avoid display disturbances, however, applications should confine access to the horizontal and vertical retrace intervals.

GRAPHICS DISPLAY CONTROL

The general concept of video display initialization discussed in "Character Display Control" also applies to initializing the adapter for graphic display. The significant difference lies in the more extensive mode control and status information needed to account for the variety of modes available in graphics programming.

The graphics display controller supports a number of degrees of graphic resolution. The graphics display adapter and initialization firmware of your NCR PERSONAL COMPUTER allow three graphic display modes, namely low, medium, and high resolution. Low and medium resolution graphics make use of a 16 KB video memory for one screen design, high resolution requires 64 KB.

Note:

A number of non-NCR personal computers apply the term "low resolution" to a 160 x 100 pixel graphic display, as, for example, transmitted to home televisions by means of a composite VHF or UHF signal. The low resolution graphic mode of your NCR PERSONAL COMPUTER supports 320 x 200 pixel color graphics, medium resolution supports a 640 x 200 pixel monochrome graphic display. The NCR high resolution mode of display, not usually supported by other personal computers, gives a high quality 640 x 400 pixel color graphic display. This enhanced feature of the NCR PERSONAL COMPUTER does not adversely affect the compatibility stated in the foreword to this Manual.

Low Resolution

The low resolution graphic display consists of 320 horizontal by 200 vertical pixels. Each pixel is represented by two bits, so that a choice of four colors is available for each pixel. Each line is output twice (duplicated in the following odd scan), so that the physical screen is actually filled by 400 graphic lines.

Low resolution uses 16 KB of video memory as follows:

0B8000H - 0B9F3FH: even line scans (0,2,...198)
0B9F40H - 0B9FFFH: not used

0BA000H - 0BBF3FH: odd scan lines (1,3,...199)
0BBF40H - 0BBFFFH: not used

The first byte (0B8000H) contains color information for the 4 leftmost pixels of the top display line, and so on:

```
                     OB8000H
                       Bit
=========================================
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
=========================================
 \     /                  \     /
  \   /                    \   /
pixel 0,0                pixel 3,0
```

Of each bit pair, the more significant bit controls the red gun, the less significant bit controls the green gun. If neither of these bits is set, the pixel takes on the current background color of the Color Select Register (port 3D9H, bits 0-3). The blue gun is governed by the Color Select Register (port 3D9H, bit 5). Therefore, the CRT display uses one of two color palettes, according to whether the blue gun is on or not. By activating the monochrome bit in the Mode Control Register Port 3D8H, it is possible to create a third color palette. Color selection is set out in Figure 7.9.

The initial settings of 6845 registers (set via ports 3D4H and 3D5H) for the low resolution mode of graphic display on the internal color CRT are given in Figure 7.10. Registers 0AH-11H can be manipulated in accordance with specific programming requirements. When both set to zero, registers 0CH and 0DH set the graphics display controller to regard video memory address 0B8000H as the first byte of display information. You can change these two registers to address the upper 16 KB of the 32 KB graphic memory, thus enabling your programs to acccess a second graphic page.

Video Memory MSB	Video Memory LSB	Port 3D8H, bit 2	Port 3D9H, bit 5	Pixel Color
0	0	0	0 or 1	Current Background
0	1	0	0	Green
1	0	0	0	Red
1	1	0	0	Brown
0	1	0	1	Cyan
1	0	0	1	Magenta
1	1	0	1	White
0	0	1	0 or 1	Current Background
0	1	1	0 or 1	Cyan
1	0	1	0 or 1	Red
1	1	1	0 or 1	White

Figure 7.9 Low resolution graphics - color selection

Notes:

Background can be any one of 16 colors (8 basic colors, with intensity bit on or off).

Foreground color can be given high intensity (bit 4 of color select register, port 3D9H).

Register	Value - hex	Register	Value - hex
0	34	5	0
1	28	6	64
2	2C	7	64
3	5	8	0
4	6B	9	3

Figure 7.10 Control registers for low resolution graphics

If your display adapter contains a 64 KB video memory, you can use these two registers to switch between two graphic pages. With additional manipulation of the page switch bit in the Mode Control register (port 3D8H, bit 7) up to 4 graphic pages can be addressed.

The memory map for the full 64 KB video memory is as follows:

```
0B8000H - 0B9F3FH: even line scans   }
0B9F40H - 0B9FFFH: not used          }   page 1
0BA000H - 0BBF3FH: odd scan lines    }
0BBF40H - 0BBFFFH: not used          }

0BC000H - 0BDF3FH: even scan lines   }
0BDF40H - 0BDFFFH: not used          }   page 2
0BE000H - 0BFF3FH: odd scan lines    }
0BFF40H - 0BFFFFH: not used          }

0A8000H - 0A9F3FH: even line scans   }
0A9F40H - 0A9FFFH: not used          }   page 3
0AA000H - 0ABF3FH: odd scan lines    }
0ABF40H - 0ABFFFH: not used          }

0AC000H - 0ADF3FH: even scan lines   }
0ADF40H - 0ADFFFH: not used          }   page 4
0AE000H - 0AFF3FH: odd scan lines    }
0AFF40H - 0AFFFFH: not used          }
```

Critical settings for the Mode Control Register (port 3D8H) are to be found in Figure 7.11 (bit 5 is "don't care").

7	6	5	4	3	2	1	0	Low Resolution Graphics
0	0	-	0	1	0	1	0	Color
0	0	-	0	1	1	1	0	Monochrome

Figure 7.11 Graphics mode control - low resolution

Medium Resolution

The medium resolution graphic display consists of 640 horizontal by 200 vertical pixels. Each pixel is represented by a single bit, so that each pixel can be displayed as on or off in 16 KB of video memory. The video memory addresses used are the same as those for low resolution graphics. The only difference is that each byte contains display information (monochrome on or off) for 8 pixels:

```
                        0B8000H
                          Bit
==========================================================
|  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
==========================================================
   |                                         |
   |                                         |
pixel 0,0                               pixel 7,0
```

The 6845 registers (port 3D4H/3D5H) are set as for medium resolution graphics.

The Mode Control Register (port 3D8H) is set as shown in Figure 7.12 (bit 5 is "don't care".

Bit								Medium Resolution Graphics
7	6	5	4	3	2	1	0	
0	0	-	1	1	1	1	0	Monochrome (640 x 200) pages 1 and 2
1	0	-	1	1	1	1	0	Monochrome (640 x 200) pages 3 and 4

Figure 7.12 Graphics mode control - medium resolution

High Resolution

The high resolution mode of the graphic display enables you to use the internal color CRT to its full advantage. This mode makes use of the maximum of 64 KB video memory which can be installed on the graphics display adapter. In the case of color graphics, this memory is used as follows:

OB8000H - OBBF3FH: even scans (0,4,8,...396)
OBBF40H - OBBFFFH: not used
OBC000H - OBFF3FH: odd scans (1,5,9,...397)
OBFF40H - OBFFFFH: not used
OA8000H - OABF3FH: even scans (2,6,10,...398)
OABF40H - OABFFFH: not used
OAC000H - OAFFFFH: odd scans (3,7,11,...399)
OAFF40H - OAFFFFH: not used

As in low resolution graphics, each pixel is represented by two bits. Bits 7 and 6 of byte OB8000H determine the color of the pixel in the top left corner of the screen: either current background color as specified by the Color Select Register, or one of three colors in the current palette selected by the Color Select Register.

The same resolution (640 x 400) can be confined to monochrome (pixel on or off) graphics. As in medium resolution graphics, each pixel is represented by one bit, starting with bit 7 at OB8000H (top left pixel). An alternate screen image can be stored at OA8000H.

The video memory map for the screen image starting at 0B8000H (the equivalent is also available at 0A8000H):

```
0B8000H - 0B9F3FH: even scans (0,4,8,...396) }
0B9F40H - 0B9FFFH: not used                  }
0BA000H - 0BBF3FH: odd scans  (2,6,10,...398)}
0BBF40H - 0BBFFFH: not used                  }image 1
0BC000H - 0BDF3FH: even scans (1,5,9,...397) }
0BDF40H - 0BDFFFH: not used                  }
0BE000H - 0BFF3FH: odd scans  (3,7,11,...399)}
0BFF40H - 0BFFFFH: not used                  }
```

The 6845 registers (port 3D4H/3D5H) are set for high resolution graphics as shown in Figure 7.13.

Register	Value - hex	Register	Value - hex
0	69	5	0
1	50	6	64
2	58	7	64
3	0A	8	0
4	6B	9	3

Figure 7.13 Control registers for high resolution graphics

Figure 7.14 illustrates Mode Control Register settings (port 3D8H) for high resolution graphics.

Bit 7	6	5	4	3	2	1	0	High Resolution Graphics
-	1	-	1	1	1	1	0	Monochrome
-	1	-	0	1	0	1	1	Color

Figure 7.14 Graphics mode control - high resolution

THE GRAPHICS CURSOR

The graphic cursor of the NCR PERSONAL COMPUTER, like the character display mode cursor, consists of up to 16 scan lines. In order to maintain compatibility with applications which assume a cursor of lower definition, a small PROM intercepts data to control registers 0AH and 0BH (via port 3D5H) before they reach the 6845 controller. The following conversion is performed:

* A scan line specified in the range 0 to 7 affects two scan lines: 0 is interpreted as 0 and 1, 1 is interpreted as 2 and 3, ... 7 is interpreted as 14 and 15.

Scan lines 8 to 15 are passed to the controller without intervening conversion. The scan line number specified for the cursor start must not be greater than that specified for the end scan line.

CONTROLLER DATA CONVERSION

In addition to the conversion applied to the character and graphics cursor, display controller conversion is applied to most of the other registers of the 6845 written via ports 3B4H/3B5H. The purpose of this conversion is to ensure that display control parameters written by some applications are received in a way that will produce the display intended, even though the particular application may have been designed for a non-NCR monitor. Non-conforming parameters are, therefore, converted to the respective values given in this Chapter.

The controller registers affected (in addition to the cursor definition registers already discussed), are the registers 0 to 9, selected via port 3B4H and written via port 3B5H. These registers convey parameters setting up display synchronization and skew/interlace modes. These parameters are supplied by the ROM BIOS, and need not normally be disturbed.

Printers and Communications

INTRODUCTION

This Chapter describes two standard types of interface which can be installed in your NCR PERSONAL COMPUTER, namely RS-232-C (serial) and Centronics (parallel). These interfaces are provided by the following Kits:

3299-K306 1 serial + 1 parallel interface
3299-K307 2 serial interfaces

A number of printers, plotters and communications devices can be controlled by your computer by means of these interfaces. The RS-232-C serial input/output interface is especially versatile in communications applications. This Chapter provides information about the hardware integration of these interfaces as well as instructions for their low level software control.

RS-232-C INPUT/OUTPUT

Connection to the external device is by means of a 9-pin D-shaped connector. The pin configuration of this connector is shown in Figure 8.1.

The RS-232-C interface is programmable by means of an 16450 asynchronous receiver/transmitter. This integrated circuit includes a programmable baud rate generator using a 1.8432 MHz crystal, and interrupt handling logic. The logic structure ad pin assigments of this integrated circuit are illustrated in Figure 8.2.

The control, address, and data signals are described in Figure 8.3.

Pin	Signal
1	Carrier Detect (CD)/
2	Receive Data (RxD)
3	Transmit Data (TxD)
4	Data Terminal Ready (DTR)/
5	Signal Ground
6	Data Set Ready (DSR)/
7	Request to Send (RTS)/
8	Clear to Send (CTS)/
9	Ring Indicator (RI)/

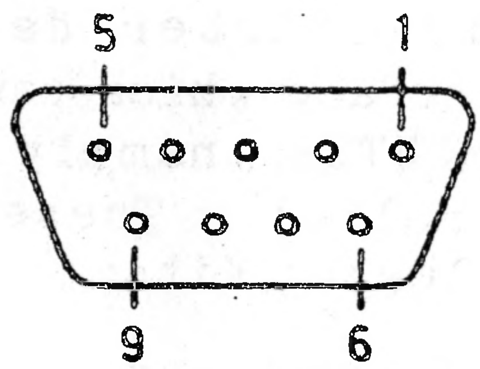


Figure 8.1 RS-232-C pin configuration

2 — 2
3 — 3

DTR → DSR
RTS → CTS
DSR ← RTS

DCD ← DTR
CTS ← RTS

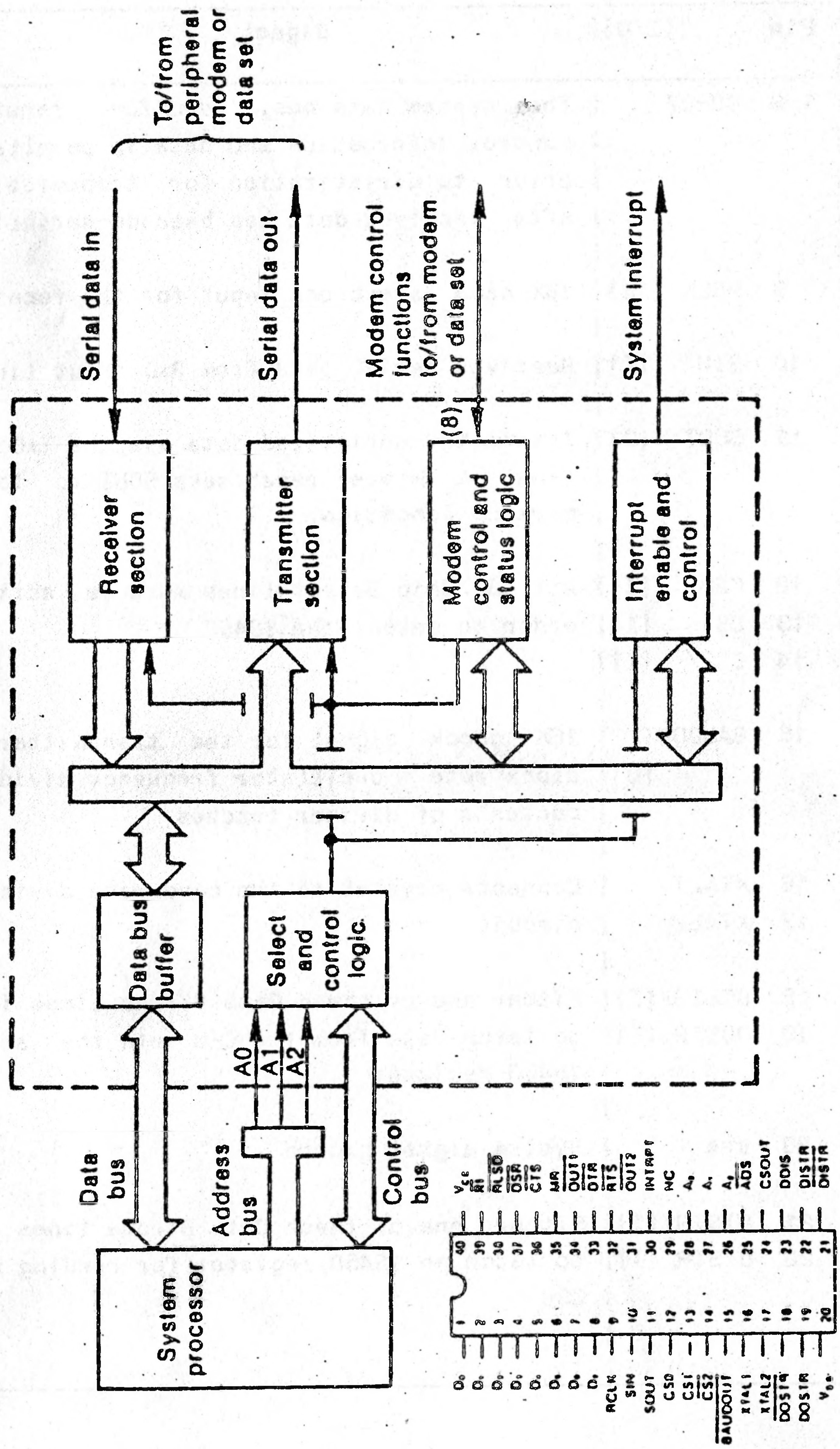


Figure 8.2 Serial/receiver transmitter

Pin		[I/O]	Signal
1-8	D0-D7		The system data bus, used for transferring control information and data in parallel form prior to serialization for transmission or after received data has been de-serialized
9	RCLK	[I]	16X baud rate clock input for the receiver
10	SIN	[I]	Receives serial data from RxD input line
11	SOUT	[O]	Transmits serialized data via the TxD output line. A Master reset sets SOUT to logic 1 marking condition
12	CS0	[I]	All 3 Chip Select lines must be active in order to select the 16450
13	CS1	[I]	
14	CS2/	[I]	
15	BAUDOUT/	[O]	16X clock signal for the transmitter. The clock rate = oscillator frequency divided by contents of divisor latches
16	XTAL1		Connects crystal to the baud rate divider circuit
17	XTAL2		
18	DOSTR/	[I]	Either one of these Data Strobe lines is used to latch data from the CPU into the selected 16450 register
19	DOSTR	[I]	
20	Vss		System signal ground
21	DISTR/	[I]	Either one of these Data Strobe lines serves to latch an 16450 register for reading by the CPU
22	DISTR	[I]	

Figure 8.3 16450 signals (1 of 3)

Pin		[I/O]	Signal
23	DDIS	[O]	Driver Disable. Output goes low whenever data is being read from the 16450. Can be used to reverse data direction of external receiver
24	CSOUT	[O]	Confirms chip selection by means of a high output. A pre-requisite for data trasfer.
25	ADS/	[I]	Address Strobe providing latching for 16450 internal registers. An active ADS/ signal is required only if the 3 address lines selecting the register do not maintain stable signals during throughout an 16450 operation.
26	A2		System address bus lines selecting an 16450 internal register
27	A1		
28	A0		
29			No connection
30	INTRPT	[O]	Output goes high whenever an enabled interrupt is imminent
31	OUT2/	[O]	User-designated output programmable by means of bit 3 of the Modem Control Register: bit set makes signal active
32	RTS/	[O]	Signal active informs the external device that the 16450 is ready to transmit data
33	DTR/	[O]	Signal active informs the external device that the 16450 is ready to communicate
34	OUT1/	[O]	User-designated output programmable by means of bit 2 of the Modem Control Register: bit set makes signal active

Figure 8.3 16450 signals (2 of 3)

Pin		[I/O]	Signal
35	MR	[I]	Signal active resets the 16450 internal registers
36	CTS/	[I]	Input signal to the 16450 from the external device, indicating that the latter is ready to transmit
37	DSR/	[I]	Input signal from the external device indicating its ready status
38	RSLD/	[I]	Received Line Signal Detect or Carrier Detect. Input signal from the external device confirming that adequate signal conditions are present
39	RI/	[I]	Input signal confirming that a ringing signal is being received by the external device
40	Vcc		+5 Vdc supply

Figure 8.3 16450 signals (3 of 3)

PROGRAMMING THE SERIAL RECEIVER/TRANSMITTER

The16450 converts parallel data to serial on the transmit side and serial to parallel on the receive side. The serial interface driven by the 16450 can be assigned to any one of four (3299-K307) or two (3299-K306) areas in the I/O map. The base port addresses selectable for serial I/O are:

```
               278H  }
3299-K306 {    2F8H  }  3299-K307
               378H  }
3299-K306 {    3F8H  }
```

These addresses are switch-selectable on the PCBs.

The programming instructions in this description refer to base port seletion 3F8H, but the four least significant address lines apply equally to the other three I/O areas.

The port addresses dedicated to this interface and the 16450 internal 8-bit registers:

3F8H	Receiver Buffer/Transmit Holding Register. This port is also used to access the lower byte of the baud rate Divisor Latch (switched by means of the Line Control Register).
3F9H	Interrupt Enable. Also upper byte of baud rate Divisor Latch (switched by means of Line Control Register).
3FAH	Interrupt Identification (read only).
3FBH	Line Control.
3FCH	Modem Control.
3FDH	Line Status.
3FEH	Modem Status.
3FFH	Not used.

Figure 8.4 shows the structure of the registers which control the operation of the 16450. The Receiver Buffer/Transmitter Holding Register is no more than an 8-bit data register accessed via the processor IN or OUT instruction, according to the direction of data flow. Bit 0 is always the first bit transmitted or received. The Divisor Latch sets the baud rate generator by means of a 16-bit binary value. The Divisor Latch is selected/de-selected by bit 7 in the Line Control Register.

Interrupt Enable Register (port 3F9H)							
Bits:							
7	6	5	4	3	2	1	0
0	0	0	0	Modem	Receive	Transmit	Data

Interrupt ID Register (port 3FAH)							
Bits:							
7	6	5	4	3	2	1	0
0	0	0	0	0	< Interr.	ID >	Pending

Line Control Register (port 3FBH)							
Bits:							
7	6	5	4	3	2	1	0
Divisor Latch	Set Break	Stick Parity	Even Parity	Parity Enable	Stop Bits	< Char.	Length>

Figure 8.4 16450 Control/Status Registers (1 of 2)

Modem Control Register (port 3FCH)							
Bit:							
7	6	5	4	3	2	1	0
0	0	0	Loop	Out 2	Out 1	RTS	DTR

Line Status Register (port 3FDH)							
Bit:							
7	6	5	4	3	2	1	0
0	TSRE	THRE	Break Interr.	Framing	Parity	Overrun	Data Ready

Modem Status Register (port 3FEH)							
Bit:							
7	6	5	4	3	2	1	0
RLSD	RI	DSR	CTS	DRLSD	TERI	DDSR	DCTS

Figure 8.4 16450 Control/Status Registers (2 of 2)

Interrupt Enable Register

If all bits are zero, no interrupts are issued by the 16450. Setting individual bits 0-3 determines which events result in the issue of an interrupt. These bits may be set in any combination:

0: Interrupt when received data available.
1: Transmitter Holding Reg. empty.
2: error or Break Interrupt.
3: change of state on CTS, DSR, RI, or RLSD.

Interrupt ID Register

If an interrupt is waiting to be acknowledged, bit 0 is zero. The binary value represented by bits 1 and 2 then denotes the pending interrupt with the highest priority (see Figure 8.5).

Priority/ ID value	Int. Type	Int. Source	Acknowledge/reset:
Highest/3	Receiver	Overrun error or Parity error or Framing error or Break Interrupt	Read Line Status
Second /2	Data	Receiver data available	Read Receive Buffer Register
Third /1	Transmit	Transmit Holding Register empty	This register read/ next write to THR
Lowest /0	Modem	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Read Modem Register

Figure 8.5 16450 Interrupt priority

Line Control Register

This register can be read as well as written, so that there is no need for applications to store the current settings.

Bits 0 and 1 contain a binary value specifying length of the serial character: 0 = 5 bits, 1 = 6 bits, 2 = 7 bits, and 3 = 8 bits.
Bit 2 specifies the number of stop bits: 0 = 1 stop bit; 1 sets 1.5 stop bits (for 5-bit character), or 2 stop bits (for other character lengths).
Bit 3 set determines that parity checking takes place. The type of parity checking is controlled by bits 4 and 5: bit 4 set means that an even number of bits are transmitted or checked; if bit 5 is set, parity is transmitted and then detected by the receiver as logic 0 (if bit 4 = 1) or as logic 1 (if bit 4 = 0).
Bit 6 forces the serial output line to a low (Break) state, where it remains until this bit is reset. The Break condition is often used to alert the external device.
Bit 7 set selects the Divisor Latch at ports 3F8H and 3F9H, in order to program the baud rate generator. As long as this bit is zero, the Receive Buffer/Transmit Holding Register (3F8H) and Interrupt Enable Register (3F9H) are selected.

Modem Control Register

Bits 0-3 set force high the 16450 output lines DTR/, RTS/, OUT1/, and OUT2/, respectively.
Bit 4 set activates 16450 internal diagnostics (see later section).

Line Status Register

Bit 0 set indicates that a serial character from the receiver has been converted to parallel form and is waiting to be read from the Receiver Buffer Register (port 3F8H). This status bit is automatically reset when the data byte is read, or if that register is filled with zeros by means of an OUT instruction from the microprocessor.
Bit 1 set means that an overrun error occurred, that is, the Receiver Buffer Register was not read before a new character was introduced to it. Reading the Line Status Register resets this bit.

Bit 2 set indicates a parity error. This bit is reset by reading the Line Status Register.
Bit 3 set indicates a framing error, that is, the stop bit is not valid.
Bit 4, the Break Interrupt detector, is set if a break condition is recognized by the receiver. Such a condition exists when the serial input line is at zero beyond the length of one character consisting of Start + Data + Parity + Stop bits.
Bit 5 indicates when the Transmit Holding Register can accept a new character for serialization and transmission (bit set), as the most recent character has been forwarded to the 16450's Transmit Shift Register. This bit is reset when this register is next written to.
Bit 6 reflects the status of the Transmit Shift Register: this bit set indicates that the register is idle.

Modem Status Register

Whenever bit 0, 1, 2, or 3 is set, a Modem Status interrupt condition is asserted (see Figure 8.5).

Bits 0 set indicates that the CTS/ line has changed state since the Modem Status Register was last read.
Bit 1 applies analogously to the DSR/ line.
Bit 2 is set when the trailing edge of the Ring Indicator is detected.
Bit 3 set indicates that the RLSD/ input has changed state.
Bits 4-7 represent the complements of the CTS/, DSR/, RI/, and RLSD/ inputs, respectively, provided that bit 4 in the Modem Control Register is zero. If this bit is set, the four Modem Status Register bits represent RTS/, DTR/, OUT1/ and OUT2/.

INTERNAL DIAGNOSTICS

The16450 includes its own loopback diagnostic feature, activated by writing the Modem Control Register with bit 4 set.

Data Integrity

The serial transmitter output (SOUT)is set to a state of marking (logic 1) and the serial receiver line (SIN) is disregarded. The output from the Transmit Shift Register is looped back into the Receiver Shift Register. The Modem control inputs CTS/, DSR/, RLSD/, and RI/ are disregarded. Instead, these signals are supplied internally by the Modem control outputs DTR/, RTS/, OUT1/, and OUT2/. This configuration allows the 16450 to verify its internal transmit and receive data paths.

The Interrupt System

In the diagnostic mode, receiver and transmitter interrupts are fully operational. The Modem Control interrupts are also operational, but the interrupts are now derived from the four least significant bits of the Modem Status Register, not from the Modem Control input lines. The interrupts can still be enabled and disabled by means of the Interrupt Enable Register.

A test of the interrupt system requires writing the lower 6 bits of the Line Status Register and the lower 4 bits of the Modem Status Register: a bit set results in the assertion of the corresponding interrupt.

To conclude diagnostics, restore the 16450 registers where appropriate and write the Modem Control Register with bit 4 set.

RECEIVER/TRANSMITTER TIMING

Figures 8.6 - 8.11 illustrate 16450 signal timing.

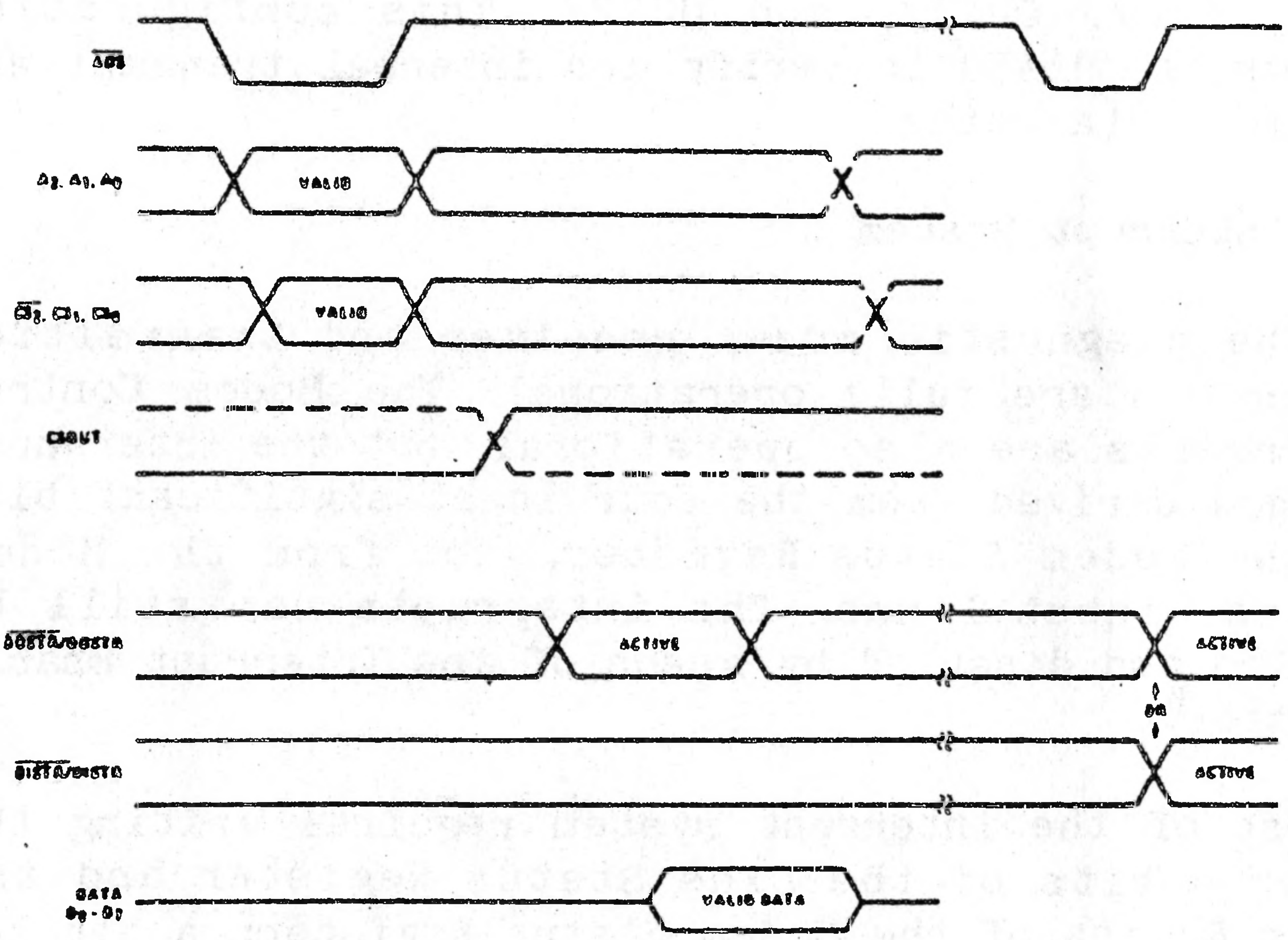


Figure 8.6 Read cycle

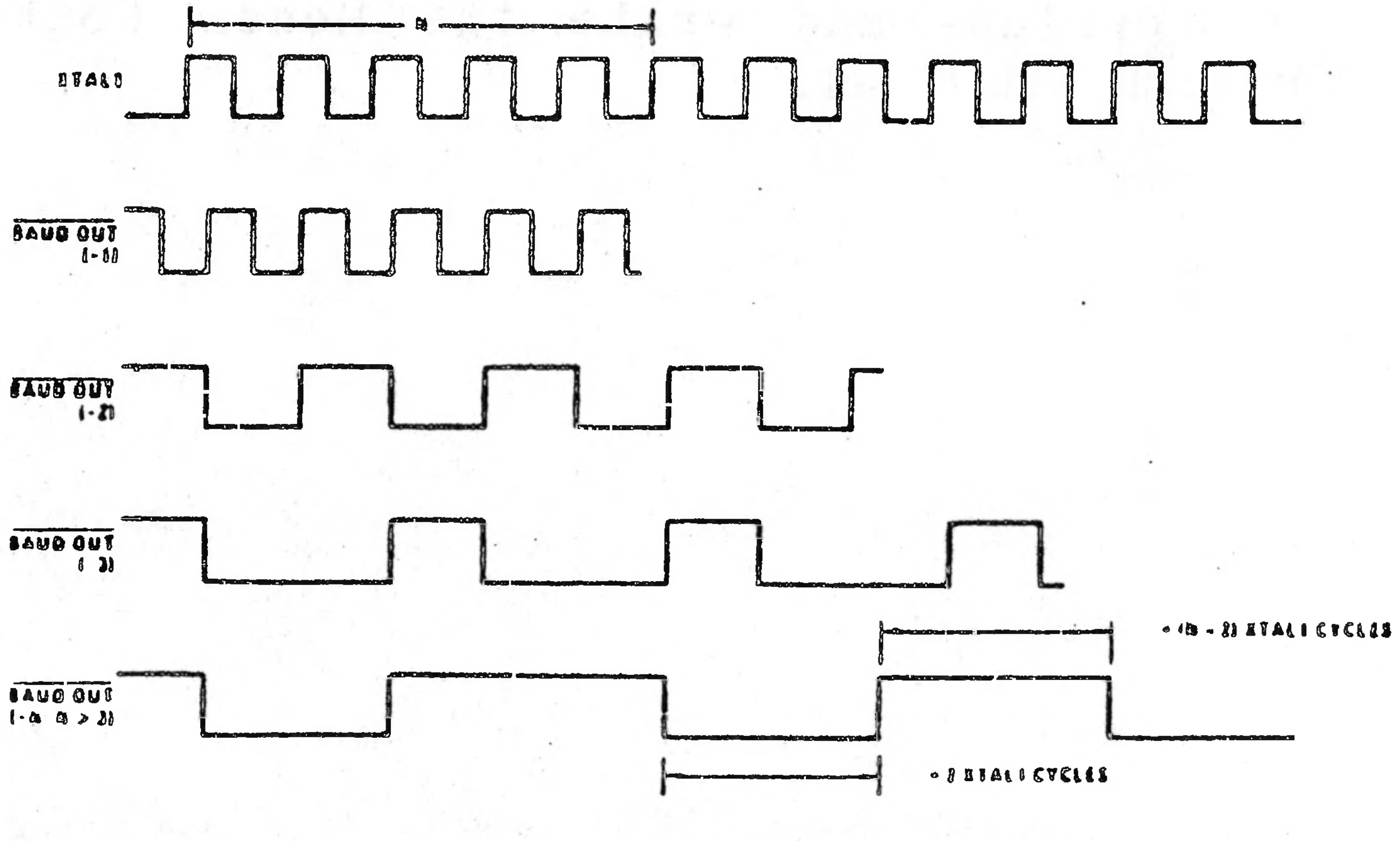


Figure 8.7 BAUDOUT/ timing

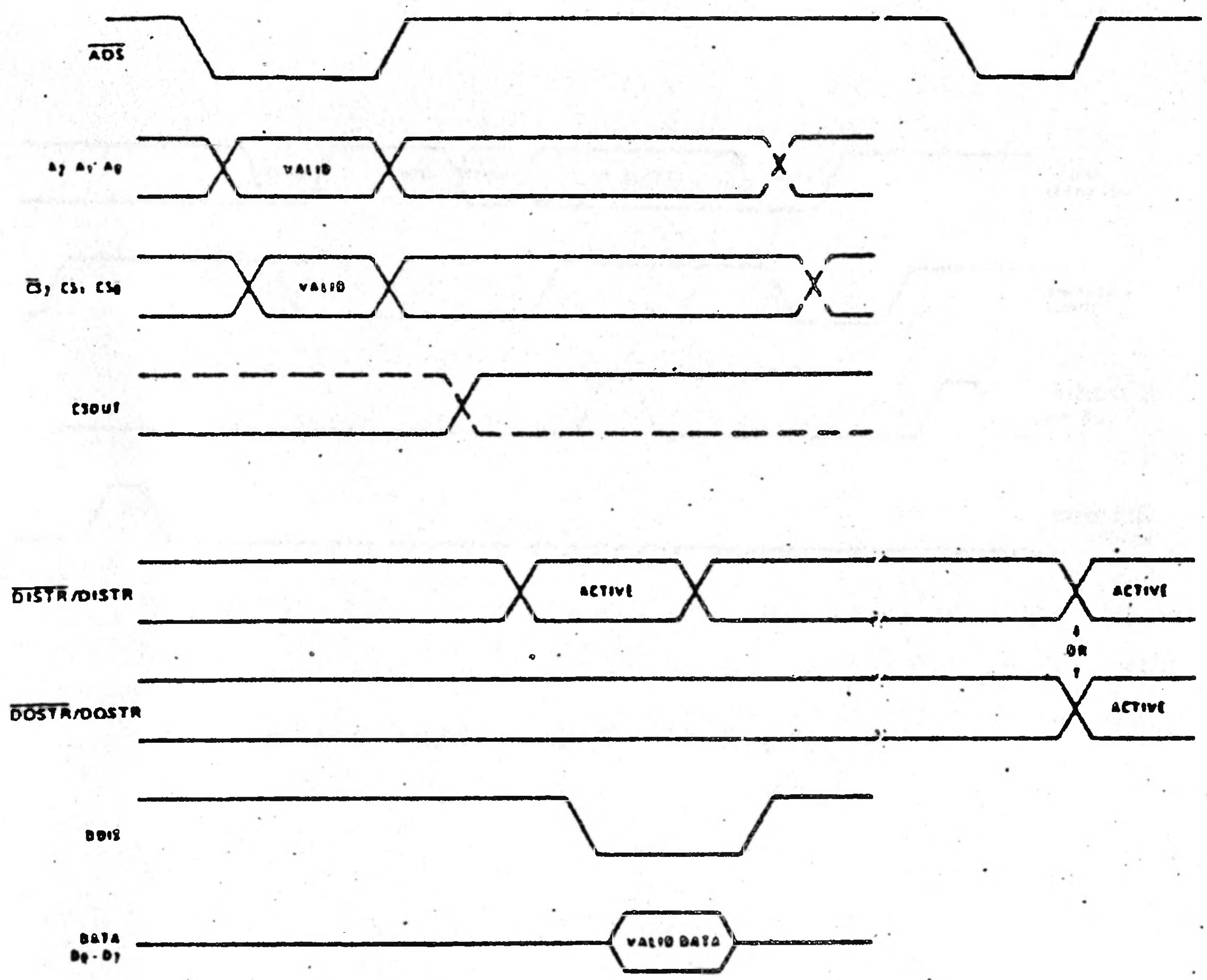


Figure 8.8 Write cycle

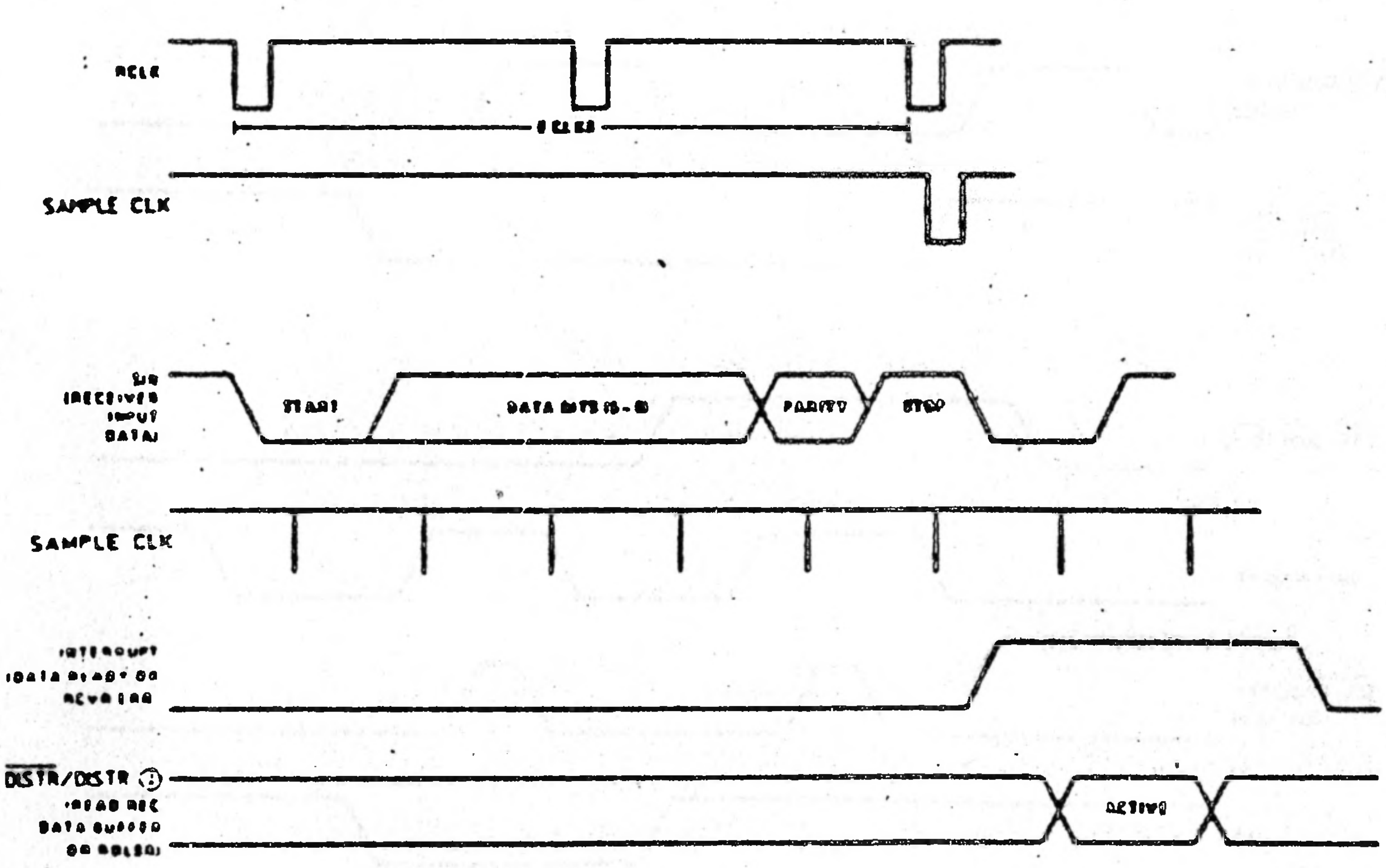


Figure 8.9 Receiver timing

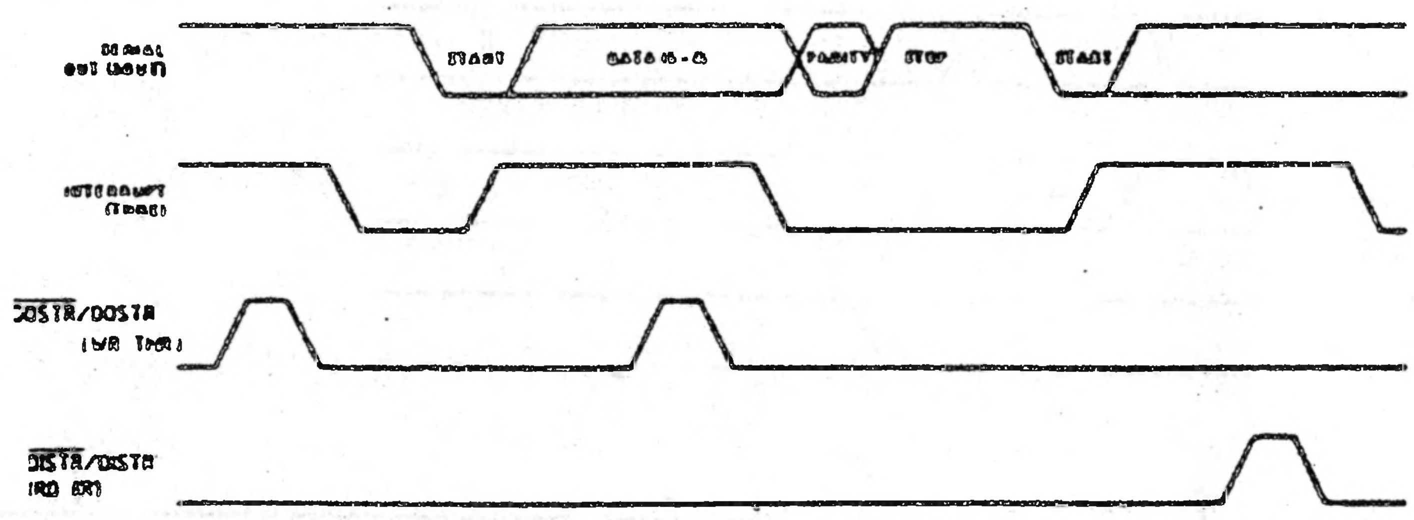


Figure 8.10 Transmitter timing

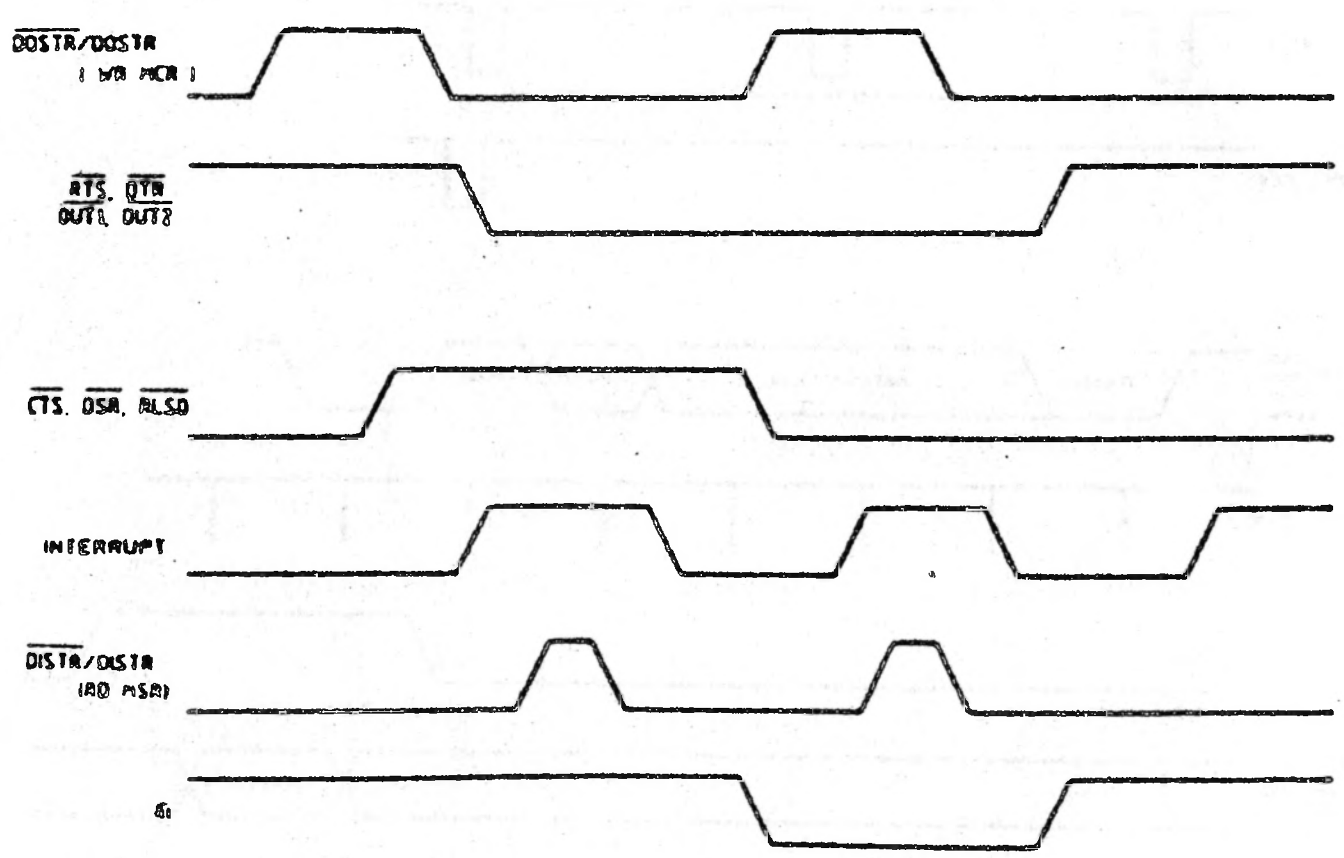


Figure 8.11 Modem Control timing

BAUD RATE SELECTION

The crystal input governing the 16450 internal baud rate generator in your NCR PERSONAL COMPUTER is set at 1.8432 MHz. Accordingly, the 16-bit Divisor Latch values for the standard baud rates are as set out in Figure 8.12. Where the integer nature of 16-bit binary counting results in a negligible deviation from the nominal baud rate, this is indicated in the rightmost column.

Nominal baud rate	Divisor Latch [hexadecimal]	Actual deviation [%]
50	900	
75	600	0.026
110	417	
134.5	359	0.058
150	300	
300	180	
600	C0	
1200	60	
1800	40	
2000	3A	0.69
2400	30	
3600	20	
4800	18	
7200	10	
9600	C	
19200	6	

Figure 8.12 Baud Rate Divisor Latch

THE CENTRONICS INTERFACE

The Centronics interface provides a parallel connection to an external input/output device. Up to two parallel interfaces can be used (2 x 3299-K306). Base port selection is by means of switches on the Kit PCB. The following base ports are selectable:

278H
378H

The interface provides 8 TTL buffered data lines, 4 TTL buffered control lines, and 5 lines for status reading. Three basic operations can be performed:

* Write data to device.
* Read data from device.
* Read status of device.

Figure 8.13 shows the logical significance of the interface signals. Physical pin connections of the D-connector are set out in Figure 8.14.

Control data comprises the following lines:

STROBE/ The pulse of at least 0.5 microseconds used to clock data read. Data is read when this signal is active (high)

AUTO/ This signal is commonly recognized by printers as an instruction to perform an automatic line feed when end of line is reached

INIT/ This signal is commonly recognized by printers as a reset instruction, usually entailing erasure of remaining printer buffer contents

SELECT INPUT/ Signal to select the external device (printer)

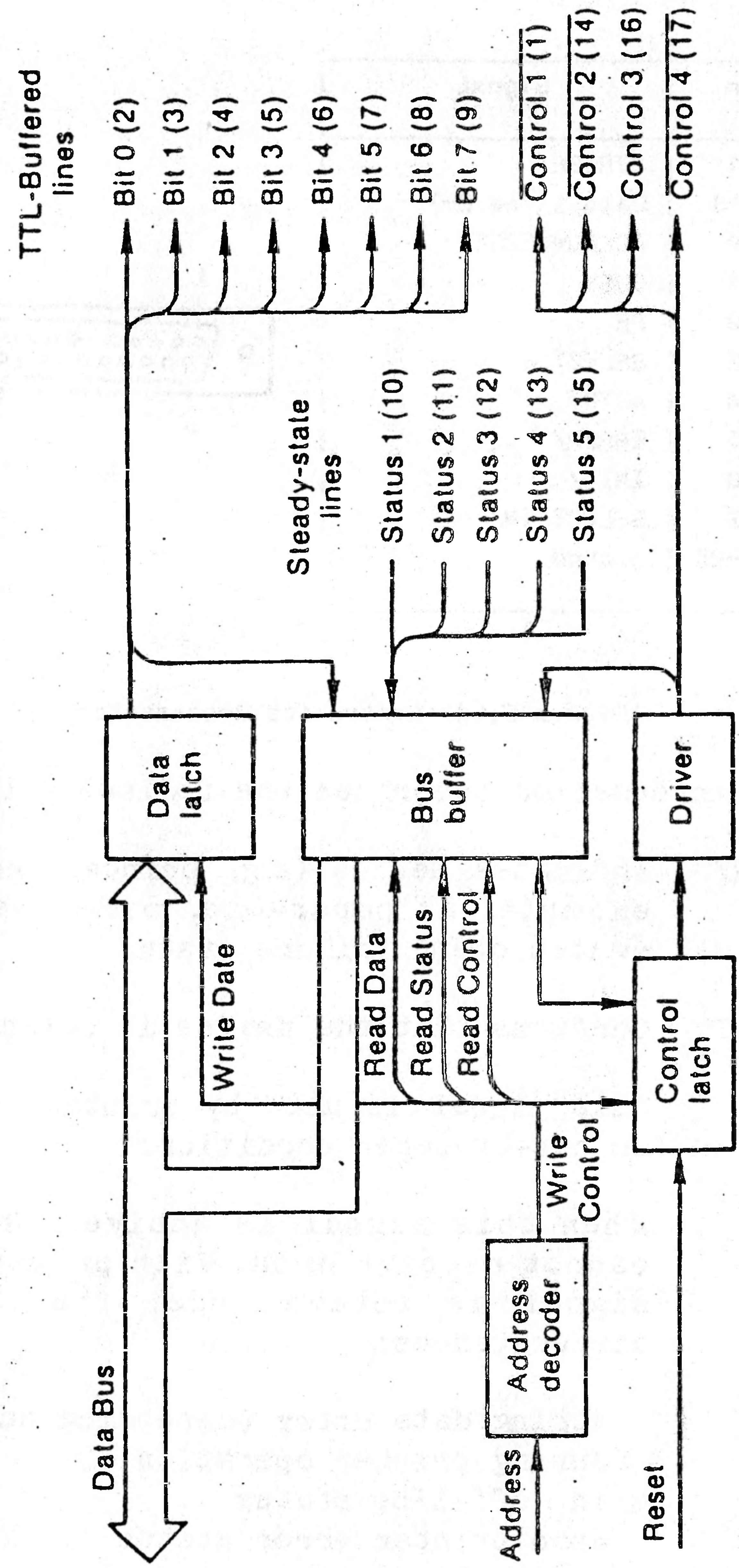


Figure 8.13 Centronics interface signals

Pin	Signal
1	STROBE/
2-9	Data lines 0-7
10	ACKNOWLEDGE/
11	BUSY
12	PE
13	SELECT
14	AUTO/
15	ERROR/
16	INIT/
17	SELECT IN/
18-25	Ground

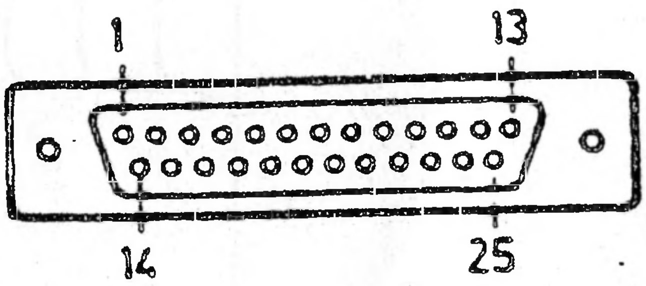


Figure 8.14 Centronics D-connector

Status information comprises the following lines:

ERROR/ Indicates device (e.g. printer) error, for example, at paper-end, off-line, safety switch open, failure status

SELECT Confirms that the device is selected.

PE This signal is used by printers to denote an out-of-paper condition.

BUSY When this signal is active, the device cannot receive data. With printers, this signal is active under the following circumstances:

during data entry (depending on printer)
during printer operation
in off-line status
upon printer error status
during line feed

ACKNOWLEDGE/
Indicates that data has been received by the printer. New data cannot be received before this signal is reset

SOFTWARE CONTROL

Data transfer between the microprocessor and the interface is via the system data bus. To write data to the external device, the data is transmitted via port 378H/278H. The interface captures the data from the bus and presents it on the data lines at the external connector. Appropriate control information must then be issued via port 37AH/27AH.

To read data from the Centronics interface, it is first necessary to transmit the appropriate control information via port 37AH/27AH. Data can then be read via port 378H/278H.

Status reading is via port 379H/279H.

Status and Control Registers

The status byte is made up as shown in Figure 8.15, the control byte as shown in Figure 8.16.

Device Status (IN 379H/279H) Bit:							
7	6	5	4	3	2	1	0
BUSY	ACKNOW-LEDGE	PE	SELECT	ERROR	<—— not used		——>

Figure 8.15 Centronics status register

Interface Control (OUT 37AH/27AH)							
Bits							
7	6	5	4	3	2	1	0
0	0	0	0	SELECT INPUT	INIT	AUTO	STROBE

Figure 8.16 Centronics control register

PORT SELECTION

Figure 8.17 shows the locations and possible settings for the 3299-K306 switches. The "enable" switches are provided so that one of the interfaces on the adapter can be used, while the other is disabled to prevent an I/O address clash with an interface being used on another adapter 3299-K306 or 3299-K307.

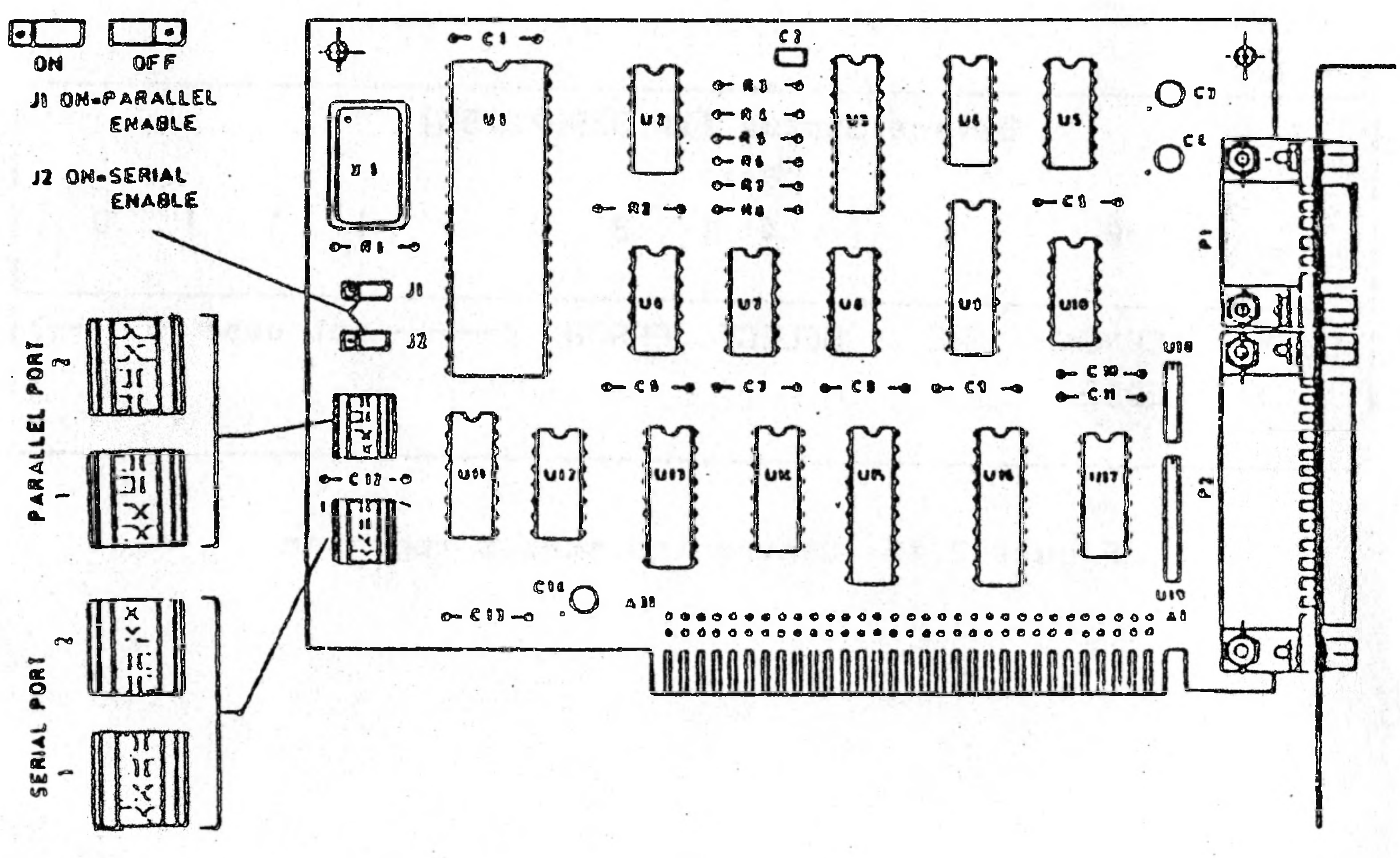


Figure 8.17 K306 I/O address selection

Figure 8.18 shows switch settings for 3299-K307.

	Base Port Address				
	2F8H	278H	378H	3F8H	
SWITCH 1	On	On	Off	On	Port Connector I
SWITCH 2	On	Off	Off	On	
SWITCH 3	On	On	Off	Off	Port Connector II
SWITCH 4	On	Off	Off	On	

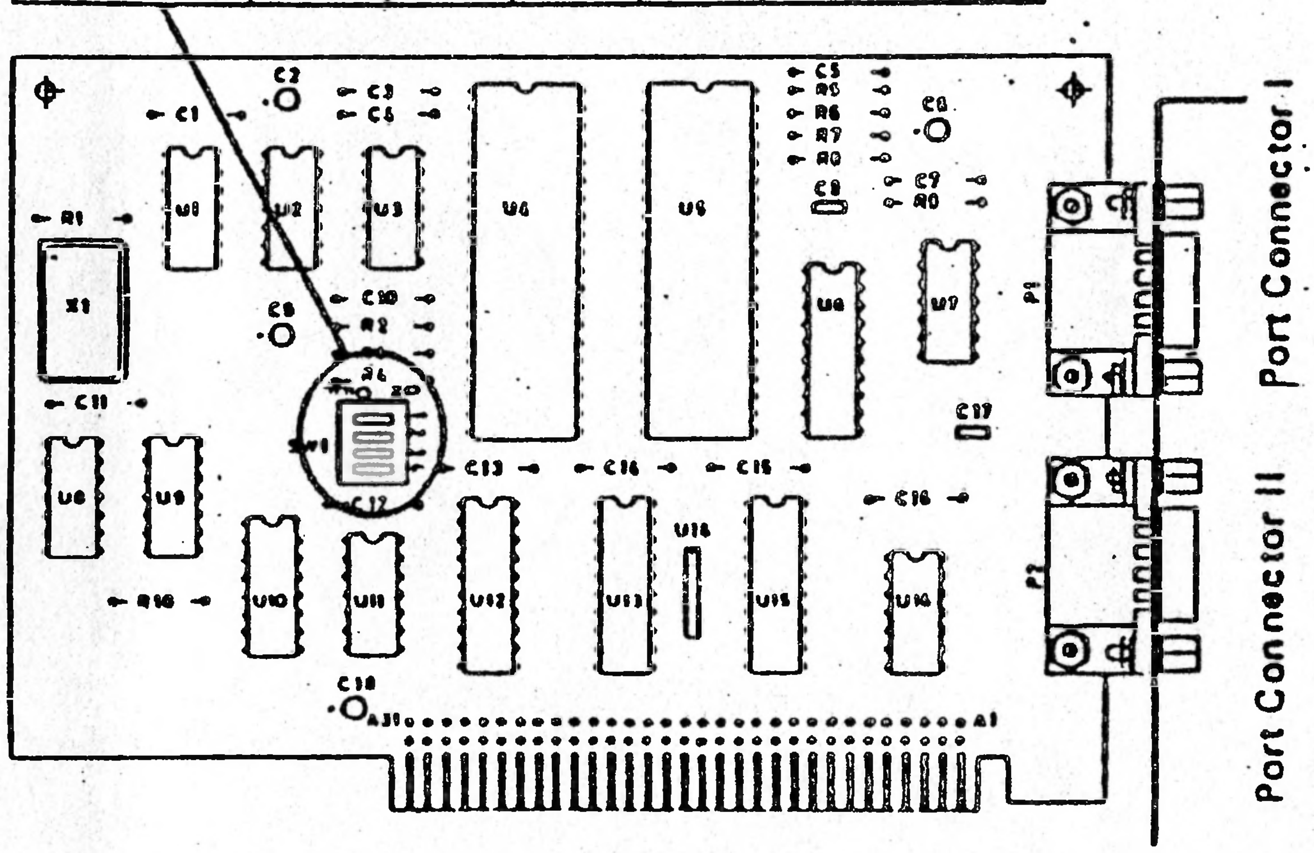


Figure 8.18 K307 I/O address selection