nicht dispositive Stückliste
1 SKS 537 E

Lfd. Nr.	Unterlagenart	Zeichnungsnummer zur Freigabe	Bemerkung	10	11	12	13
1	Stückliste	MC 80 - 96 A	3 Blatt	1	2	3	4
2	Klebeoriginal	80 - 96 - 3	Vorder u. Rückseite		4		5
3	Dia	8o - 96 - 3	Vorder u. Rückseite		4		5
4	Bohrplan	MC 80 - 96	1 Blatt	1	2		3
5	Bestückungsplan	MC 8o - 96 A	1 Blatt	1	2	3	4
6	Logikplan	MC 8o - 96	3 Blatt	1	2	3	
7	Steckerbelegungsliste	MC 80 - 96	4 Blatt	1	2		
8	Signalbenennungsliste	MC 80 - 96	1 Blatt	1			
9	El. Spezifikation	MC 80 - 96	1 Blatt	1			
10	Tech. Funktionsbeschreibung	MC 8o - 96	37 Blatt	1	2		
11	Blockschaltbild	MC 80 - 96	1 Blatt	1			
12							
13							
14							
15							
			Baugruppenänderungsstand	10	11	12	13
			Nr. der Änderungsanweisung		1557	1558	1576

Liste ist Bestandteil der Baugruppenstückliste.

Ersetzt durch: | Liste ungültig am:

Ausgabe	Änderung	Tag	Name
1	Freigabe		

83	Tag	Name
Bearb.	14.6	S.H.
Gepr.		
Norm		

MEDIA - CONTROLLER

MC 80 - 96 A

80 - 96

Blatt 3

Steinmetz Krischke Systemtechnik GmbH Ettlingen

Änderungsmitteilung

Änderungsnummer E 1557

Unterlagen-Nr.	MC 80 - 96 A
Bezeichnung:	Media - Controller
Bemerkung:	

Kopien an:	Unterschrift	Datum
GF (SEL 3)		
Hr. Auerswald		
Hr. Schiller		
Hr. Kufner		
Hr. Weißflog		
Hr. Bähr		
Hr. Schrauber		

Änderung:

In die Unterlage wird die Leiterplatte mit Index -4 aufgenommen

Begründung:

Zusaätzlicher Floppy-Abgang

Einführungstermin: sofort

Kannänderung [x]

Mußänderung [ ]

Zu ändernde Unterlagen:

- Stückliste
- Klebeoriginal, Dia
- Bohrplan
- Bestückungsplan
- Logikplan
- Steckerbelegungsliste
- Techn. Funktionsbeschreibung

Datum: 8.9.1983	Antragst.: Bittmann	Bearb.: Bittmann

Originalablage bei: SKS - Dokumentation Elektronik

Steinmetz Krische Systemtechnik GmbH Ettlingen

Änderungsmitteilung

Änderungsnummer
E 1558

Unterlagen-Nr.	MC 80 - 96 A, C
Bezeichnung:	Media - Controller
Bemerkung:	

Kopien an:	Unterschrift	Datum
GF (SEL 3)		
Hr. Auerswald		
Hr. Schiller		
Hr. Küfner		
Hr. Weißflog		
Hr. Bähr		
Hr. Schrauber		

Änderung:

Widerstandsnetzwerk A1, MDP 1405 220/330R

wird durch Netzwerk MDP 1401 150R ersetzt

Pin 7 von A1 ist auf der Leiterplatte abzutrennen

Begründung:

Lieferschwierigkeiten des Herstellers

Einführungstermin: sofort

Kannänderung [x]

Mußänderung [ ]

Zu ändernde Unterlagen:

- Stückliste
- Bestückungsplan
- Logikplan

Datum: 8.9.1983	Antragst.: Schiller	Bearb.: Bittmann

Originalablage bei: SKS - Dokumentation Elektronik

Steinmetz Krische Systemtechnik GmbH Ettlingen

Änderungsmitteilung

Änderungsnummer
E 1576

Unterlagen-Nr.	MC 80 - 96 A/C
Bezeichnung:	Media Controller
Bemerkung:	

Kopien an	Unterschrift	Datum
GF (SEL 3)		
Hr. Auerswald		
Hr. Schiller		
Hr. Küfner		
Hr. Weißflog		
Hr. Bähr		
Hr. Schrauber		

Änderung:

Änderung E 1558 fließt in die Kaschierung ein

Kondensator 10 µF/20V ETS wird durch

Tantal-Kondensator 10 µF/35V ETP ersetzt

Kaschierungsraster für den Kondensator wird berichtigt

Leiterplatten Index -5

Baugruppen Index -13

Begründung:

Überarbeitung des Klebeoriginals

Einführungstermin: sofort

Kannänderung [x]

Mußänderung [ ]

Zu ändernde Unterlagen:

- Stückliste
- Klebeoriginal, Dia
- Bestückungsplan
- Bohrplan

Datum: 19.9.1983	Antragst.: Bittmann	Bearb.: Bittmann

Originalablage bei: SKS - Dokumentation Elektronik

Losgröße	Ausstelldatum	Termin	Fertigungsstätte	EKE	Auftrags-Nr. LH

Bezeichnung: MEDIA - CONTROLLER — Zn.-Nr.: MC 80 - 96 A

1 Lfd. Nr.	2 Stück-zahl	3 Benennung	4 Sach-Nr	5 Bemerkung	6 Soll	7 Ist
1	1	Leiterplatte	80 - 96 - 5			
2						
3	2	IC SN 74 LS 00		Texas		
4	1	IC SN 74 S 04		Texas		
5	1	IC SN 74 LS 04		Texas		
6	1	IC SN 74 LS 14		Texas		
7	1	IC SN 74 LS 20		Texas		
8	4	IC SN 74 38		Texas		
9	1	IC SN 74 LS 85		Texas		
10	1	IC SN 74 LS 138		Texas		
11	1	IC SN 74 LS 240		Texas		
12	2	IC SN 74 LS 244		Texas		
13	2	IC SN 74 LS 273		Texas		
14	1	IC SN 74 LS 640		Texas		
15						
16	1	IC 1797		Western-Digital Siemens		
17						
18	1	IC 9229 B		SMC		
19						
20						
21	1	IC Sockel 40 pol.	641 606 - 3	AMP		
22	1	IC Sockel 20 pol.	641 602 - 3	AMP		
23						
24	1	Quarz 16.0 MHz Grundwelle,Metallausfg.	HC 18 UTol. $\pm 10^{-4}$			
25						

Ausgabe	Änderung	Tag	Name
4	1576	29.9.	Bi
2	1557	23.8.	Bi
1	Freigabe		

	Tag	Name
Bearb	14.6	S.H.
Gepr.		
Norm		

Material gerichtet am: ..... von: .....

Verwendung

Stewmetz Kirschke Systemtechnik GmbH Karlsruhe

MEDIA - CONTROLLER

MC 80 - 96 A

Bestent aus 3 Bl

Blatt Nr. 2

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Losgröße	Ausstelldatum	Termin	Fertigungsstätte	SKS	Auftrags-Nr. LH

Bezeichnung: MEDIA - CONTROLLER — Zn.-Nr.: MC 80 - 96 A

1 Lfd. Nr.	2 Stück-zahl	3 Benennung	4 Sach-Nr.	5 Bemerkung	6 Soll	7 Ist
26						
27	1	Keramik - Kondensator 220pF / 50V	MA 10 5A 221 JAA	AVX		
28	12	Keramik - Kondensator 0,1 µF / 50V	MA2o 5E 104 ZAA	AVX		
29		Tantal-Kondensator 10uF/35V	ETP	Roederstein		
30						
31	1	Widerstandsnetzwerk 150R	MDP 1401/ 899-1	Dale /Beckman		
32	2	Widerstandsnetzwerk Sip 150R ± 10%	C44	Matsushita		
33						
34	4	Widerstand 1K ± 5%	0207	Vitrohm / Beyschlag		
35	2	Widerstand 2K2 ± 5%	0207	Vitrohm / Beyschlag		
36	2	Wicerstand 10K ± 5%	0207	Vitrohm / Beyschlag		
37						
38						
39	n.B.	Silberdraht Ø 0,8 mm				
40						
41	1	Haftetikett	8 x 12 / 2310	Herma		
42						
43	1	Stiftleiste 96 pol.	PI 96 B30 P00 F00	Burndy		
44						
45	1	Frontplatte III	2 MIC 045 E			
46	2	Senkschraube M 2,5 x 8	DIN 963	vernickelt		
47						
48						
49						
50						

Ausgabe	Änderung	Tag	Name
3	1558	23.8.	Bi
2	1557	23.8	Bi
1	Freigabe		

	Tag	Name
Bearb	14.6	S.P.
Gepr		
Norm		

Stemmetz Krische Systemtechnik GmbH Karlsruhe

Material genehmigt am: ..... von: .....

Verwendung

MEDIA - CONTROLLER

MC 80 - 96 A

bestent aus 3 B.

Blatt Nr. 3

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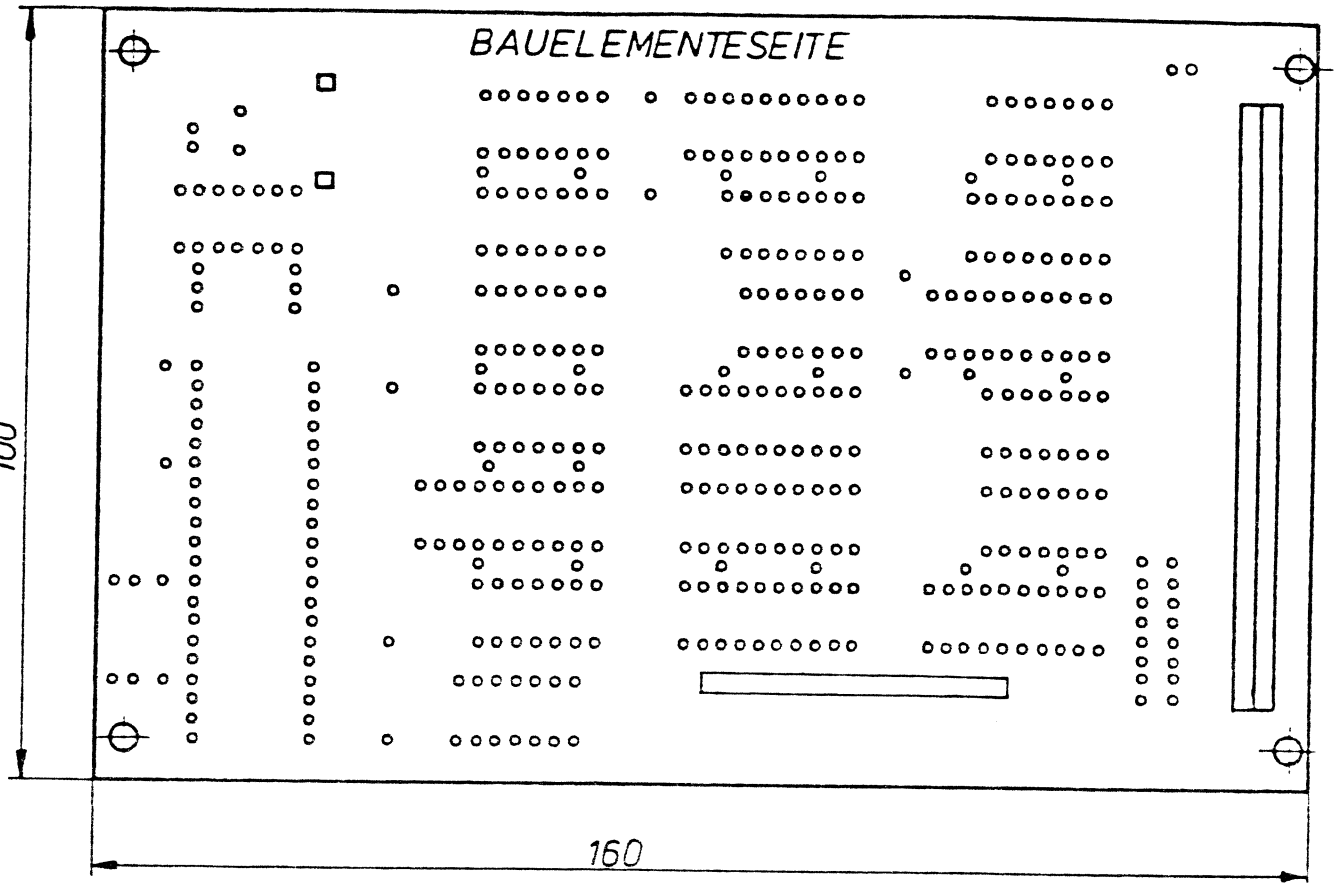


▭ = 1,0 mm
o = 0,8 mm
Rest = 0,6 mm
} durchkontaktiert

⊕ = 2,8 mm nicht durchkontaktiert

3	1576	29.9.88	Bi
2	1557	24.8.88	Bi
1	Freigabe		
Aus-	Änderung	Tag	Name

	Tag	Name
Bearb	25.8	
Gepr		
Norm		

Steinmetz Krischke Systemtechnik GmbH

BOHRPLAN

MEDIA CONTROLLER

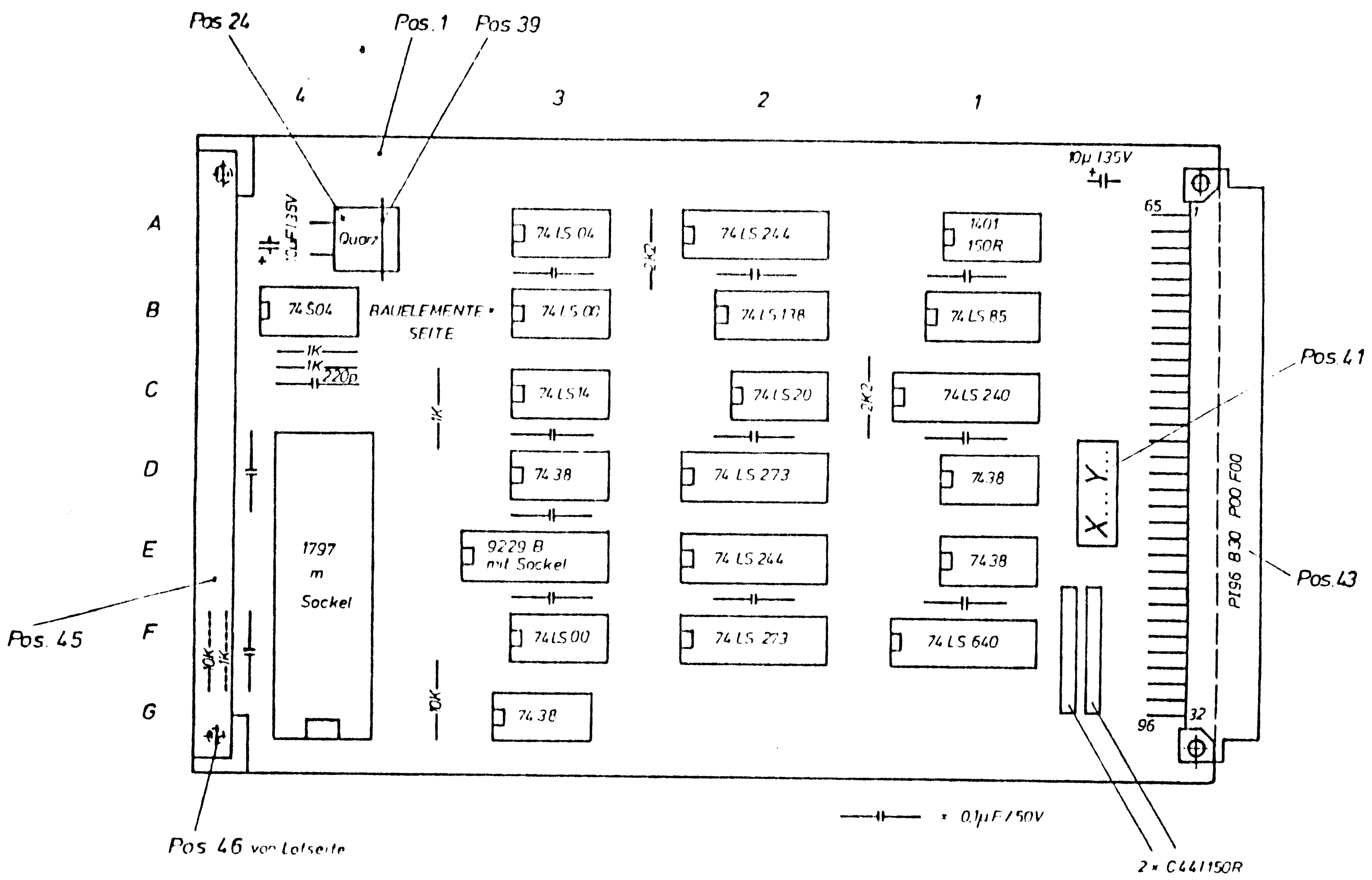
MC 80 - 96

Maßstab 1 : 1

Verwendung

besteht aus 1 Blatt

Blatt-Nr.



X Kennzeichnung des Herstellers

Y gefertigter Baugruppenstand

Ausgabe	1	2	3		SKS GmbH	MEDIA CONTROLLER	Maßstab ./.	Bestuckungsplan
Tag		23.8.7[illegible]	23.8.7[illegible]					MC 80 - 96 A
Name		[illegible]	[illegible]					Blatt 1

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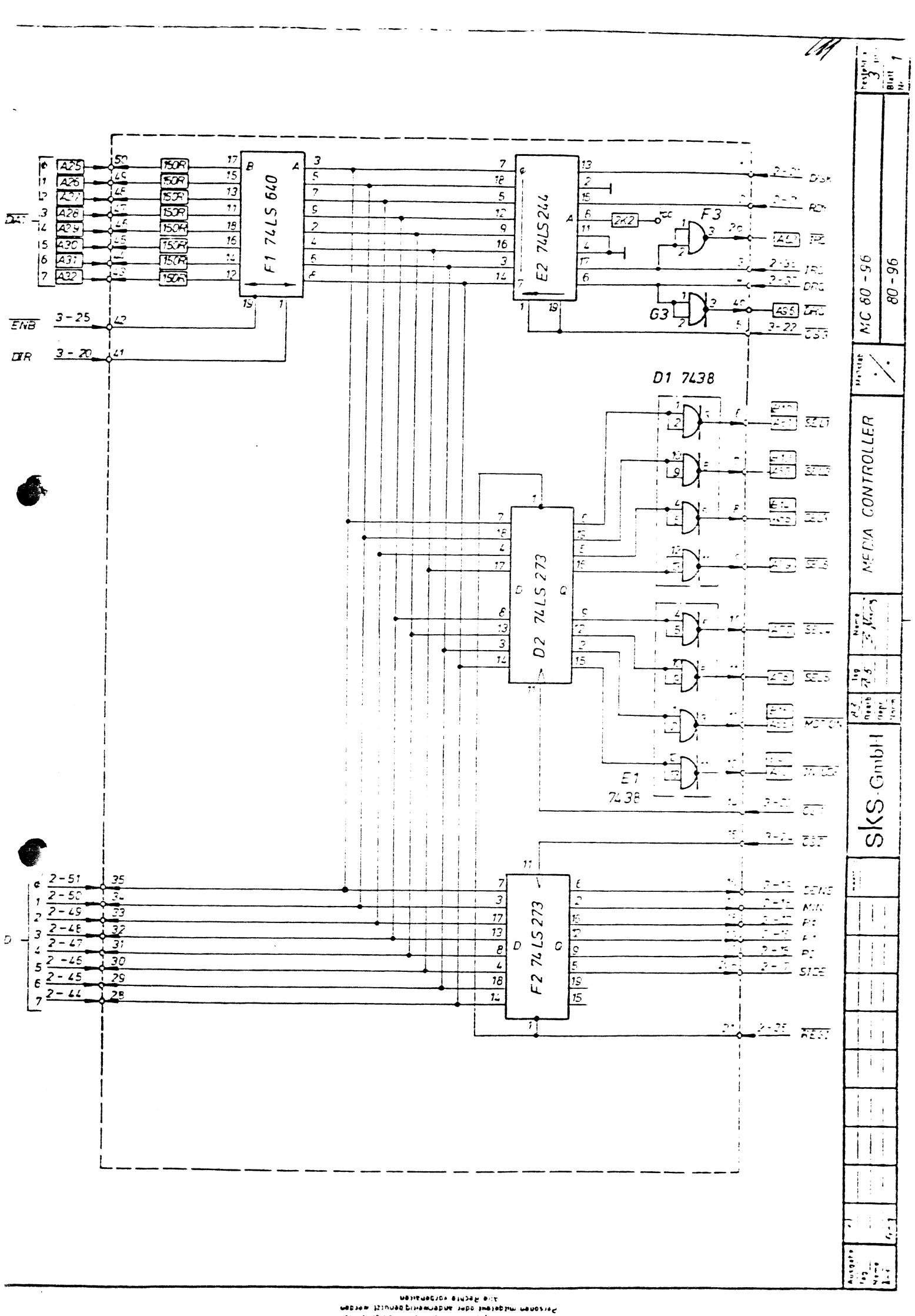
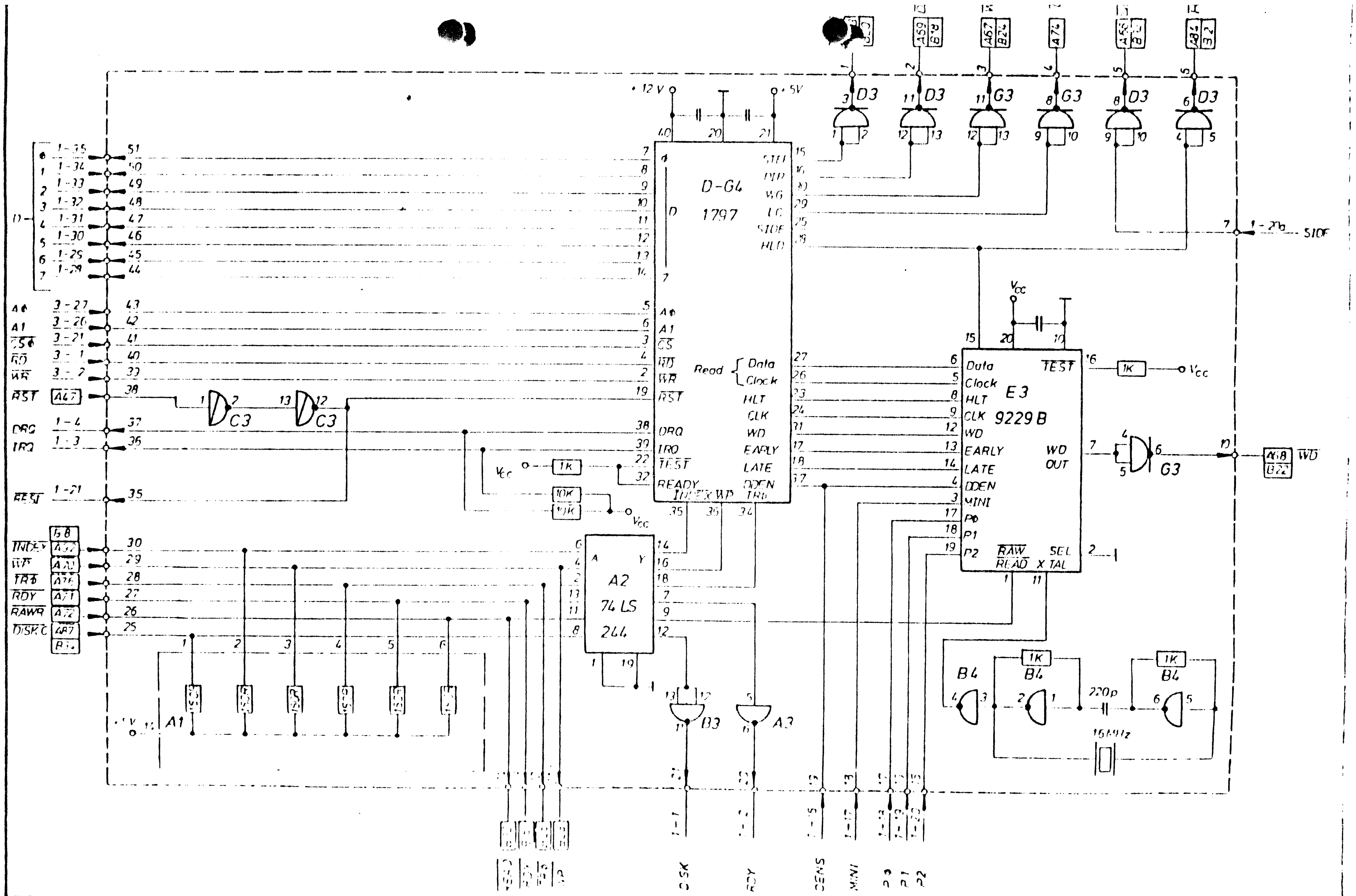

F1 74LS 640
E2 74LS244
D2 74LS 273
F2 74LS 273
D1 7438
E1 7438
F3
G3
2K2
ENB
DIR
3 - 25
3 - 20
A25
A26
A27
A28
A29
A30
A31
A32
150R
DISK
RDY
IRQ
DRQ
3 - 22
D
2 - 51
2 - 50
2 - 49
2 - 48
2 - 47
2 - 46
2 - 45
2 - 44
MC 60 - 96
80 - 96
MEDIA CONTROLLER
SKS-GmbH



SKS GmbH	MEDIA-CONTROLLER	MC 80-96
		80-96

Blatt 3, Nr. 2

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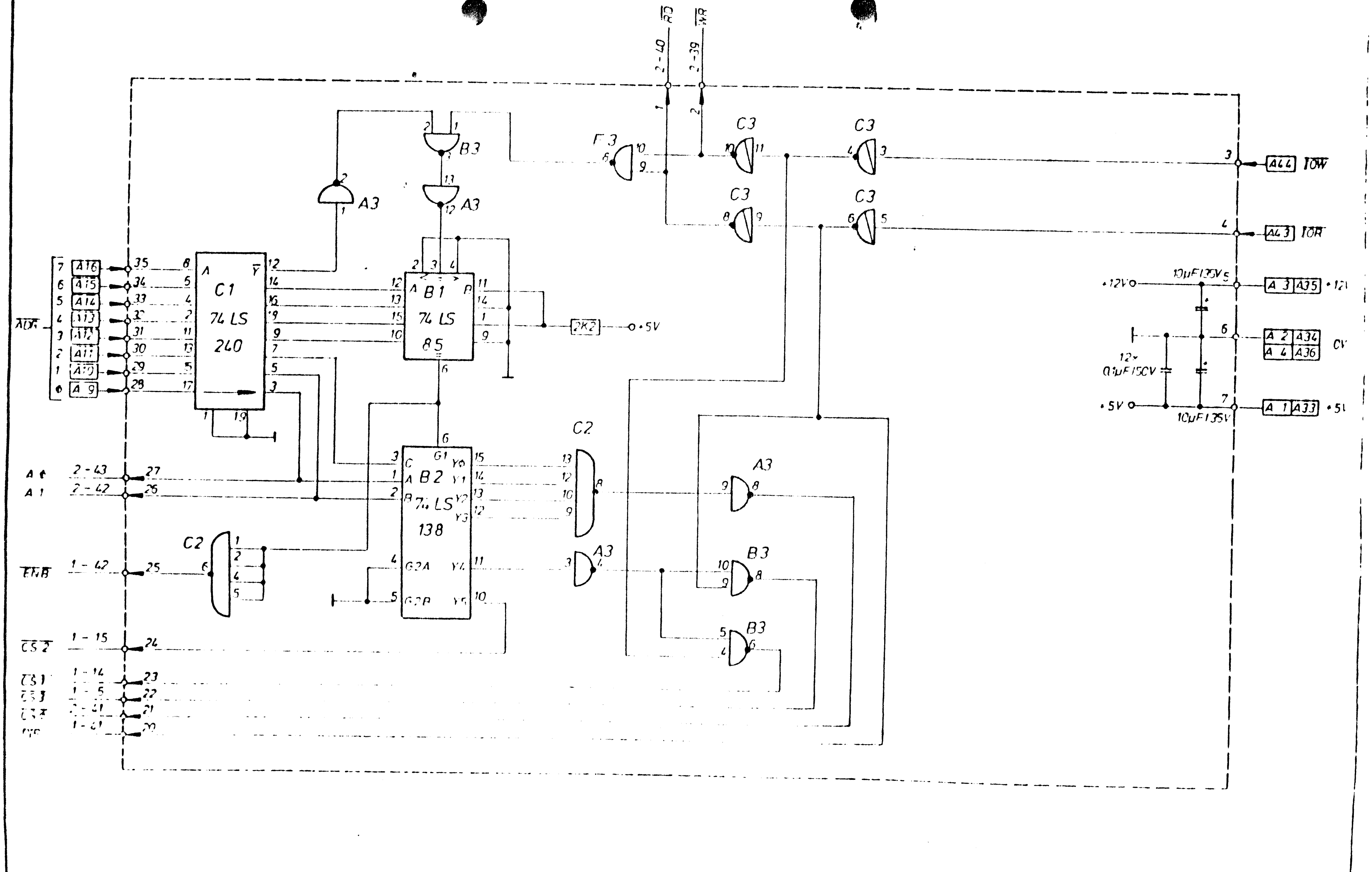


sks-GmbH	Bearb. 5.4.	Name	MEDIA CONTROLLER	Maßstab	MC80 - 96
					80 - 96
					Blatt Nr. 3

Personen zugänglich oder anderweitig benutzt werden
Alle Rechte vorbehalten

SKS GmbH	STECKERBELEGUNGSLISTE	STECKER : B

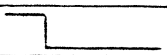
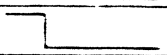
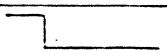
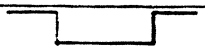
PIN	Bezeichnung	Diagramm	Erläuterungen	Blatt Nr
01	+5V			
02	0V			
03	+12V			
04	0V			
05	-12V			
06	0V			
07				
08				
09	$\overline{\text{ADR 0}}$		Adress-Bit 0	
10	$\overline{\text{ADR 1}}$		Adress-Bit 1	
11	$\overline{\text{ADR 2}}$		Adress-Bit 2	
12	$\overline{\text{ADR 3}}$		Adress-Bit 3	
13	$\overline{\text{ADR 4}}$		Adress-Bit 4	
14	$\overline{\text{ADR 5}}$		Adress-Bit 5	
15	$\overline{\text{ADR 6}}$		Adress-Bit 6	
16	$\overline{\text{ADR 7}}$		Adress-Bit 7	
17				
18				
19				
20				
21				
22				
23				
24				
25	$\overline{\text{DAT 0}}$		Daten-Bit 0	
26	$\overline{\text{DAT 1}}$		Daten-Bit 1	
27	$\overline{\text{DAT 2}}$		Daten-Bit 2	
28	$\overline{\text{DAT 3}}$		Daten-Bit 3	
29	$\overline{\text{DAT 4}}$		Daten-Bit 4	
30	$\overline{\text{DAT 5}}$		Daten-Bit 5	
31	$\overline{\text{DAT 6}}$		Daten-Bit 6	
32	$\overline{\text{DAT 7}}$		Daten-Bit 7	

Nr	Änderung	TTMMJJ	Name
1	Freig.		

198 TTMM Name	Bezeichnung	Blatt Nr
Autor	Media Controller	1
Gepr	Unterlagen Nr.: MC 80 - 96	von 1
Kontrb		
Datei	Referenz-Baugruppe	Seite

SKS

SKS GmbH	STECKERBELEGUNGSLISTE	STECKER : B

PIN	Bezeichnung	Diagramm	Erlauterungen	Blatt Nr
33	+5V			
34	OV			
35	+12V			
36	OV			
37	-12V			
38	OV			
39				
40				
41				
42				
43	$\overline{IOR}$		IN/OUT Read	
44	$\overline{IOW}$		IN/OUT Write	
45				
46				
47	$\overline{RST}$		Reset intern	
48				
49				
50				
51				
52				
53				
54				
55				
56				
57				
58				
59				
60				
61				
62	$\overline{IRQ}$		Interrupt Request	
63				
64				

			1983	TTMMJJ	Name	Bezeichnung: Media Controller — Blatt Nr: 2
			Gepr.			
			Freigb.			Unterlagen Nr: MC 80 - 96 — von: 4
1	Freig.		SKS			Referenz- Baugruppe — Seite
Nr	Anderung	TTMMJJ	Name			

sks GmbH	STECKERBELEGUNGSLISTE	STECKER: B

PIN	Bezeichnung	Diagramm	Erläuterungen	Blatt Nr.
65	$\overline{\text{MOTON}}$		Motor EIN	
66	$\overline{\text{SIDE}}$		Diskettenseite-Anwahl	
67	$\overline{\text{WG}}$		Schreibstrom-Freigabe	
68	$\overline{\text{WD}}$		Schreibdaten	
69	$\overline{\text{DIR}}$		Richtung zur Diskettenmitte	
70	$\overline{\text{WP}}$		Schreibschützung	
71	$\overline{\text{RDY}}$		Antrieb-Bereitmeldung	
72	$\overline{\text{RAWR}}$		Ungetrennte Lesedaten	
73				
74	$\overline{\text{LC}}$		Reduzierter Schreibstrom	
75				
76	$\overline{\text{TR 0}}$		Spur ØØ Position	
77	$\overline{\text{SEL 4}}$		Anwahl-Antrieb 4	
78	$\overline{\text{SEL 5}}$		Anwahl-Antrieb 5	
79	$\overline{\text{SEL 6}}$		Anwahl-Antrieb 6	
80				
81	$\overline{\text{SEL 1}}$		Anwahl-Antrieb 1	
82	$\overline{\text{SEL 2}}$		Anwahl-Antrieb 2	
83	$\overline{\text{STEP}}$		Schrittmotor Puls	
84	$\overline{\text{HLD}}$		Schreib-Lese-Kopf anziehen	
85	$\overline{\text{SEL 3}}$		Anwahl-Antrieb 3	
86	$\overline{\text{INUSE}}$		Door-Lock Option	
87	$\overline{\text{DISKC}}$		Diskette gewechselt	
88				
89				
90				
91				
92	$\overline{\text{INDEX}}$		Index-Puls	
93				
94				
95				
96	$\overline{\text{DRQ}}$		Data-Request	

			1983 TTM Kommel	Bezeichnung	Blatt Nr.
			Autor	Media Controller	3
			Datum	Unterlagen Nr.:	von
			Gez. 18.9	MC 80 - 96	4
1	Freig.		sks	Referenz-Baugruppe	Seite
Nr.	Änderung	TTM	Name		

Platte: 80 - 96

Stecker B

Pin	Farbe	Signal	verbunden mit Stecker	Pin	Pin	Farbe	Signal	verbunden mit Stecker	Pin
1		OV			2		HLD	A	84
3		OV			4		$\overline{\text{INUSE}}$	A	86
5		OV			6		$\overline{\text{RDY}}$	A	71
7		OV			8		$\overline{\text{INDEX}}$	A	92
9		OV			10		$\overline{\text{SEL 1}}$	A	81
11		OV			12		$\overline{\text{SEL 2}}$	A	82
13		OV			14		$\overline{\text{SEL 3}}$	A	85
15		OV			16		$\overline{\text{MOTON}}$	A	65
17		OV			18		$\overline{\text{DIR}}$	A	69
19		OV			20		$\overline{\text{STEP}}$	A	83
21		OV			22		$\overline{\text{WD}}$	A	68
23		OV			24		$\overline{\text{WG}}$	A	67
25		OV			26		$\overline{\text{TR0}}$	A	76
27		OV			28		$\overline{\text{WP}}$	A	70
29		OV			30		$\overline{\text{RAWR}}$	A	72
31		OV			32		$\overline{\text{SIDE}}$	A	66
33		OV			34		$\overline{\text{DISKC}}$	A	87

83	Tag	Name	
Bearb	10.8	S.H.	MEDIA CONTROLLER
Gepr			
Norm			
1 Freigabe		SKS-GmbH	MC80 - 96
Ausg.	Änderung	Tag	Name

Verwendung

bestehend aus — Blatt

SKS 510 E 96/62

sks GmbH	SIGNALBENENNUNGSLISTE	
Kurzbezeichnung	Erläuterung interner Signale	Blatt Nr
CS Ø - 3	Chip - Selekt Ø bis 3	
P Ø - 3	Kompensations-Steuersignale Ø bis 3	
DISK	Diskette gewechselt	
ENB	Enable Bus	
RESI	Reset Intern	
DENS	Auswahl Schreibdichte	
MINI	Umschaltung 8" - 5 1/4"	

1	Freigabe			1983 6.9.	Media Controller	1
					MC 80 - 96	1
				sks		

sks GmbH | ELEKTRISCHE SPEZIFIKATION

[X] Stromversorgung
[X] Zeitzentrale
[ ] Schnittstellen
[ ] Timing-Diagramme

Spezifikation MC80 - 96

Stromaufnahme: + 5 V : < 400 mA

+ 12 V : < 15 mA

Taktgenerator: 16 MHz ± 10-4

				1983	TTMM	Name	Bezeichnung: Media - Controller	Blatt Nr. 1
				Autor	29.8			
				Geor			Unterlagen Nr.: MC 80 - 96	von 1
				Bearb				
				Doku				
1	Freigabe			sks			Referenz-Baugruppe:	Seite
Nr.	Änderung	TTMMJJ	Name					

Media - Controller

Eigenschaften:

Single und Double Density
8", 5 1/4" und Mikrofloppy
IBM 3740 (FM)
IBM 34 (MFM)
Schreibkompensation variabel
bis zu 6 Laufwerke anschließbar
250Kbit oder 500Kbit Übertragungsrate

1. Allgemeines:

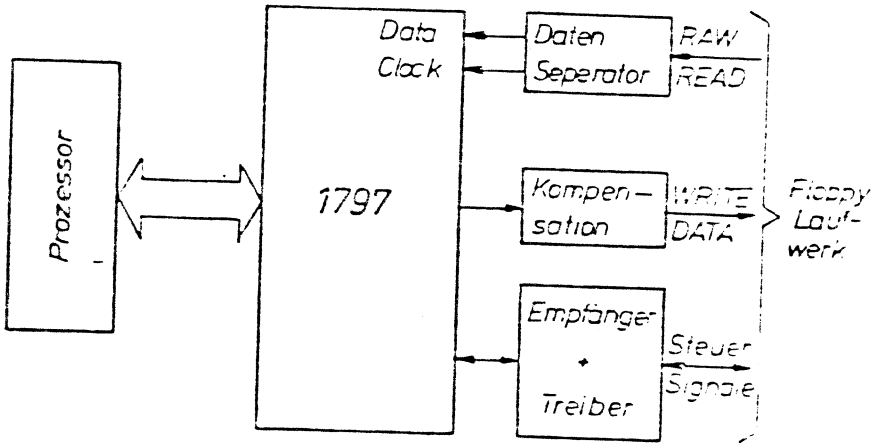
Der Media-Controller MC80-96 basiert auf der Floppy Disk-Controller 1797 und dem Datenseparator 92098 und unterteilt sich in folgende Funktionsblöcke:

- Floppy Disk Controller/Formatter 1797
- Datenseparator und Floppy-Supportchip 9229
- Disk-Interface
- Bus-Interface

Der Anschluß der Laufwerke erfolgt über die c-Reihe der 96-poligen VG-Leiste oder optional über 34-poligen Flachbandkabelstecker.

2. Disk-Controller/Formatter 1797

Der Baustein 1797 stellt mit einigen externen Bausteinen ein komplettes Interface für Standard-Floppy-Laufwerke (8", 5 1/4", 3 1/2") dar.
Er arbeitet sowohl im FM-Verfahren als auch im MFM-Verfahren. Die meisten Signale, die zur Steuerung eines Floppy-Laufwerkes notwendig sind, generiert der 1797 direkt, wie z.B. Write Gate, Step, Direction. Signale vom Laufwerk, wie Index, Write Protect, Track 00 und Ready kann der 1797 direkt empfangen und verarbeiten.



Der 1797 produziert die für die Kompensation notwendigen Signale EARLY und LATE nach folgendem Algorithmus:

				MFM	FM
X	1	1	0	EARLY	EARLY
X	0	1	1	LATE	LATE
0	0	0	1	EARLY	-
1	0	0	0	LATE	-

wurde geschrieben
am Schreiben
soll als nächstes geschrieben werden

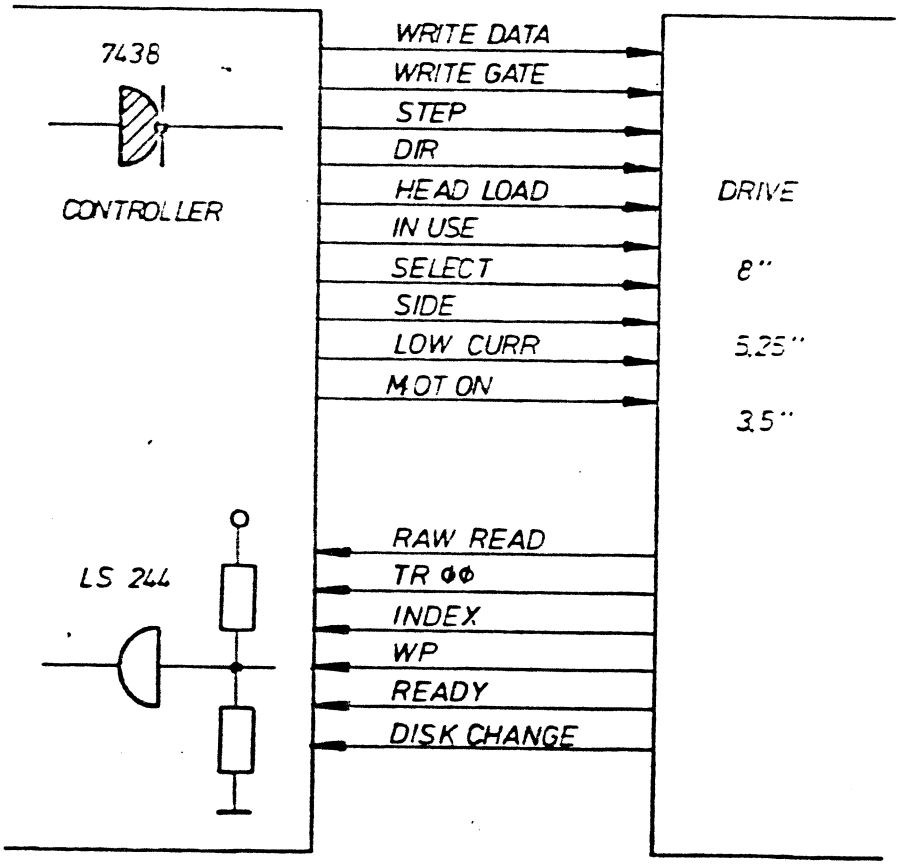
Der 1797 wandelt beim Lesen die serielle Information in eine 8-Bit Information, die der Prozessor aus dem Data-Register lesen kann.
Beim Schreiben wird die parallel vorhandene Information des Data-Registers in eine serielle Information gewandelt und über den WD-Ausgang ausgegeben. Das Spur-Register enthält die momentane Position des Schreib-Lesekopfes des Floppy-Laufwerkes. Das Kommando-Register enthält das aktuelle Kommando während der Ausführung. Dieses Register kann nur geschrieben werden. Das Status-Register kann nur gelesen werden.

3. Datenseparator 9229

Der Baustein 9229 enthält eine Datentrennstufe für FM und MFM kodierte Daten. Der Baustein 1797 benötigt zum Signal Read Data zusätzlich ein Read-Clock Signal, dieses wird im 9229 erzeugt. Zusätzlich hat der 9229 eine Schreibkompensationslogik, die in Abhängigkeit von der Beschaltung der Eingänge P0, P1 und P2 eine variable Kompensation ermöglicht. Bei 8"-Betrieb kann von 0 bis 312,5 Nanosekunden in Schritten von 62,5 ns. kompensiert werden. Bei 5 1/4"-Laufwerken ist die Kompensation von 0 bis 625 ns in 125 ns Schritten einstellbar.
Ein interner Taktgenerator erzeugt das Signal CLK für den 1797, das entweder 2 MHz oder 1 MHz, je nach Anwendung, beträgt.
Um mechanische Reaktionszeiten des Laufwerkes zu berücksichtigen, enthält der 9229 einen Head-Load-Timer, der ein HLT-Signal für den 1797 erzeugt.

4. Disk-Interface

Das Interface zum Floppy-Disk Laufwerk besteht aus einem Register, das die Signale SELEKT 1-6 und das Signal Motor ON erzeugt. Alle anderen Signale werden vom 1797 in Verbindung mit dem Baustein 9229 erzeugt. Alle Leitungen zum Laufwerk gehen über Treiber vom Typ 7438. Alle Empfänger haben Schmitt-Triggereingange und einen Abschluß von 220/330 Ohm.



5. BUS-Interface

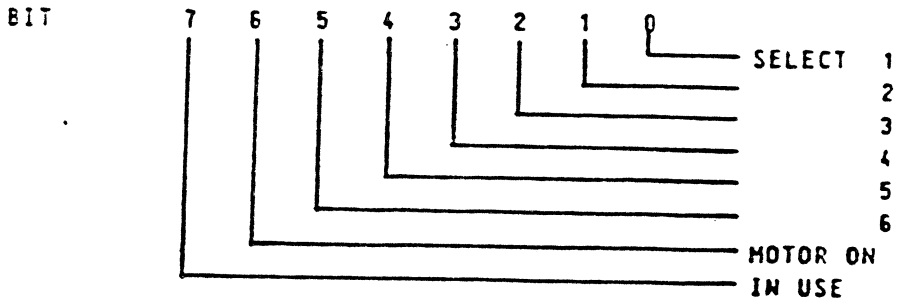
Das BUS-Interface besteht aus einem 74LS640 als bidirektionalem Datentreiber und einer Adressdekodierschaltung. Mittels eines Vergleichers werden die Adressbits 4 bis 7 als Kartenadresse dekodiert. Das DRQ-Signal (Data Request) des 1797 ist über einen Treiber auf den Bus gelegt, um damit einen DMA-Controller anzusteuern. Bei einer Übertragungsrate von 500 Kbit ist das Übertragen von Daten zwischen Speicher und Media-Controller nur im DMA-Betrieb möglich.

Adressbelegung:

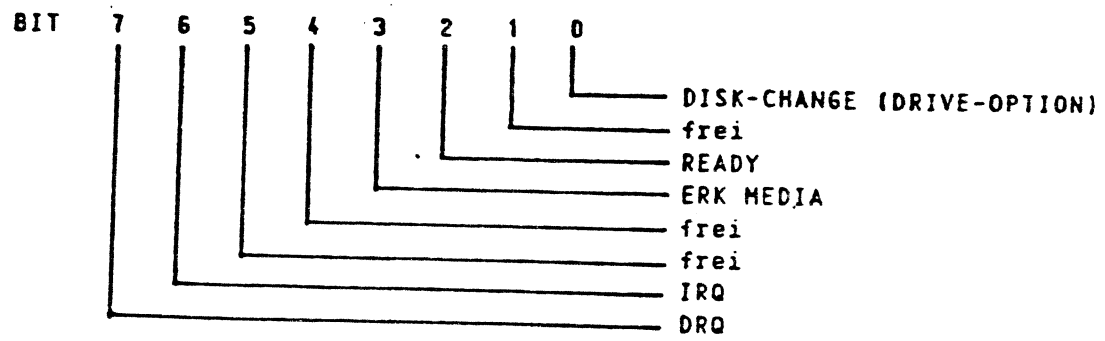
Kartenadresse: 50_H - 55_H

ADR.	50	READ Statusregister	
	50	WRITE Commandregister	
	51	Spurregister	1797
	52	Sektorregister	
	53	Dataregister	

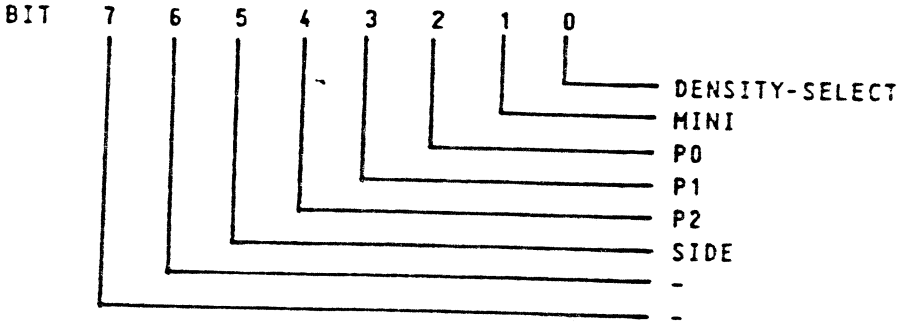
ADR. 54 WRITE



ADR. 54 READ



ADR. 55 WRITE



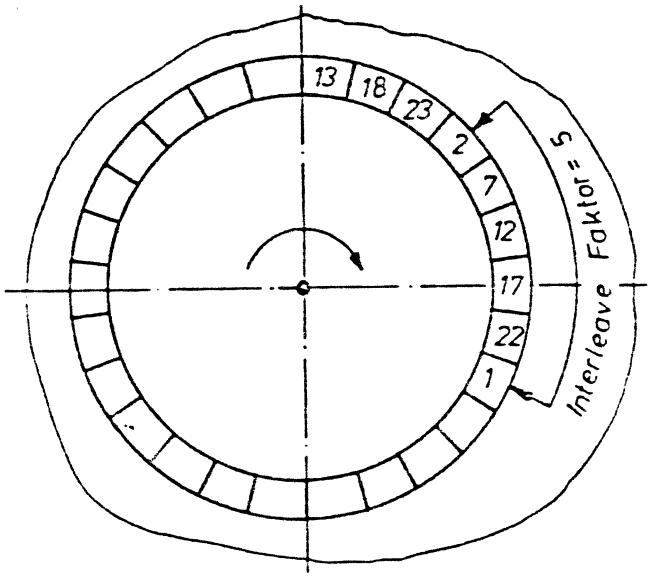
Das DRQ-Signal kann über IN 54_H auf Bit 7 vom Prozessor gepollt werden.

Nominal-Zeiten für Daten-Transfer eines Bytes

		Nominal	Worst Case 1797
5,25"	SINGLE	64 µs	47 µs
5,25"	DOUBLE	32 µs	23 µs
8"	SINGLE	32 µs	23 µs
8"	DOUBLE	16 µs	11,5 µs

6. Appendix

6.1 Sektor Interleaving

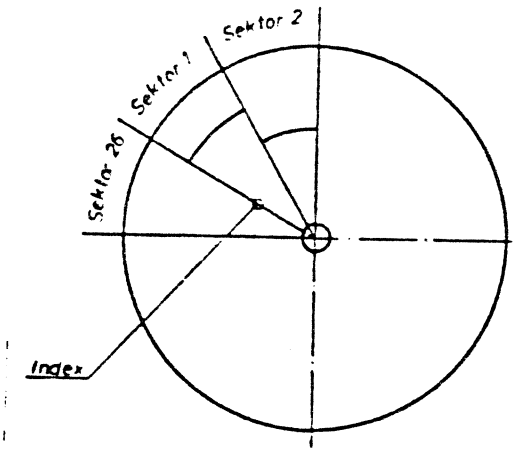


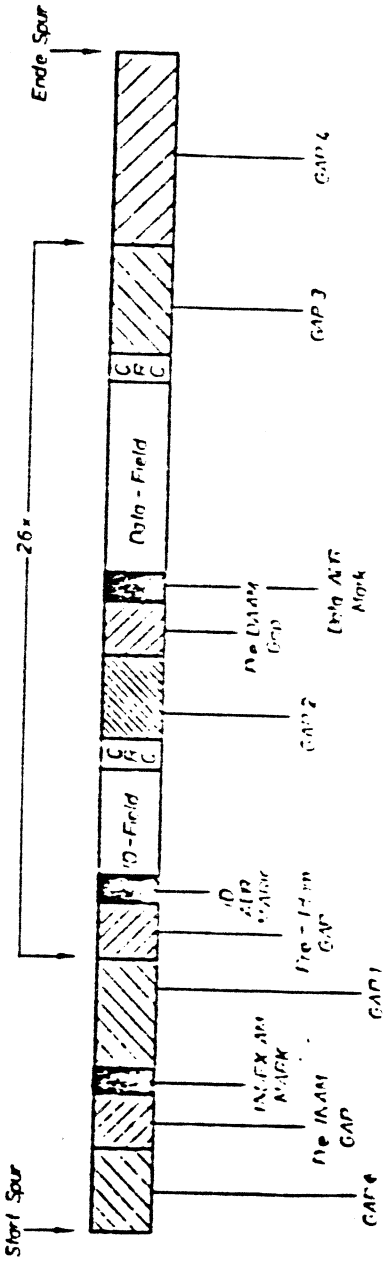
Das Formatieren einer Diskette ist ein pro Spur sequentiell ablaufender Vorgang. Ein Interleavefaktor von 1 formatiert dann in der Reihenfolge Sektor 1, 2, 3 ... 26. Ist der Prozessor nicht in der Lage, Daten zweier aufeinanderfolgender Sektoren zu verarbeiten, so entstehen Wartezeiten von z. B. 166 ms, da der Prozessor eine volle Umdrehung der Diskette abwarten muss um auf den Folgesektor zugreifen zu können. Ein Interleavefaktor von zwei kann den Zugriff während einer Umdrehung ermöglichen und so diese Zeit auf 6,4 ms reduzieren. Der für einen schnellstmöglichen Zugriff zu wählende Interleavefaktor muß anhand der Prozessorzeit errechnet werden.

6.2 Formattieren einer Diskette

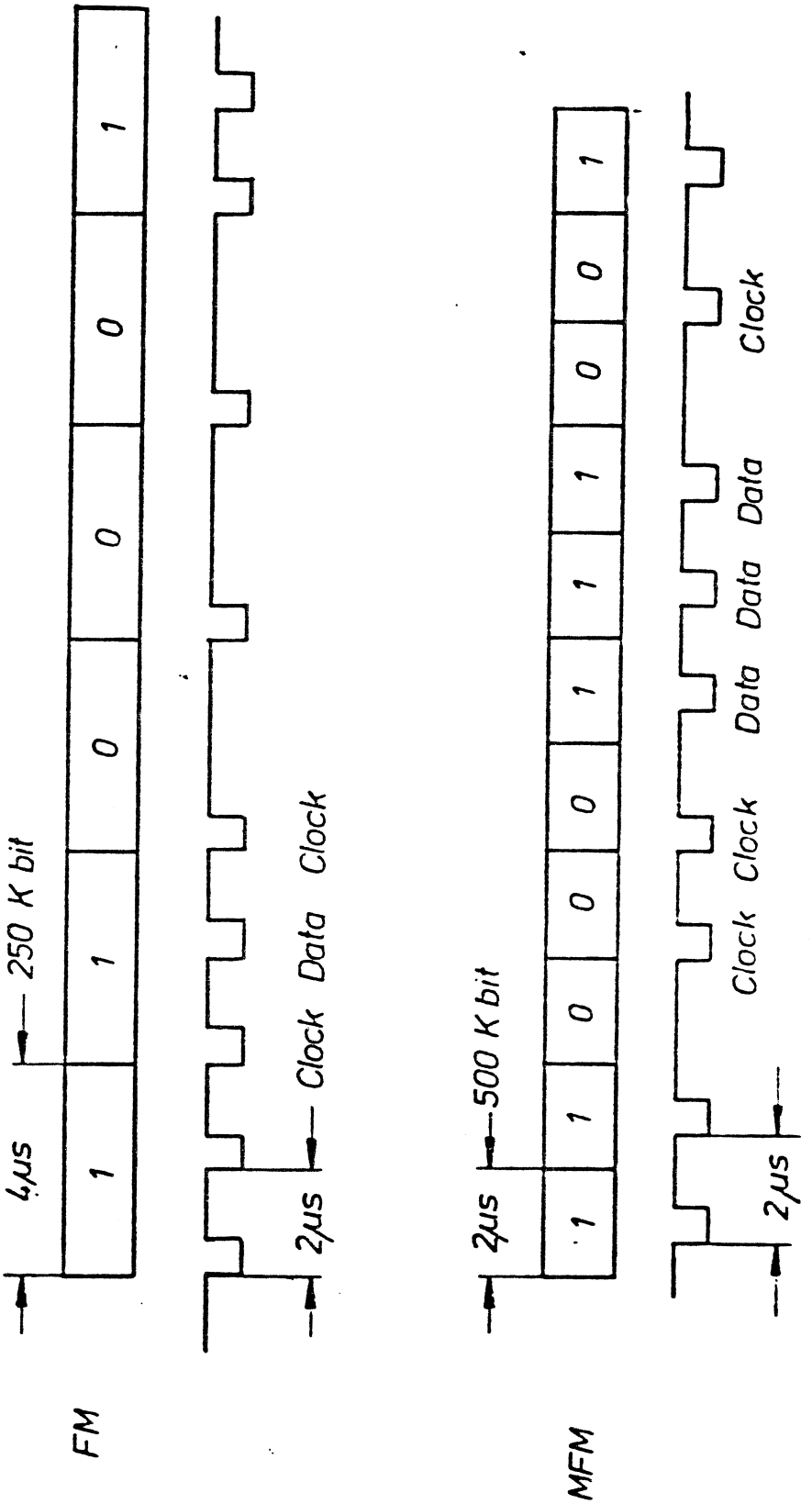
IBM 3740

GAP Ø	40 Bytes ØØ/FF
Pre - INAM	6 Bytes ØØ
Index AM	FC
CAP 1	26 Bytes ØØ/FF
Pre - IDAM	6 Bytes ØØ
ID - AM	FE
ID - Feld	6 Bytes
GAP 2	11 Bytes ØØ/FF
Pre - DAAM	6 Bytes ØØ
Data - AM	FB
Data - Field	128 Bytes
CAP 3	27 Bytes ØØ/FF
CAP 4	250 Bytes ØØ/FF





6.3 Schreibverfahren



WESTERN DIGITAL
CORPORATION

FD179X-02
FLOPPY DISK FORMATTER/CONTROLLER FAMILY

AUGUST, 1981

FEATURES

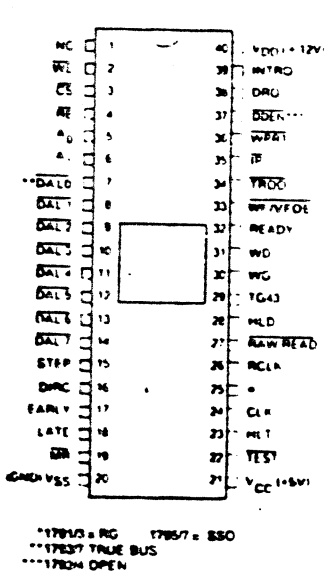
- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1792	1793	1794	1795	1797
Single Density (FM)	X	X	X	X	X	X
Double Density (MFM)	X		X		X	X
True Data Bus			X	X		X
Inverted Data Bus	X	X			X	
Write Precomp	X	X	X	X	X	X
Side Selection Output					X	X

APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTPOLLER/FORMATTER



*1793/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS
***1793/4 OPEN

PIN CONNECTIONS

FD179X SYSTEM BLOCK DIAGRAM

ITT-MName			ITT-MName		Bezeichnung:	Blatt Nr.	Ver.
Autor			Bearb.		Media Controller	10	37
Gepr.			Doku.		Unterlagen Nr.: MC 80 - 96	Referenz Baugruppe:	

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ± 5%
40		V_{DD}	+12V ± 5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control.
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit Bidirectional bus used for transfer of data, control and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference. 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for mini-floppies.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.

$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to + 5V or left open by the user unless interfacing to voice coil actuated steppers.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.
25	READ GATE (1791, 1792, 1793, 1794)	RG	This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read/Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ / $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
35	INDEX PULSE	IP	This input informs the FD179X when the index hole is encountered on the diskette
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected. This line must be left open on the 1792/4.

GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1795 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input ($\overline{RAW\ READ}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL but not loaded from the DAL.

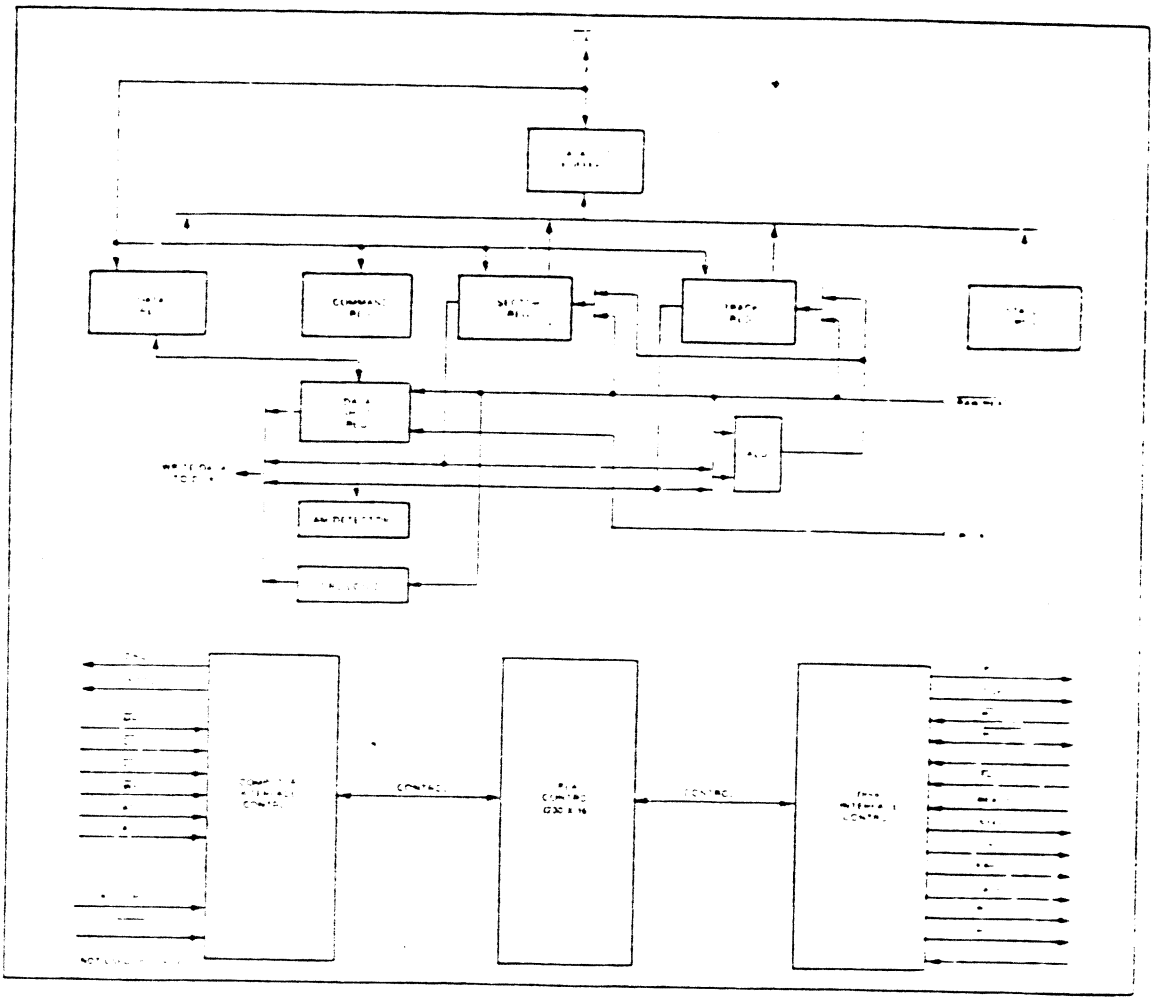
CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single



FD179X BLOCK DIAGRAM

density (FM) is assumed. 1792 & 1794 are single density only.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data

Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1". For MFM formats, $\overline{DDEN}$ should be placed to a logical "0". Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track, or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations in 8" double density the FD179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes, otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 200 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual values is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A Commands for Models 1791, 1792, 1793, 1794

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	I_1	I_3	I_2	I_1	I_0

B Commands for Models 1795, 1797

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Load head at beginning h = 1, Unload head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No 15 MS delay E = 1, 15 MS delay
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	

	LSB's Sector Length in ID Field: 00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_1 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE See Type IV Command Description for further information

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r0 r1), which determines the stepping motor rate as defined in Table 3.

A 2 µs (MFM) or 4 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 µs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	x	x
r1 r0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	164 µs	368 µs
0 1	6 ms	6 ms	12 ms	12 ms	190 µs	380 µs
1 0	10 ms	10 ms	20 ms	20 ms	198 µs	396 µs
1 1	15 ms	15 ms	30 ms	30 ms	208 µs	416 µs

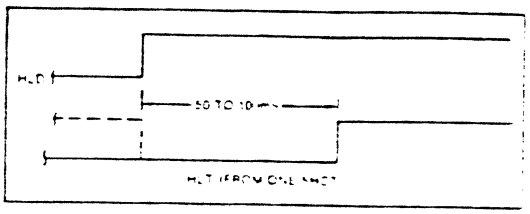
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond setting time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0), or if the FD179X is in an idle state (non busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

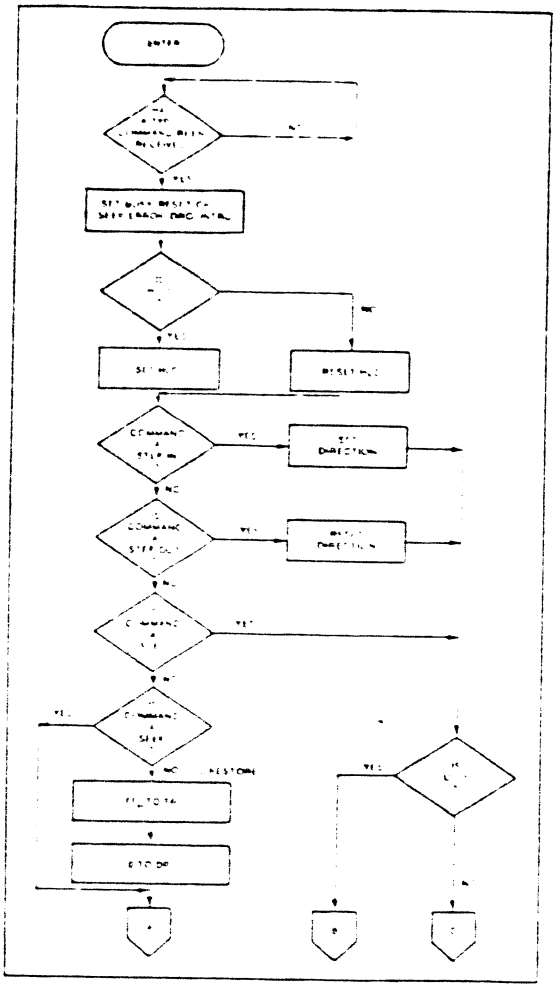
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

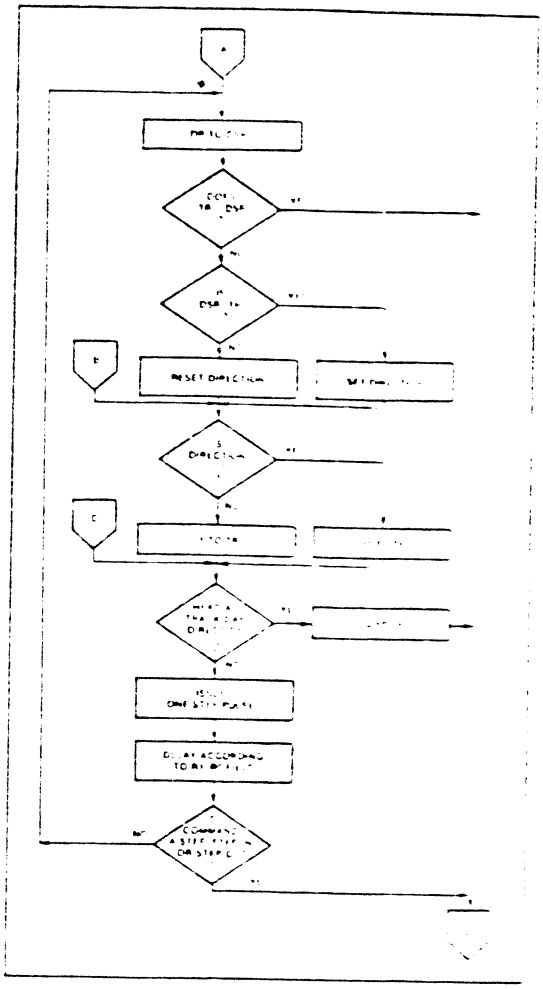
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1 r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state and that the DRQ pin stays low.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

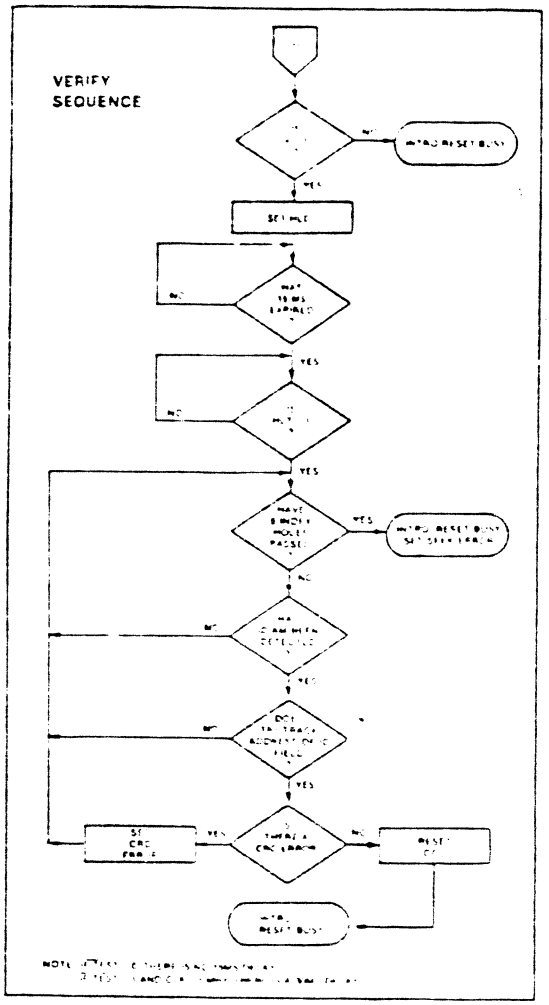
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

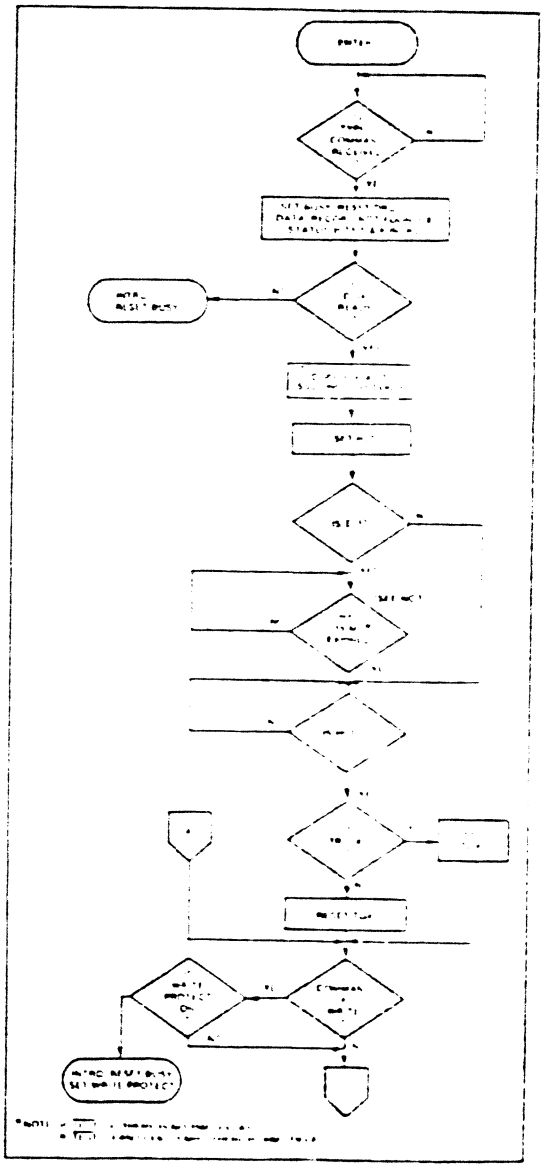


TYPE I COMMAND FLOW

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk, otherwise the Record not found status bit is set (Status Bit 3) and the command is terminated with an interrupt.



TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0 a single sector is read or written and an interrupt is generated at the

completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

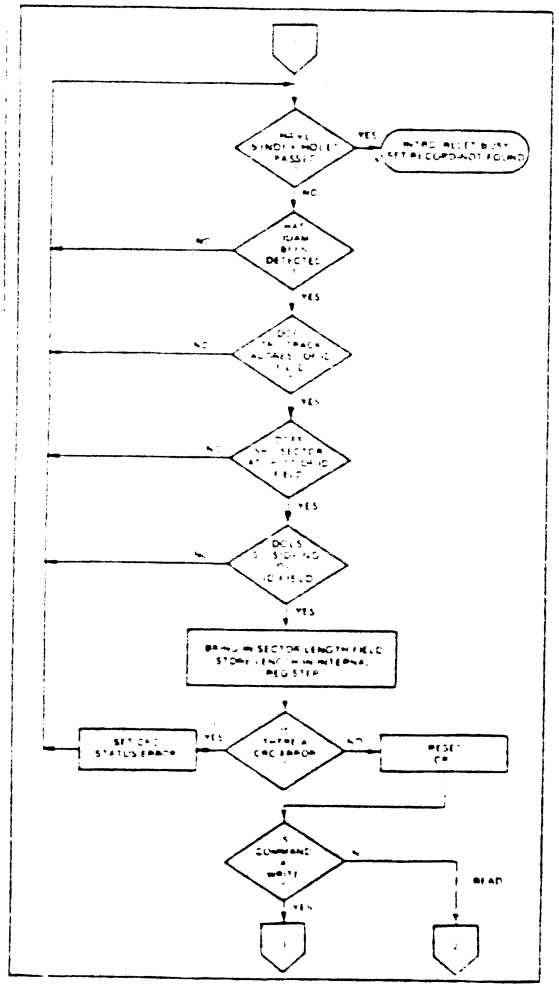
The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record Not-Found status bit is set.

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

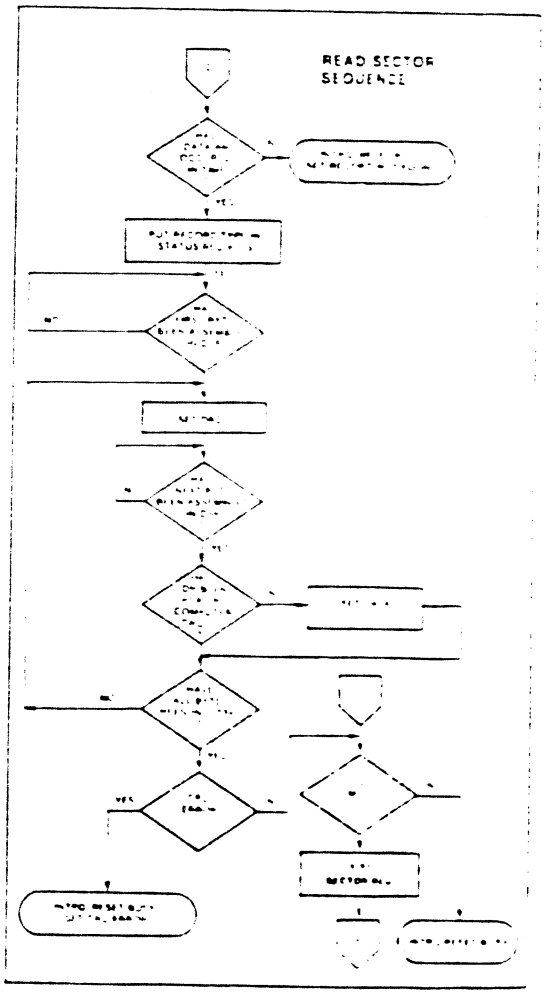
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address

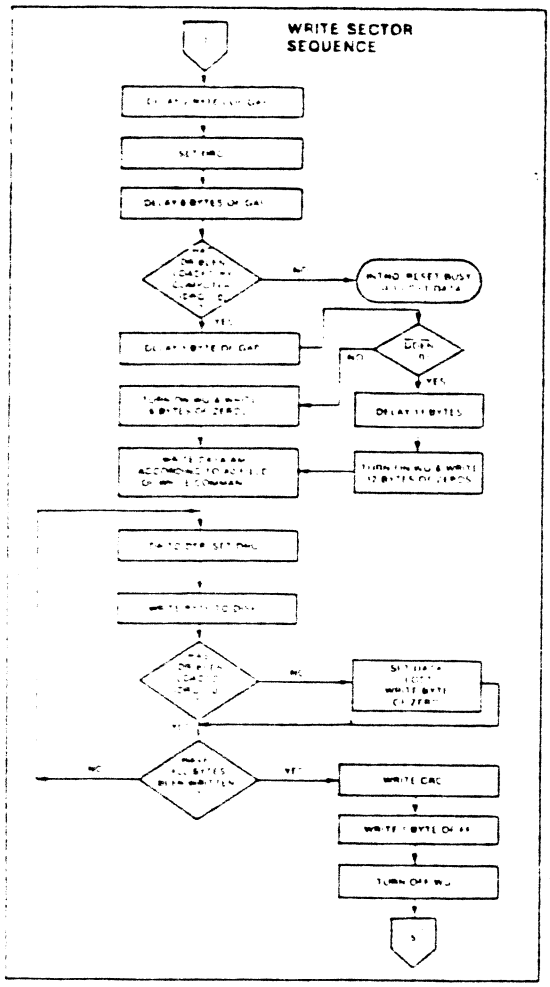


TYPE II COMMAND



TYPE II COMMAND

	IT.NR.	Name		IT.NR.	Name	Bezeichnung:	BLATT Nr.	VON
Autor			Bearb			Media Controller	20	37
Gepr			Doku			Unterlagen Nr.: MC 80 - 96	Referenz Baugruppe	



TYPE II COMMAND

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte, if not the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown :

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

a0	Data Address Mark (Bit 0
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ s to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC bytes.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below.

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

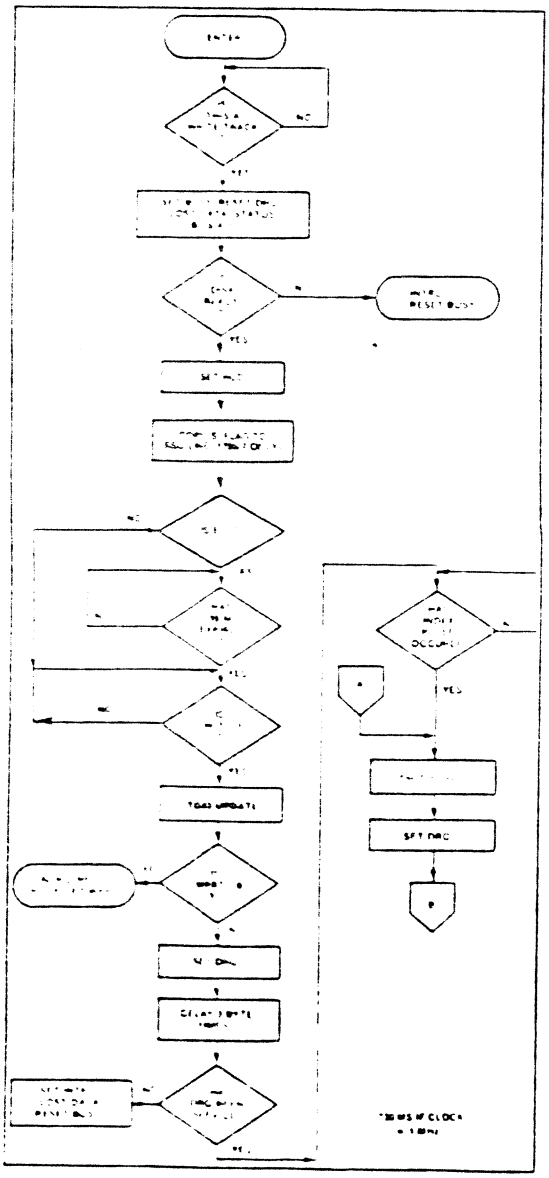
Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

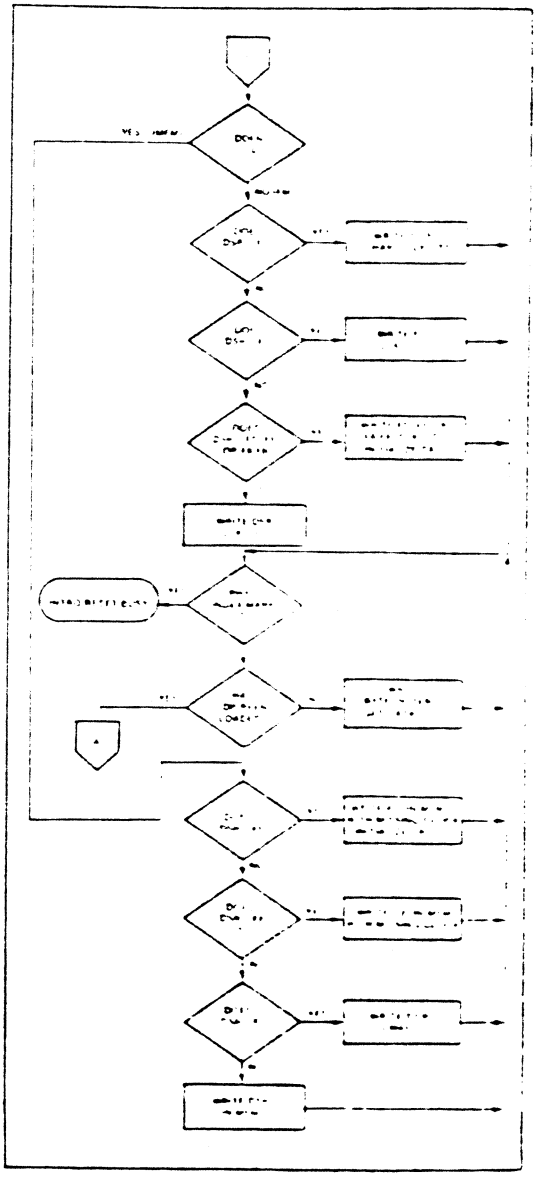
Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed, gap information is included in the data stream, the internal side compare is not performed, and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5 **Missing clock transition between bits 3 & 4

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

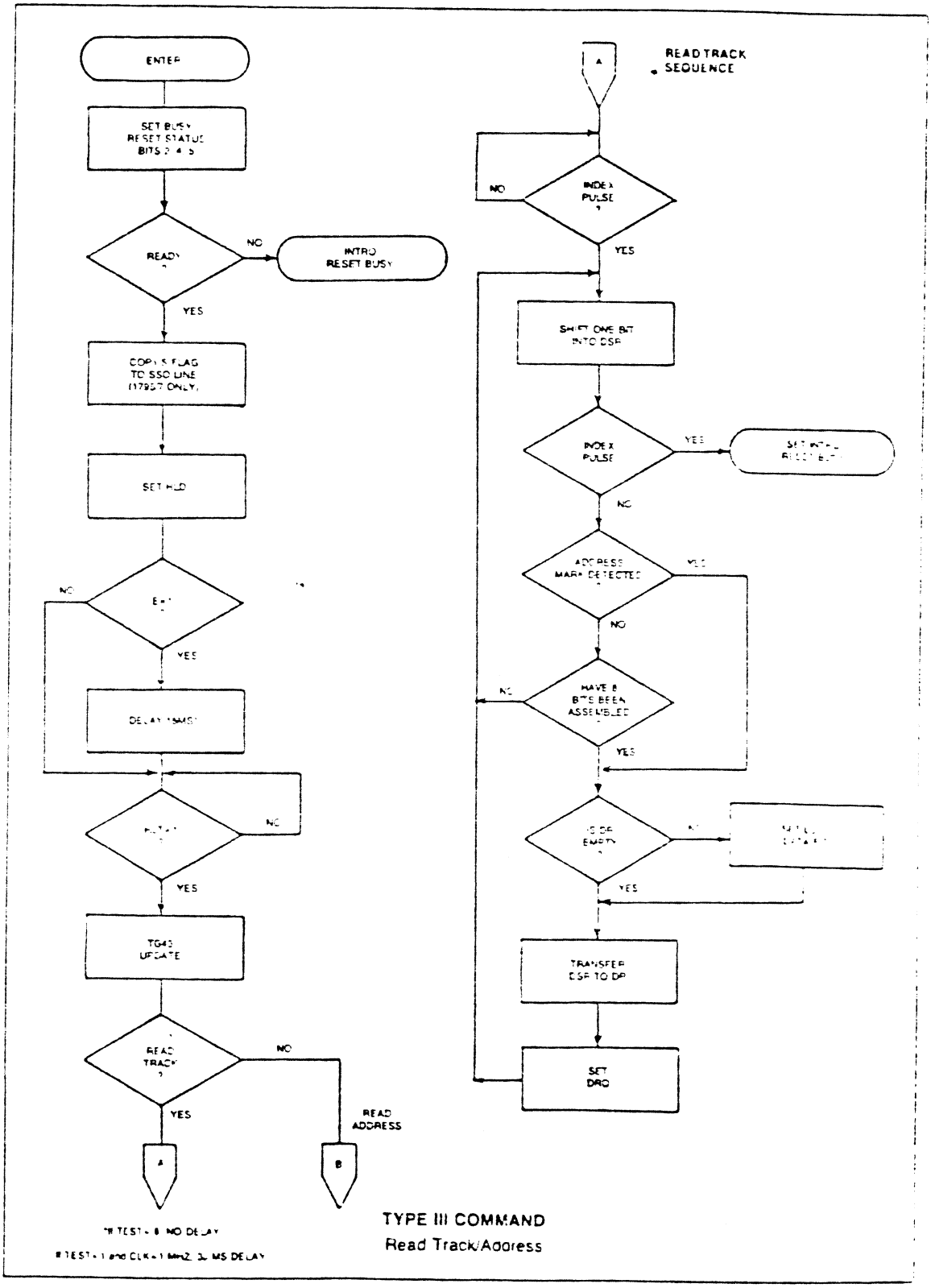
I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0) no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

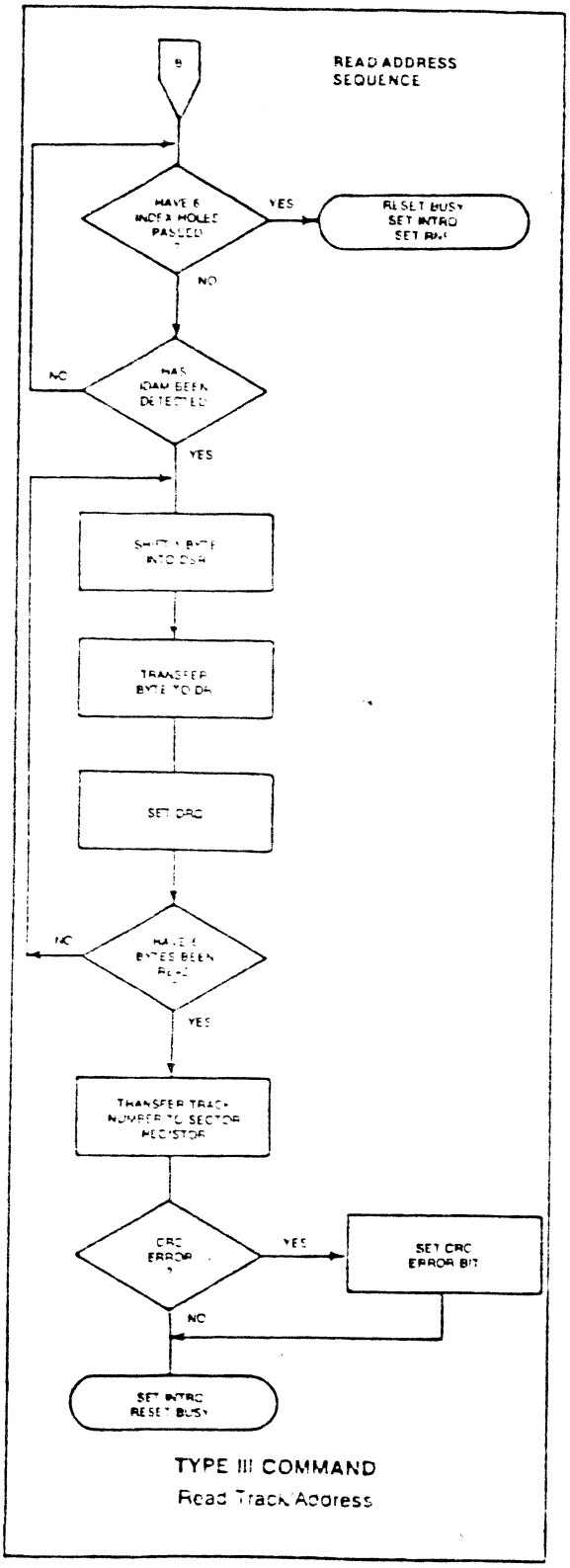
Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



	ITT-Name			ITT-Name		Bezeichnung	Blatt Nr.	Von
Autor			Bearb			Media Controller	24	37
Gepr			Doku			Unterlagen Nr.: MC 80 - 96	Referenz Baugruppe	



TYPE III COMMAND

Read Track Address

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete in lieu of using the INTRQ line. When using the INTRQ a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

BITS							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under program control. These are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd FM	Delay Req'd MFM
Write to Command Reg	Read Busy Bit (Status Bit 0)	12 µs	6 µs
Write to Command Reg	Read Status Bits 1-7	28 µs	14 µs
Write Any Register	Read From Diff Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FC (Index Mark)
* 26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247**	FF (or 00)

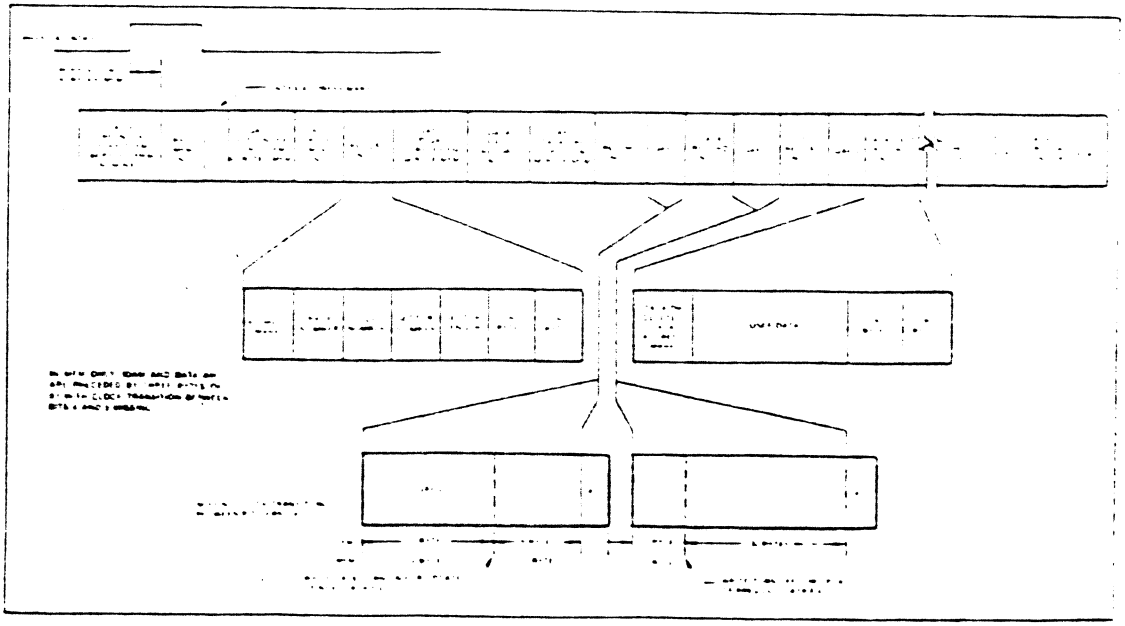
*Write bracketed field 26 times
**Continue writing until FD179X interrupts out.
Approx. 247 bytes
1-Optional '00' on 1795/7 only.

IBM SYSTEM 34 FORMAT-
256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

*Write bracketed field 26 times
**Continue writing until FD179X interrupts out.
Approx. 598 bytes.



IBM TRACK FORMAT

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 or 1024 bytes.

2) Gap 2 cannot be varied from the IBM format.

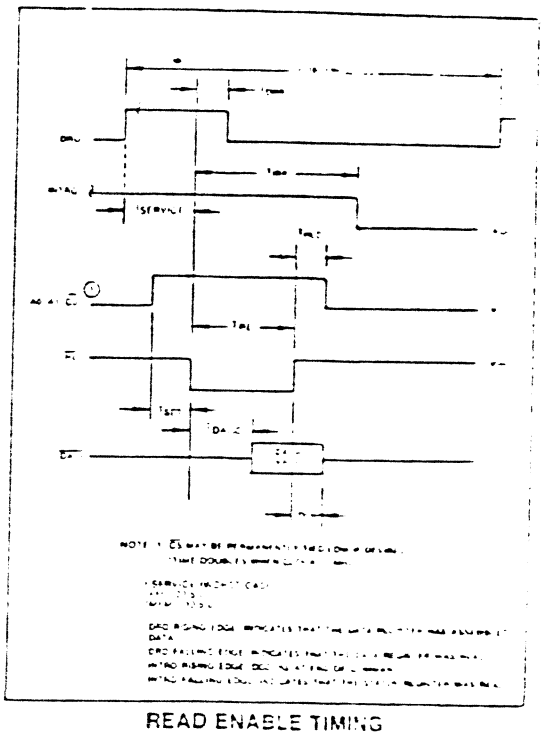
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



READ ENABLE TIMING

TIMING CHARACTERISTICS

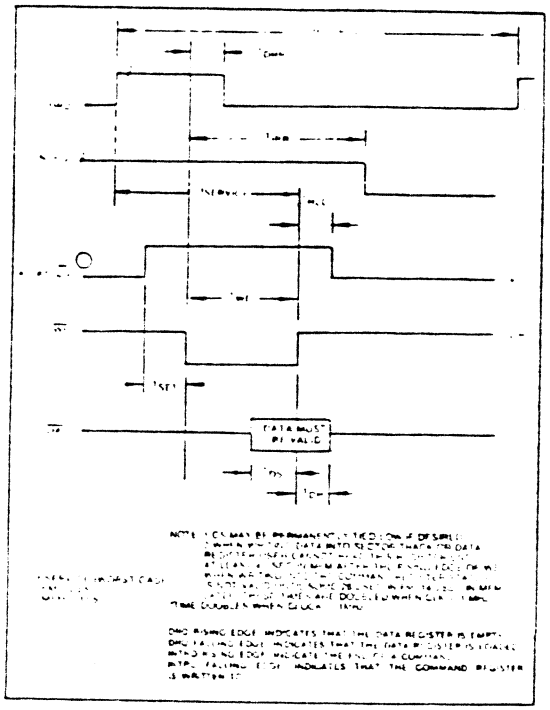
T_A = 0°C to 70°C, V_{BB} = +12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING (See Note 6, Page 21)

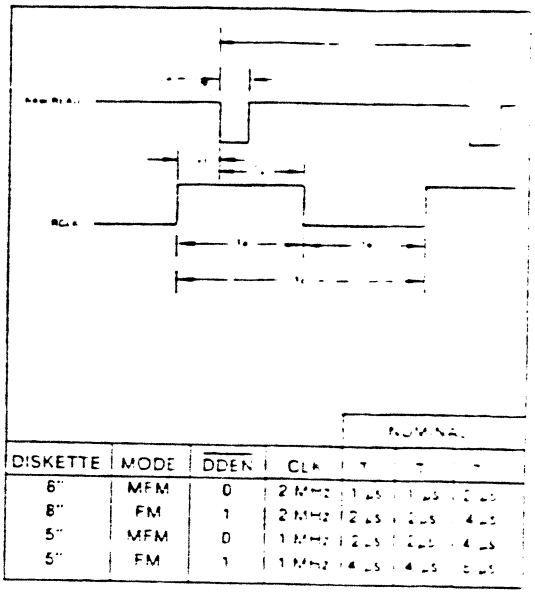
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$				nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf

WRITE ENABLE TIMING (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	



WRITE ENABLE TIMING



DISKETTE	MODE	DDEN	CLK	T	T	T
8"	MFM	0	2 MHz	1 µs	1 µs	2 µs
8"	FM	1	2 MHz	2 µs	2 µs	4 µs
5"	MFM	0	1 MHz	2 µs	2 µs	4 µs
5"	FM	1	1 MHz	4 µs	4 µs	8 µs

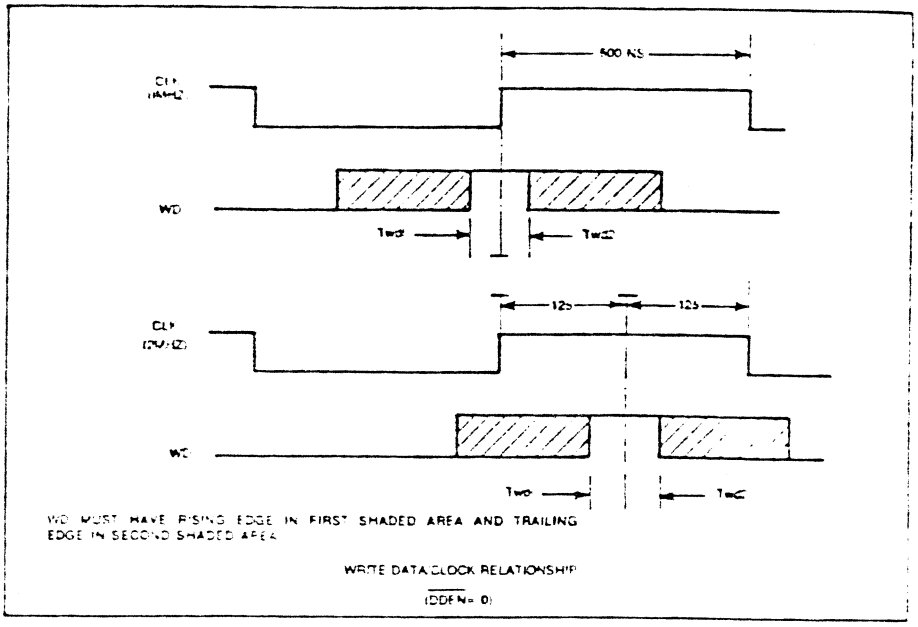
INPUT DATA TIMING

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time	1500	2000		nsec	1800 ns @ 70°C
Tx1	RCLK hold to $\overline{\text{Raw Read}}$	40			nsec	See Note 1
Tx2	$\overline{\text{Raw Read}}$ hold to RCLK	40			nsec	See Note 1

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (See Note 6, Page 21)

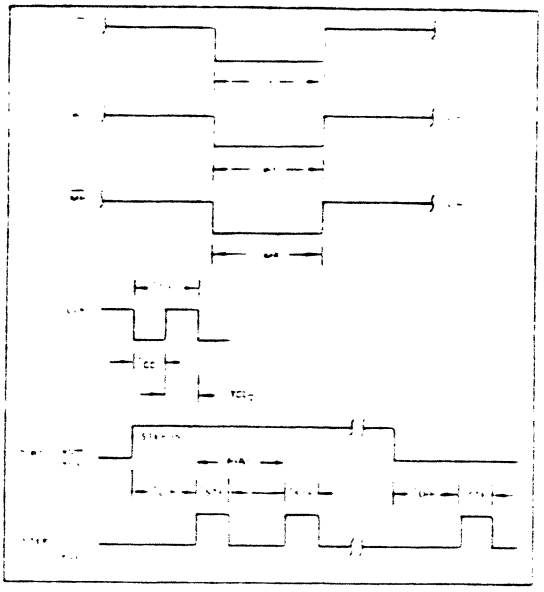
SYMBOL	CHARACTERISTICS	MIN	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Twg	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
Tbc	Write data cycle Time		2,3, or 4		µsec	± CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM
Twd1	WD Valid to Clk	100			nsec	CLK = 1 MHz
		50			nsec	CLK = 2 MHz
Twd2	WD Valid after CLK	100			nsec	CLK = 1 MHz
		30			nsec	CLK = 2 MHz



WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX.	UNITS	CONDITIONS
TCD$_L$	Clock Duty (low)	230	250	20000	nsec	
TCD$_H$	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			µsec	See Note 6
TDIR	Dir Setup to Step		12		µsec	= CLK ERROR
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	See Note 6
TWF	Write Fault Pulse Width	10			µsec	



MISCELLANEOUS TIMING

*FROM STEP RATE TABLE

NOTES:
1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 µs. nominal in MFM and 4 µs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at V_{OL} = 0.6v and V_{OH} = 2.0v.

Table 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically ored with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical and of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: it indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{DD} with repect to V_{SS} (ground): + 15 to − 0.3V

Voltage to any input with respect to V_{SS} = + 15 to − 0.3V

I_{DD} = 60 MA (35 MA nominal)

I_{CC} = 15 MA (10 MA nominal)

Dissipation = 0.6 W

C_{IN} & C_{OUT} = 15 pF max with all pins grounded except one under test.

Operating temperature = 0°C to 70°C

Storage temperature = − 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	µA	$V_{IN} = V_{DD}$ **
I_{OL}	Output Leakage		10	µA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = − 100 µA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.6 mA*
P_D	Power Dissipation		0.6	W	

*1792 and 1794 I_O = 1.0 mA

**Leakage conditions are for input pins without internal pull-up resistors.

STANDARD MICROSYSTEMS CORPORATION

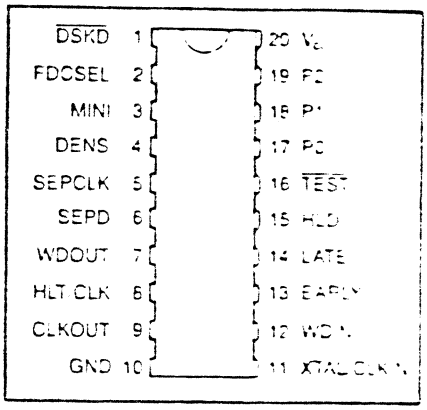
FDC 9229
FDC 9229B

FLOPPY DISK INTERFACE CIRCUIT

FEATURES

- Digital Data Separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 5¼" and 8" compatible
- Variable Write Precompensation
- Internal Crystal Oscillator Circuit
- Track-Selectable Write Precompensation
- Retriggerable Head-Load Timer
- Compatible with the FDC 179X, 765, and other standard Floppy Disk Controllers
- COPLAMOS® n-channel MOS Technology
- Single +5 Volt Supply
- TTL Compatible

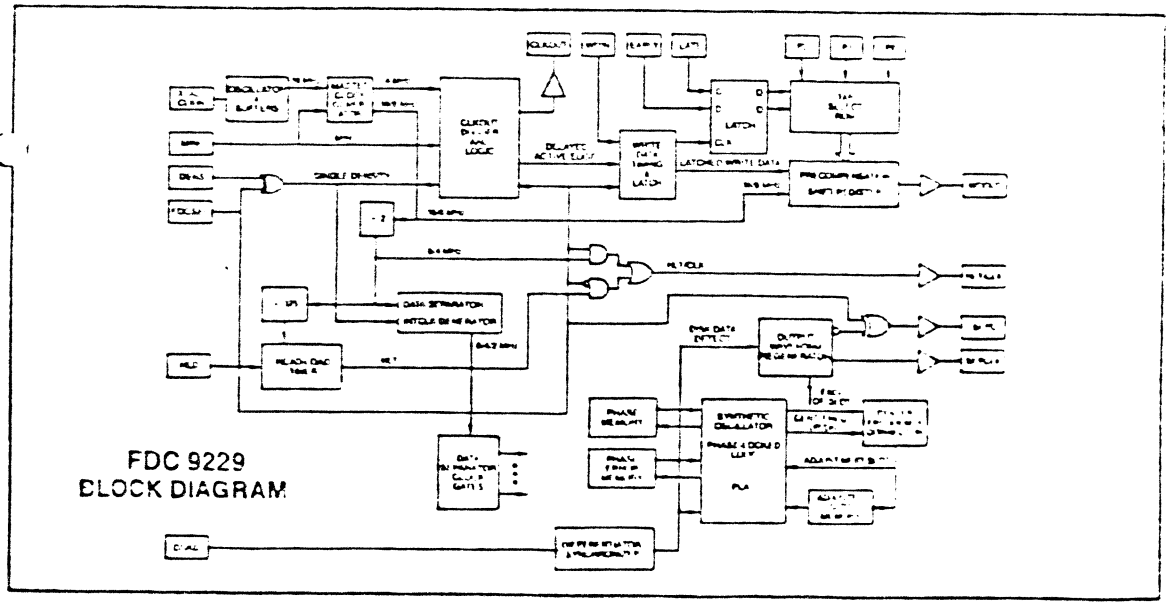
PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The FDC 9229 B is an MOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 9229 B provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 9229 B operates from a +5V supply and simply requires that a 16 or 8 MHz crystal or TTL-level clock be connected to the XTAL CLKIN pin. All inputs and outputs are TTL compatible.

The FDC 9229 is available in two versions: the FDC 9229 which is intended for 5¼" disks and the FDC 9229 B for 5¼" and 8" disks.



FDC 9229
BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO	SYMBOL	I/O	DESCRIPTION
1	$\overline{DSKD}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low, programs the FDC 9229 B for a 179X type of LSI controller. When FDCSEL is high, the FDC 9229 B is programmed for a 765 (8272) type of controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the FDC 9229 B is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT CLK frequency (when in 765 mode). (See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the FDC 9229 B is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the DSKD input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input (DSKD). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT CLK	O	When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	XTAL CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz crystal. (The other pin of the crystal is grounded, and a 470K resistor is connected across the crystal.) XTAL CLKIN may alternatively be connected to a single-phase TTL-level clock.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written early to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.)
16	$\overline{TEST}$	I	This input (when low) decreases the head-load time delay and initializes the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{cc}		+ 5 VOLT SUPPLY

OPERATION

Data Separator

The XTAL/CLKIN input clock is internally divided by the FDC 9229 B to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

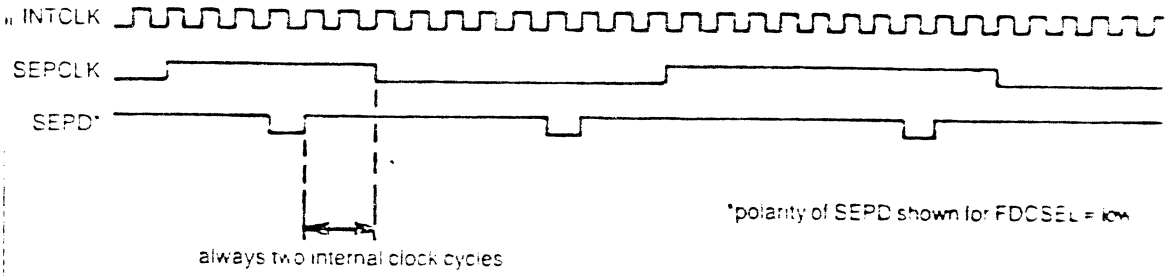
The FDC 9229 B detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

INPUTS			DIVISOR
FDCSEL	DENS	MINI	f(XTAL/CLKIN)/f(INTCLK)
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4

FIG. 1



Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 9229 B as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	PRECOMP VALUE
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION

OPERATION (CONT'D)

Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 9229/B goes high before starting a read or write operation.

INPUTS			OUTPUTS	
FDCSEL	DENS	MINI	CLKOUT	HLT.CLK
0	0	0	2 MHz	40 ms*
0	0	1	1 MHz	80 ms*
0	1	0	2 MHz	40 ms*
0	1	1	1 MHz	80 ms*
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

*May be mask programmed at factory to any value from 1 to 512 ms in 15.625 µs increments (MINI low) or 1 to 1024 ms in 31.25 µs increments (MINI high).

FIG. 3 CLOCK AND HEAD LOAD TIME DELAY SELECTION

INPUTS			FLOPPY DISK DRIVE TYPE	FLOPPY DISK DRIVE DENSITY	FLOPPY DISK CONTROLLER TYPE
FDCSEL	DENS	MINI			
0	0	0	8" DRIVE	DOUBLE	179X
0	0	1	5¼" DRIVE	DOUBLE	179X
0	1	0	8" DRIVE	SINGLE	179X
0	1	1	5¼" DRIVE	SINGLE	179X
1	0	0	8" DRIVE	SINGLE	765/82C72
1	0	1	5¼" DRIVE	SINGLE	765/82C72
1	1	0	8" DRIVE	DOUBLE	765/82C72
1	1	1	5¼" DRIVE	DOUBLE	765/82C72

FIG. 4 FLOPPY DISK DRIVE AND CONTROLLER SELECTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	- 55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 300°C
Positive Voltage on any I/O Pin, with respect to ground	+ 6.0V
Negative Voltage on any I/O Pin, with respect to ground	- 0.3V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low Level V_{IL}	- 0.3		0.8	V	Except XTAL CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
XTAL CLKIN INPUT VOLTAGE					
AC Amplitude	1.0			V_{pp}	XTAL CLKIN or ... must be AC-coupled
Instantaneous voltage	- 0.3		(V_{CC})	V	
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT CLK I_{OL} = 0.4 mA HLT CLK only
High Level V_{OH}	2.4			V	I_{OH} = - 100 µA except HLT CLK I_{OH} = - 400 µA HLT CLK only
POWER SUPPLY CURRENT					
I_{CC}			100	mA	
INPUT LEAKAGE CURRENT					
I_{LI}			10	µA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE			10	pF	Except CLKIN
C_{IN}			25	pF	CLKIN only

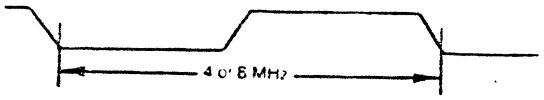
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
AC ELECTRICAL CHARACTERISTICS	(All times assume XTAL/CLKIN = 16 MHz unless otherwise specified)				
XTAL CLKIN frequency	3.95	16	16.2	MHz	FDC 9229B
	3.95	8	8.1	MHz	FDC 9229
XTAL CLKIN DUTY CYCLE	25		75	%	
t_{CLCL}	465	500	515	ns	FDCSEL = low, MINI = high
	215	250	265	ns	FDCSEL = low, MINI = low
	90	125	140	ns	FDCSEL = high
t_{CHCL}	280	312.5	350	ns	
t_{CLCH}	50		400	ns	
t_{CHCH}	0		400	ns	
t_{WLWH}		562.5		ns	
t_{WLWH}		precomp value			See fig. 2
t_{WLWH}		2 x precomp value			See fig. 2
t_{RR}	1.0			µs	

	ITT/VM Name		ITT/VM Name		Bezeichnung	Blatt Nr.	von
Autor			Sachb.		Media Controller	36	37
Gepr.			Doku		Unterlagen Nr. MC 80 - 96	Referenz Baugruppe	

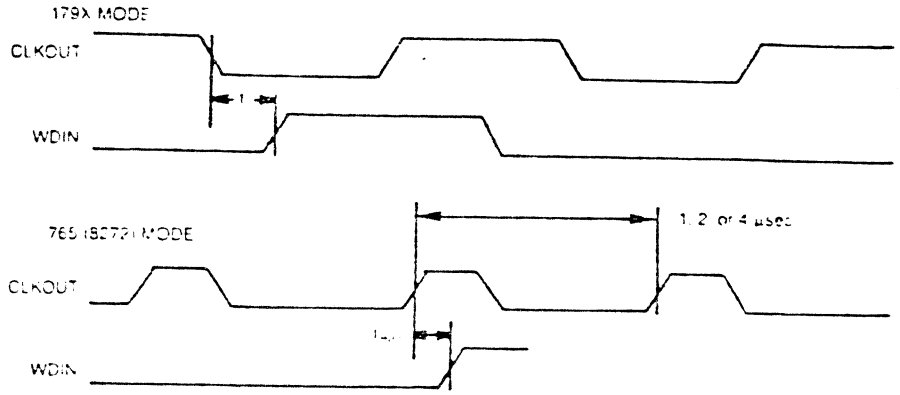
AC TIMING CHARACTERISTICS

HLT CLK (765 MODE)

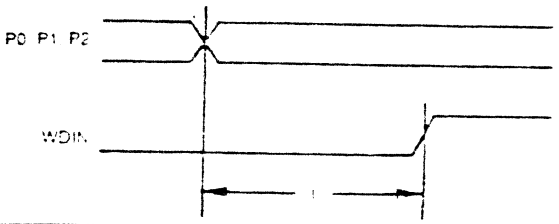


WDOUT PULSE WIDTH

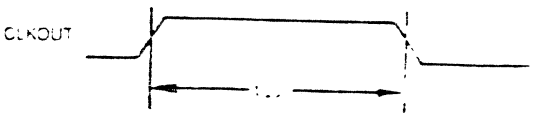
CLKOUT VS. WDIN TIMING

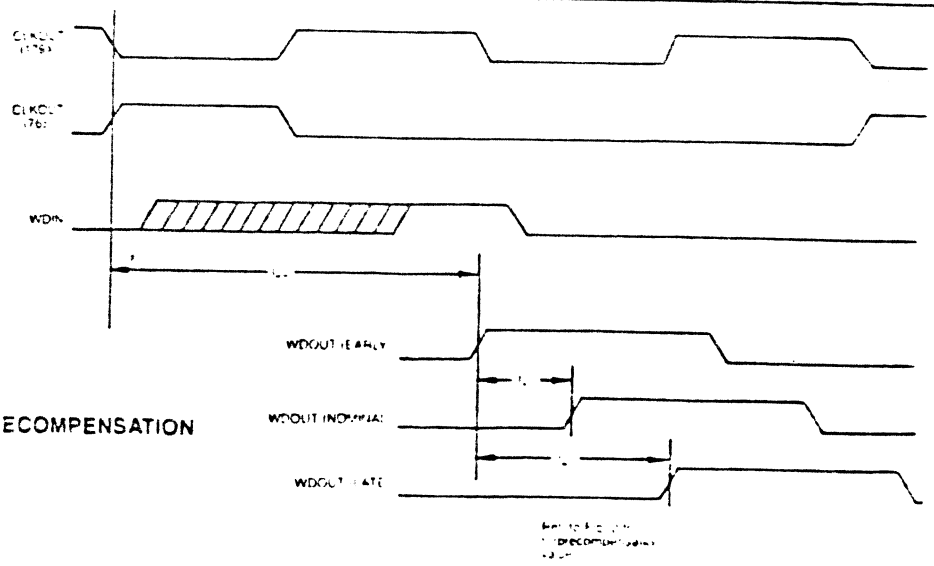


SET-UP TIME P0, P1 AND P2 TO WDIN



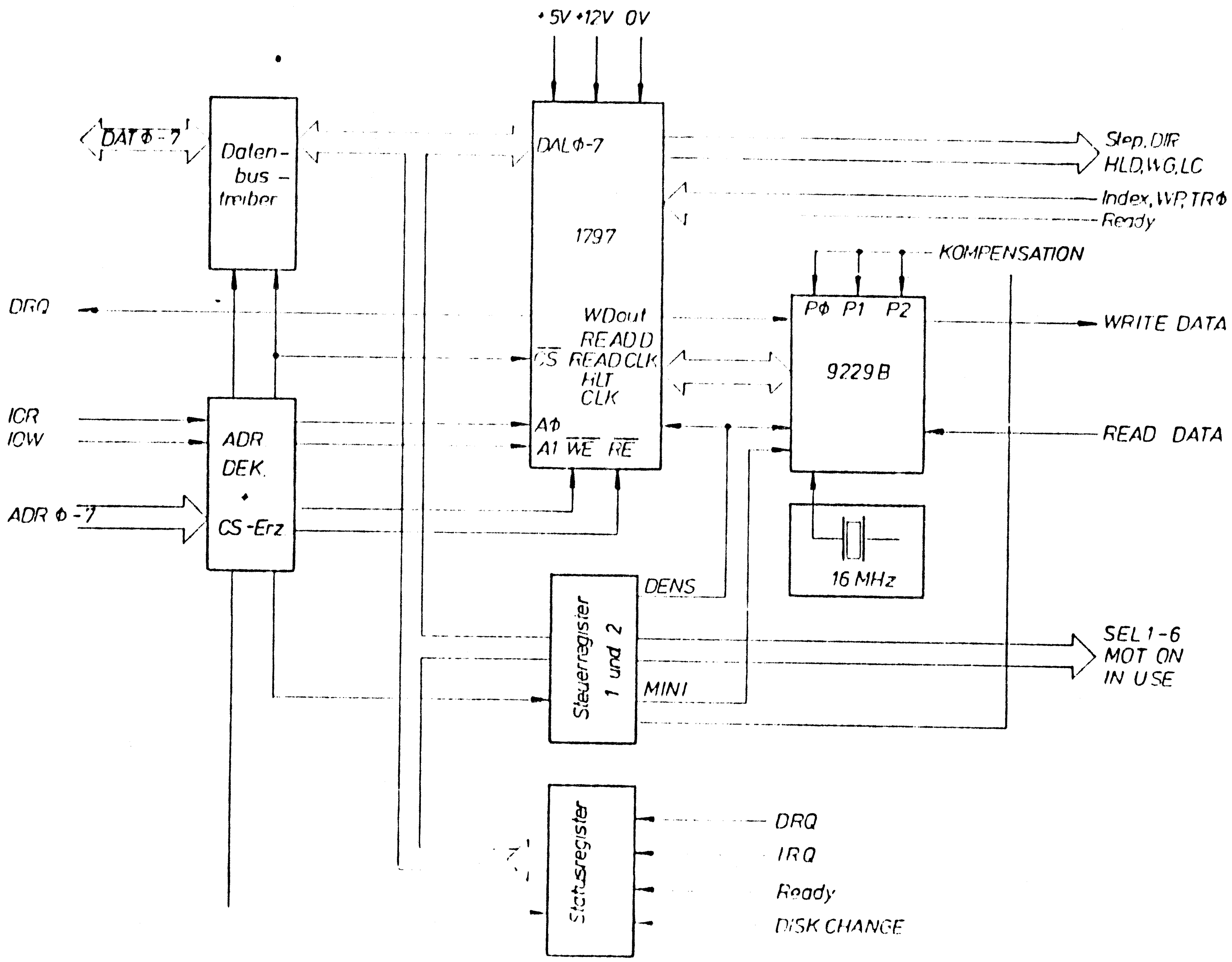
CLKOUT





PRECOMPENSATION

	FTAM Name			FTAM Name		Bezeichnung:	Blatt Nr.	Ver
Autor			Sachb			Media Controller	37	37
Gepr			Doku			Unterlagen Nr.: MC 80 - 96	Referenz Baugruppe	



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