Supertex inc.

Leadership in CMOS/DMOS Technologies

DATABOOK 1988-1989

1225 Bordeaux Drive • Sunnyvale, California 94088-3607

Preliminary

Microprocessor Supervisory Circuits

Ordering Information

Device	Temperature Range	Package	Order No.
MP690	0°C to + 70°C	8 Lead Plastic Dip	MP690P
	-40°C to + 85°C	8 Lead Plastic Dip	MP690 MP
	-40°C to + 85°C	8 Lead CERDIP	MP690MD
	-55°C to + 125°C	8 Lead CERDIP	RCMP690D
	-55°C to + 125°C	8 Lead CERDIP HI-REL	RBMP 690D
MP691	0°C to + 70°C	Dice	MP691X
	0°C to + 70°C	16 Lead Plastic DIP	MP691P
	0°C to + 70°C	16 Lead Small Outline	MP691WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP691MP
	-40°C to + 85°C	16 Lead CERDIP	MP691MD
	-40°C to + 85°C	16 Lead Small Outline	MP691MWG
	-55°C to + 125°C	16 Lead CERDIP	RCMP691D
	-55°C to + 125°C	16 Lead CERDIP HI-REL	RBMP691D
MP692	0°C to + 70°C	8 Lead Plastic DIP	MP692P
	-40°C to + 85°C	8 Lead Plastic DIP	MP692MP
	-40°C to + 85°C	8 Lead CERDIP	MP692MD
	-55°C to + 125°C	8 Lead CERDIP	RCMP 692D
	-55°C to + 125°C	8 Lead CERDIP HI-REL	RBMP692D
MP693	0°C to + 70°C	Dice	MP693X
	0°C to + 70°C	16 Lead Plastic DIP	MP693P
	0°C to + 70°C	16 Lead Small Outline	MP693WG
	-40°C to + 85°C	16 Lead Plastic DIP	MP693MP
	-40°C to + 85°C	16 Lead CERDIP	MP693MD
	-40°C to + 85°C	16 Lead Small Outline	MP693MWG
	-55°C to + 125°C	16 Lead CERDIP	RCMP693 D
	-55°C to + 125°C	16 Lead CERDIP HI-REL	RBMP693 D

Features

- ☐ Precision Voltage Monitor:
  4.65V in MP690 and MP691
  4.40V in MP692 and MP693
- ☐ Power OK/Reset Time Delay
- ☐ Watchdog Timer –100ms, 1.6 sec, or adjustable
- ☐ Minimum Component Count
- ☐ 1μA Standby Current
- ☐ Battery Backup Power Switching
- ☐ Onboard Gating of Chip Enable Signals
- ☐ Voltage Monitor for Power Fail or Low Battery Warning

General Description

The MP690 Family of supervisory circuits reduces the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems.

The MP690 and MP692 are supplied in 8-pin packages and provide four functions:

1) A Reset output during power-up, power down, and brownout conditions.
2) Battery backup switching for CMOS RAM, CMOS microprocessor other low power logic.
3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
4) A 1.25V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MP691 and MP693 are supplied in 16-pin packages and perform all MP690/692 functions, plus:

1) Write protection of CMOS RAM or EEPROM.
2) Adjustable reset and watchdog timeout periods.
3) Separate outputs for indicating a watchdog timeout, battery switchover, and low V_{CC}.

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
V_{BATT}	-0.3V to 6.0V
All other Inputs (Note 1)	-0.3V to (Vout +0.5V)
Input Current	
V_{CC}	200mA
V_{BATT}	50mA
GND	20mA
Output Current	
V_{OUT}	short circuit protected
All other Outputs	20mA
Rate-of-Rise, V_{BATT}, V_{CC}	100V/µs

Power Dissipation	
8 Pin Plastic DIP	
(Derate 5mW/°C above +70°C)	400mW
8 Pin CERDIP	
(Derate 8mW/°C above +85°C)	500mW
16 Pin Plastic DIP	
(Derate 7mW/°C above +70°C)	600mW
16 Pin Small Outline	
(Derate 7mW/°C above +70°C)	600mW
16 Pin CERDIP	
(Derate 10mW/°C above +85°C)	600mW
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1 and 2)

Parameter	Min	Typ	Max	Unit	Conditions
BATTERY BACKUP SWITCHING					
Operating Voltage Range					
MP690, 691 V_{CC}	4.75		5.5	V	
MP690, 691 V_{BATT}	2.0		4.25		
MP692, 693 V_{CC}	4.5		5.5		
MP692, 693 V_{BATT}	2.0		4.0		
V_{OUT} Output Voltage		V_{CC} - 0.1		V	I_{OUT} = 1mA
		V_{CC} - 0.25		V	I_{OUT} = 50mA
V_{OUT} in Battery Backup Mode	V_{BATT} - 0.1	V_{BATT} - 0.02		V	I_{OUT} = 100µA, V_{CC}< V_{BATT} - 0.2V
Supply Current (excludes I_{OUT})		4		mA	I_{OUT} = 1mA
		10		mA	I_{OUT} = 100mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0V, V_{BATT} = 2.8V
Battery Standby Charging Current			1	µA	5.5V > V_{CC} > V_{BATT} + 0.2V I_{OUT} = 1mA
			5	µA	5.5V > V_{CC} > V_{BATT} + 0.2V I_{OUT} = 100mA
Battery Switchover Threshold		70		mV	Power Up
V_{CC} - V_{BATT}		50		mA	Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.4	V	I_{SINK} = 3.2mA
BATT ON Output Short Circuit Current		7		mA	BATT ON = V_{OUT}
	0.5	1	25	µA	BATT ON = 0V
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	4.5	4.65	4.75	V	MP690, 691
	4.25	4.4	4.5	V	MP690, 691
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay	35	50	70	ms	Figure 6. OSC SEL High
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	sec	Long Period
	70	100	140	ms	Short Period
Watchdog Timeout Period, External Clock	4032		4097	Clock Cycles	Long Period
	960		1025		Short Period
Minimum WDI Input Pulse Width	200			ns	V_{IL} = 0.4, V_{IH} = 3.5V

Electrical Characteristics (continued)

(V_{CC} = full operating range; V_{BATT} = 2.8V; T_A = 25°C, unless otherwise noted.) (Notes 1 and 2)

Parameter		Min	Typ	Max	Unit	Conditions
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage				0.4	V	I_{SINK} = 1.6mA
		3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
RESET and $\overline{WDO}$ Output Voltage				0.4	V	I_{SINK} = 800µA
		3.5				I_{SOURCE} = 1µA, V_{CC} = 5V
Output Short Circuit Current		1	3	25	µA	$\overline{RESET}$, RESET, $\overline{WDO}$, $\overline{LOWLINE}$
WDI Input Threshold	Logic Low			0.8	V	V_{CC} = 5V (Note 2)
	Logic High	3.0				
WDI Mid-Level Logic Voltage		1.3	1.9	2.5	V	V_{CC} = 5V (Note 2)
WDI Input current			20		µA	WDI = V_{OUT}
			-15		µA	WDI = 0V

POWER FAIL DETECTOR

PFI Input Threshold	1.15	1.25	1.35	V	
PFI Input Current		±0.01	±10	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 3.2mA
			3.5	V	I_{SOURCE} = 1µA
$\overline{PFO}$ Short Circuit Source Current	1	3	25	µA	PFI = 0V, $\overline{PFO}$ = 0V

CHIP ENABLE GATING

$\overline{CE}$ IN Thresholds	0.8			V	V_{IL}
			3.0	V	V_{IH}
$\overline{CE}$ IN Pullup Current		3		µA	
$\overline{CE}$ OUT Output Voltage			0.4	V	I_{SINK} = 3.2mA
	V_{CC} -1.5			V	I_{SOURCE} = 3.0mA
$\overline{CE}$ Propagation Delay			50	ns	

OSCILLATOR

OSC IN Input Current		±2		µA	
OSC SEL Input Pullup Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0V
OSC IN Frequency with External Capacitor		2		kHz	OSC SEL = 0V, C_{OSC} = 47pF

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Caution - Battery Backup Function

Initial insertion of the back-up battery may cause excessive battery drain (10– 20mA) on early production parts. This condition will not damage the IC, but could prematurely discharge the battery.

CONDITIONS: Two conditions must be present simultaneously for the problem to occur: a voltage rate-of-rise greater that 0.25V/µs at the V_{BATT} terminal (such as can occur when battery is first inserted into the system), and V_{CC} connected to ground with a resistance of less than 10 kilohms.

PREVENTION: Either limit the rate-of-rise of V_{BATT} by inserting a 100 ohm series resistor between the battery and the V_{BATT} terminal and connect a 0.22µF or greater capacitor between V_{BATT} and ground, or insert the battery while V_{CC} is applied to the IC.

CORRECTION: In some instances, it may not be possible to take either of the preventative measures described above. Normal operation can be restored simply by raising V_{CC} above V_{BATT} (i.e., by applying power). The high current mode will not recur, even if V_{CC} subsequently returns to ground.

Pin Description

Name	Pin		Function
	MP690/692	MP 691/693	
V_{CC}	2	3	The +5V input.
V_{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	1	2	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	3	4	0V ground reference for all signals.
$\overline{RESET}$	7	15	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MP 690 and MP691, and 4.4V for the MP692 and MP693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V. $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	5	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.25V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN		13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT		12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MP691, 4.4V for MP693). See Figure 6.
BATT ON		5	BATT ON goes low when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 7mA and can directly drive the base of an external PNP transistor to increase the output current above the 100mA rating of V_{OUT}.
$\overline{LOW\ LINE}$		6	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET		16	RESET is an active high output. It is the inverse of $\overline{RESET}$.
OSC SEL		8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3µA internal pullup. See Table 1.
OSC IN		7	OSC IN sets the Reset delay timing and Watchdog timeout period when OSC SEL floats or is driven high. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is low, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$		14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

Typical Applications

MP691 and MP693

A typical connection for the MP 691/693 is shown in Figure 1. CMOS RAM is powered from V_{OUT}. V_{OUT} is internally connected to V_{CC} when 5V power is present, or to V_{BATT} when V_{CC} is less than the battery voltage. V_{OUT} can supply 100mA from V_{CC}, But if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing 7mA of base drive for the external transistor. When V_{CC} is lower than V_{BATT}, an internal 500Ω MOSFET connects the backup battery to V_{OUT}. The quiescent current in the battery backup mode is 1µA maximum when V_{CC} is between 0V and V_{BATT} - 700mV.

Reset Output

A voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor's Reset line low when V_{CC} is below 4.65V (4.4V for MP693). An internal monostable holds $\overline{\text{RESET}}$ low for 50ms after V_{CC} rises above 4.65V (4.4V for MP693). This prevents repeated toggling of $\overline{\text{RESET}}$ even if the 5V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The MP690 Family power-up $\overline{\text{RESET}}$ pulse lasts 50ms to allow for this oscillator start-up time. The manual reset switch and the 0.1µF capacitor connected to the reset bus can be omitted if manual reset is not needed. An inverted, active high, RESET output is also supplied.

Power Fail Detector

The MP691/93 issues a non-maskable interrupt (NMI) to the microprocessor when a power failure occurs. The +5V power line is monitored via two external resistors connected to the Power Fail Input (PFI). When the voltage at PFI falls below 1.25V, the Power Fail Output ($\overline{\text{PFO}}$) drives the processor's NMI input low. If a Power Fail threshold of 4.8V is chosen, the microprocessor will have the time when V_{CC} falls from 4.8V to 4.65V to save data into RAM. An earlier power fail warning can be generated if the unregulated DC input of the 5V regulator is available for monitoring.

RAM Write Protection

The MP691/93 CE OUT line drives the $\overline{\text{Chip Select}}$ inputs of the CMOS RAM, $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN as long as V_{CC} is above the 4.65V (4.4V for MP693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{\text{CE}}$ OUT goes high, independent of the logic level at $\overline{\text{CE}}$ IN. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The $\overline{\text{LOW LINE}}$ output goes low when V_{CC} falls below 4.65V (4.4V for MP693).

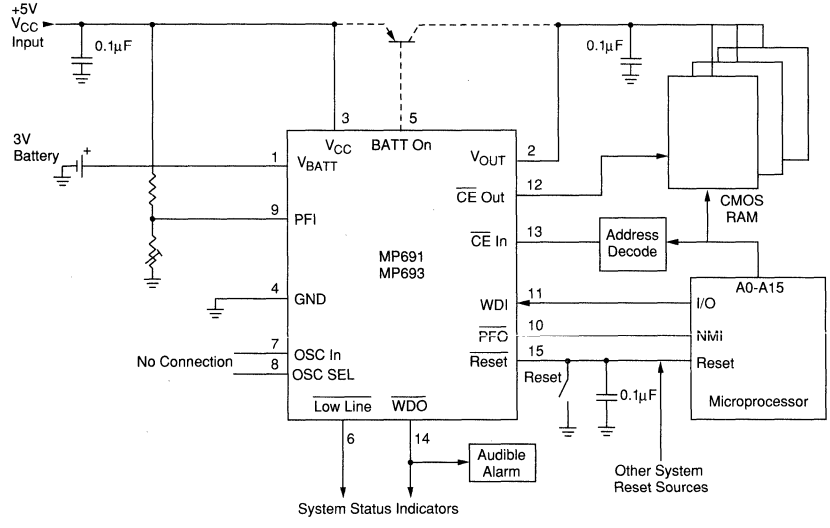


Figure 1. MFP691/693 Typical Application

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC SEL are connected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the MP691/93 will issue a 50ms $\overline{\text{RESET}}$ pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. Once $\overline{\text{WDO}}$ goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MP690 and MP692

The 8-pin MP690 and MP 692 have most of the features of the MP691 and MP693. Figure 2 shows the MP690/692 in a typical application. Operation is much the same as with the MP691/693 (Figure 1) but in this case the Power Fail Input (PFI) monitors the unregulated input to the 7805 regulator. The MP690 $\overline{\text{RESET}}$ output goes low when V_{CC} falls below 4.65V. The $\overline{\text{RESET}}$ output of the MP692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 100mA. The MP690/692 does not have a BATT ON output to drive an external transistor. The MP690/92 also does not include chip enable gating circuitry that is available on the MP691/93. In many systems though, $\overline{\text{CE}}$ gating is not needed since a low input to the microprocessor $\overline{\text{RESET}}$ line prevents the processor from writing to RAM during power-up and power-down transients.

The MP690/92 watchdog timer has a fixed 1.6 second timeout period. If WDI remains either low or high for more than 1.6 seconds., a $\overline{\text{RESET}}$ pulse is sent to the microprocessor. The watchdog timer is disable, if WDI is left floating.

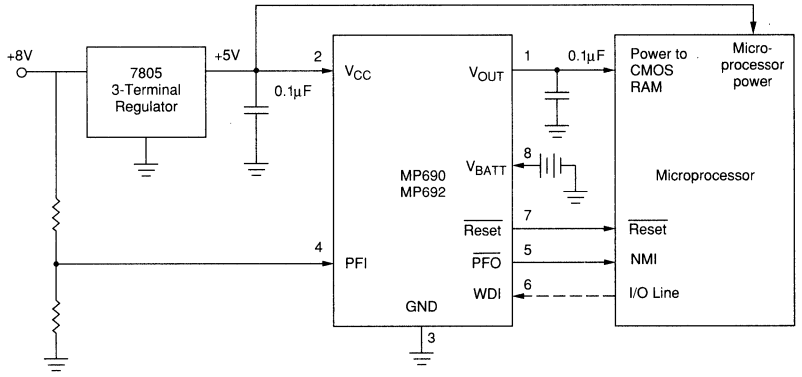


Figure 2. MP690/692 Typical Application

Detailed Description

Battery-Switchover and V_{OUT}

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hystersis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 100mA output current capability and thermal shutdown short circuit protection. Use an external PNP pass transistor in parallel with the internal transistor if the output current requirement at V_{OUT} exceeds 100mA or if a lower V_{CC}-V_{OUT} voltage differential is desired. The BATT ON output (MP691/693 only) can directly drive the base of the external transistor.

It should be noted that the MP690/91/92/93 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1µF bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1µF or greater must be connected to the V_{OUT} terminal to ensure stability.

A 500 ohm MOSFET connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12µA. When V_{CC} is between 0V and (V_{BATT} -700mV) the typical supply current is only 600nA typical, 1µA maximum.

The MP690/691 operates with battery voltages from 2.0V to 4.25V while the MP692/693 operates with battery voltages from 2.0V to 4.0V. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term

memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC}.

A small charging current of typically 10nA (5µ max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharging current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (5µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC}. Table 2 shows the state of the inputs and output in the low power battery backup mode.

Reset Output

$\overline{RESET}$ is an active low output which goes low whenever V_{CC} falls below 4.5V (MP690/691) or 4.25V (MP692/693). It will remain low until V_{CC} rises above 4.75V (MP 690/691) or 4.5V (MP692/693) for 50 milliseconds. (See Figures 5 and 6.)

The guaranteed minimum and maximum thresholds of the MP 690/691 are 4.5V and 4.75V, while the guaranteed thresholds of the MP692/693 are 4.25V and 4.5V. The MP690/691 is compatible with 5V supplies with a +10%, -5% tolerance while the MP692/693 is compatible with 5V ±10% supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MP690/691, and 4.4V in the MP692/693.

The response time of the reset voltage comparator is about 100µs. V_{CC} should be bypassed to ensure that glitches do not activate the $\overline{RESET}$ output.

$\overline{RESET}$ also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. $\overline{RESET}$ has an internal 3µA pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

$\overline{CE}$ Gating and RAM Write Protection

The MP691 and MP693 use two pins to control the $\overline{Chip\ Enable}$ or $\overline{Write}$ inputs of CMOS RAMs. When V_{CC} is +5V, $\overline{CE}$ OUT is a buffered replica of $\overline{CE}$ IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces $\overline{CE}$ OUT high, independent of $\overline{CE}$ IN. The MP693 $\overline{CE}$ OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The $\overline{CE}$ output of both devices is also forced high when V_{CC} is less than V_{BATT}. (See Figure 5.)

$\overline{CE}$ OUT typically drives the $\overline{CE}$, $\overline{CS}$, or $\overline{Write}$ input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the $\overline{CE}$ OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of $\overline{CE}$ OUT is too long, connect $\overline{CE}$ IN to GND and use the resulting second alternative is to AND the $\overline{LOW\ LINE}$ output with the $\overline{CE}$ or $\overline{WR}$ signal. An external logic gate and the $\overline{RESET}$ output of the MAX690/692 can also be used for CMOS RAM write protection.

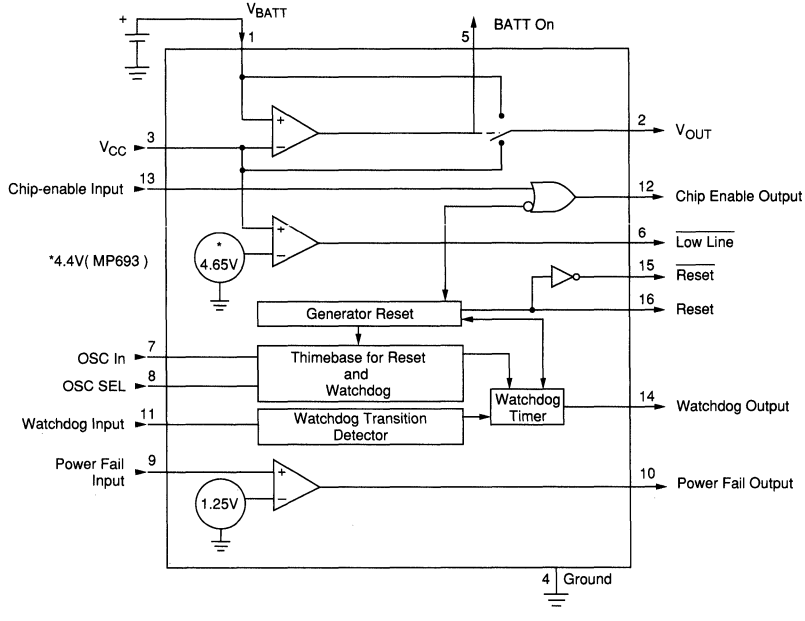


Figure 3. MP691/693 Block Diagram

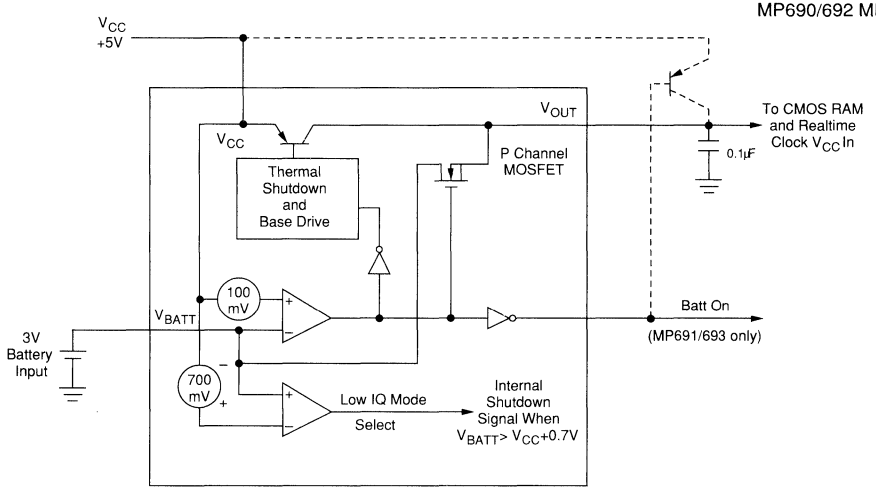


Figure 4. Battery Switchover Block Diagram

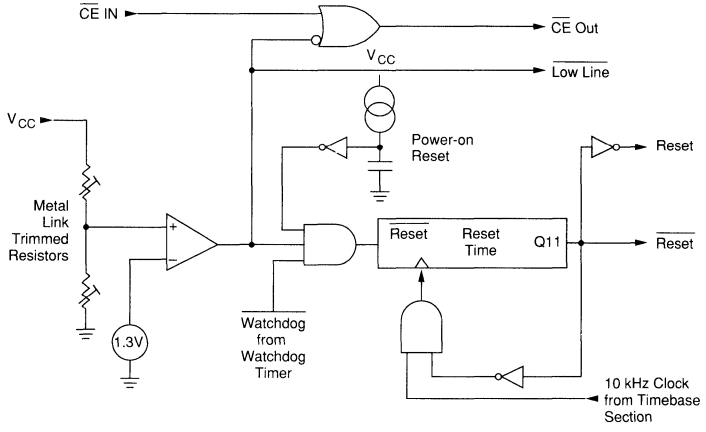


Figure 5. Reset Block Diagram

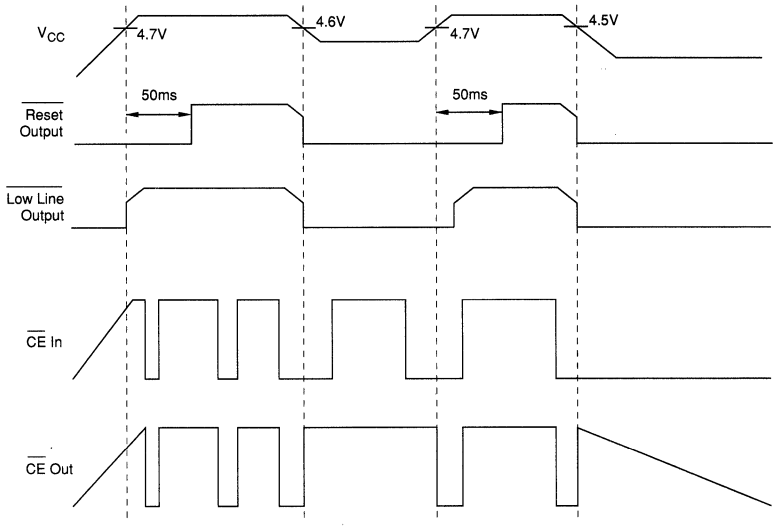


Figure 6. MP691 Reset Timing

1.25V Comparator and Power Fail Warning

The Power Fail Input (PFI) is compared to an internal 1.25V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.25V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.25V several milliseconds before the +5V supply falls below 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the $\overline{RESET}$ output goes low (4.5V for MP692/93).

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and $\overline{PFO}$ is forced low when V_{CC} is lower than the V_{BATT} input voltage.

Watchdog Timer and Oscillator

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 millisecond $\overline{RESET}$ pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MP691/693 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after $\overline{RESET}$ has gone high. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output ($\overline{WDO}$, MP691/693 only) goes low if the watchdog timer "times out", and it remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6 seconds and the rest pulse width is fixed at 50ms on the 8-pin MP690 and MP692. The MP691 and MP693 allow these times to be adjusted per Table 1. Figure 8 show various oscillator configurations.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period to 70ms.

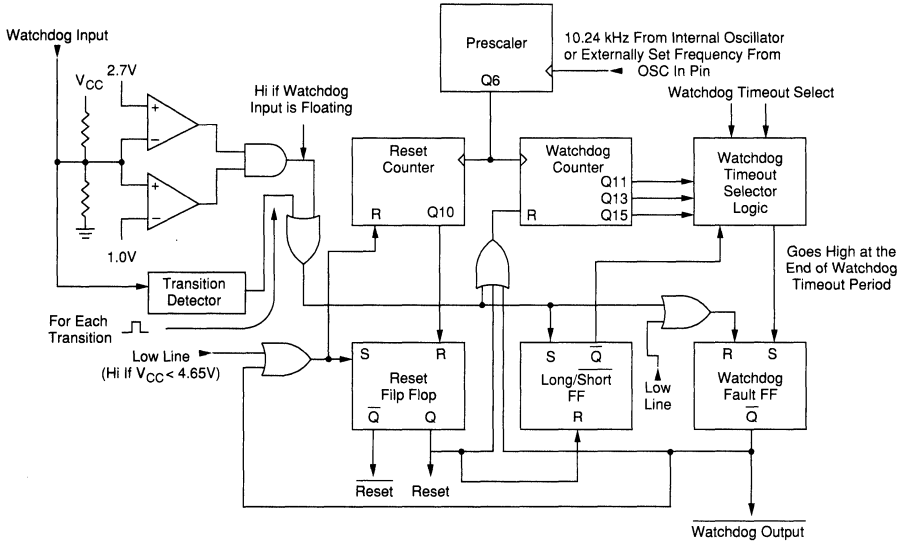


Figure 7. Watchdog Timer Block Diagram

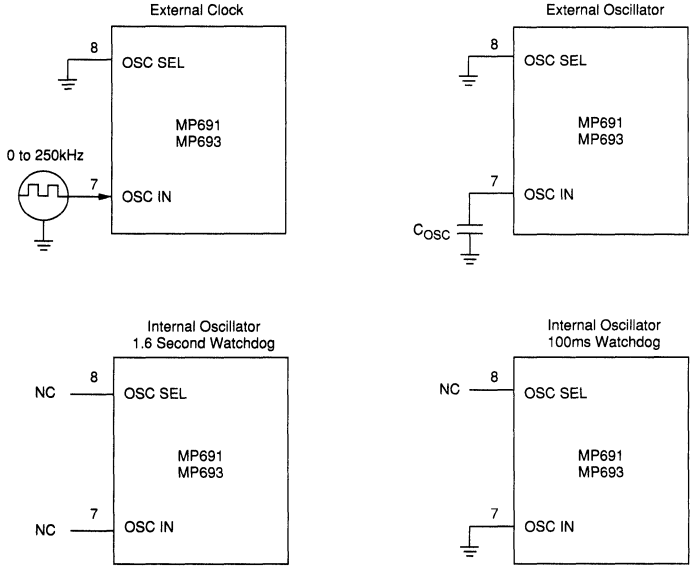


Figure 8. Oscillator Circuits

Table 1. MP691 and MP693 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 clks	4096 clks	512 clks
Low	External Capacitor	$\frac{400ms}{47pF} \times C$	$\frac{1.6\ sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$
High/Floating	Low	100ms	1.6 sec	50ms
High/Floating	High / Floating	1.6 sec	1.6 sec	50ms

Note 1. The MP690 watchdog timeout period is fixed at 1.6 seconds nominal; the MP690 Reset pulse width is fixed at 50ms nominal.

Note 2. When the MP691 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz.
The nominal oscillator frequency with external capacitor is $F_{OSC}\ (Hz) = \frac{1.75 \times 10^7}{C_{OSC}\ (Farads)}$

Note 3. See Electrical Specifications Table for minimum and maximum timing values.

Application Hints

Other uses of the Power Fail Detector

In Figure 9 the Power Fail Detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the Power Fail Detector is not as accurate as the onboard Reset voltage detector, a trimput must be used to adjust the voltage detection threshold. Both the PFO and $\overline{RESET}$ outputs have high sink current capability and only 10µA of source current drive. This allows the two outputs to be connected directly to each other in a "wired or" fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 12. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 13). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MP690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01µF capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 14 is used.

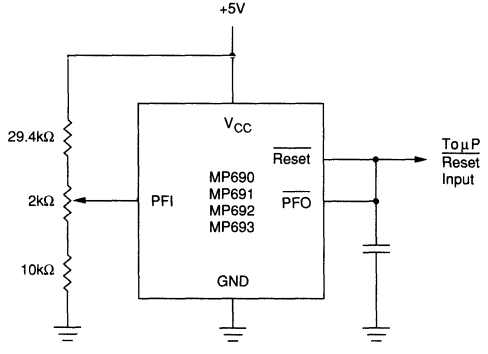


Figure 9. Externally Adjustable V_{CC} Reset Threshold

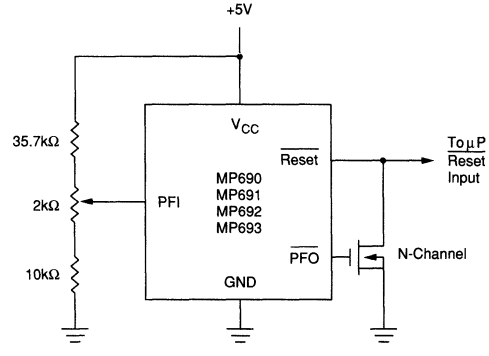


Figure 10. Reset on Overvoltage or Undervoltage

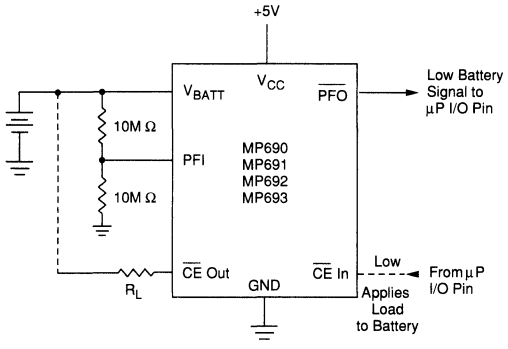


Figure 11. Backup Battery Monitor with Optional Test Load

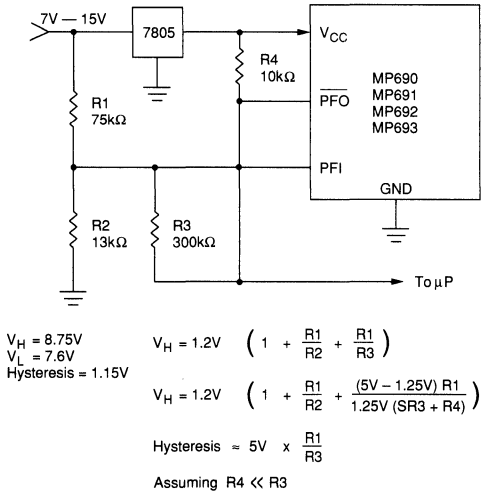


Figure 12. Adding Hysteresis to the Power Fail Voltage Comparator

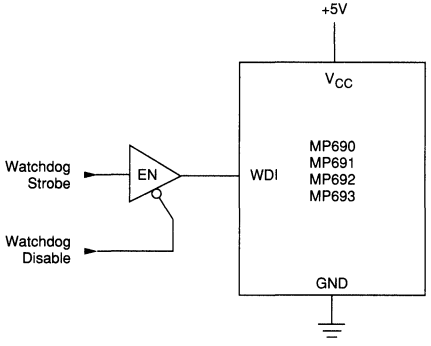


Figure 13. Disabling the Watchdog under Program Control

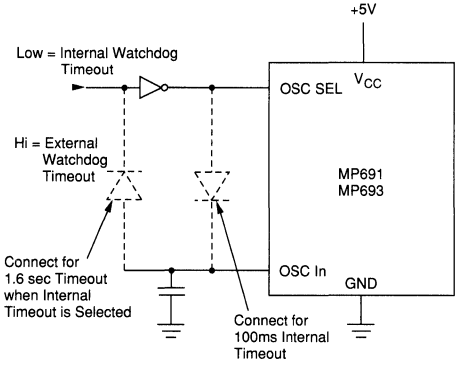
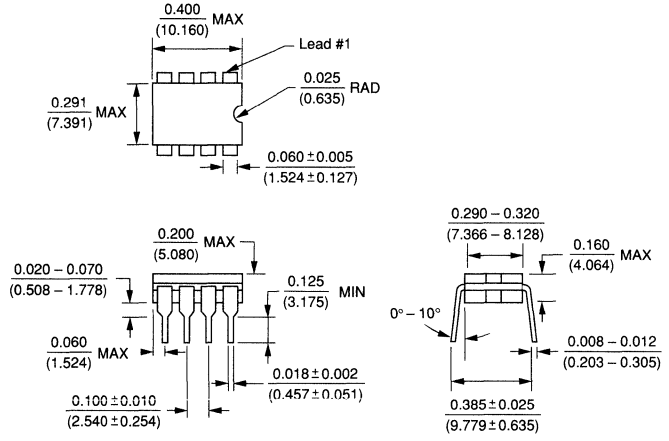


Figure 14. Selecting Internal or External Watchdog Timeout

Table 2. Input and Output Status In Battery Backup Mode

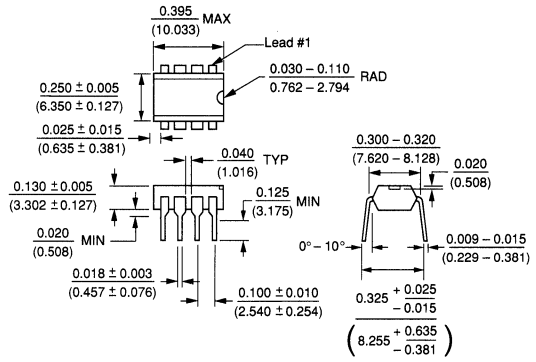
V_{BATT}, V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	Logic high.
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high.
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
$\overline{PFO}$	Logic low.
$\overline{CE}$ IN	$\overline{CE}$ IN has a 2µA input pullup current source. Float or drive high to minimize supply current.
$\overline{CE}$ OUT	Logic high.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12µA is drawn from the V_{BATT} input when V_{CC} is between V_{BATT} + 100mV and V_{BATT} - 700mV. The supply current is 1µA maximum when V_{CC} is less than V_{BATT} - 700mV.

Package Information



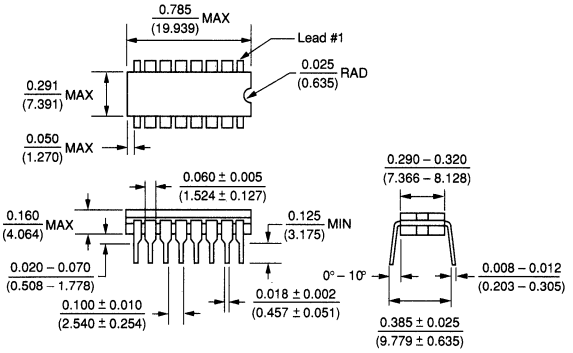
8 LEAD CERDIP (D)

θ_{ja} = 125°C/W
θ_{jc} = 55°C/W



8 LEAD PLASTIC DIP (P)

θ_{ja} = 120° C/W
θ_{jc} = 70° C/W

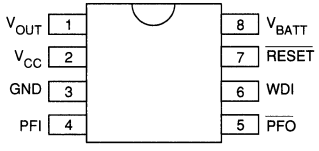


16 LEAD CERDIP (D)

θ_{ja} = 100° C/W
θ_{jc} = 50° C/W

Pin Configuration

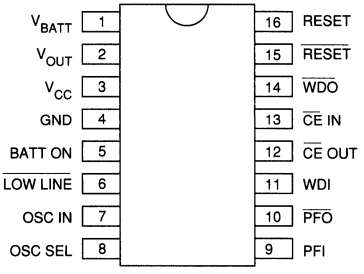
MP690 & MP692



top view

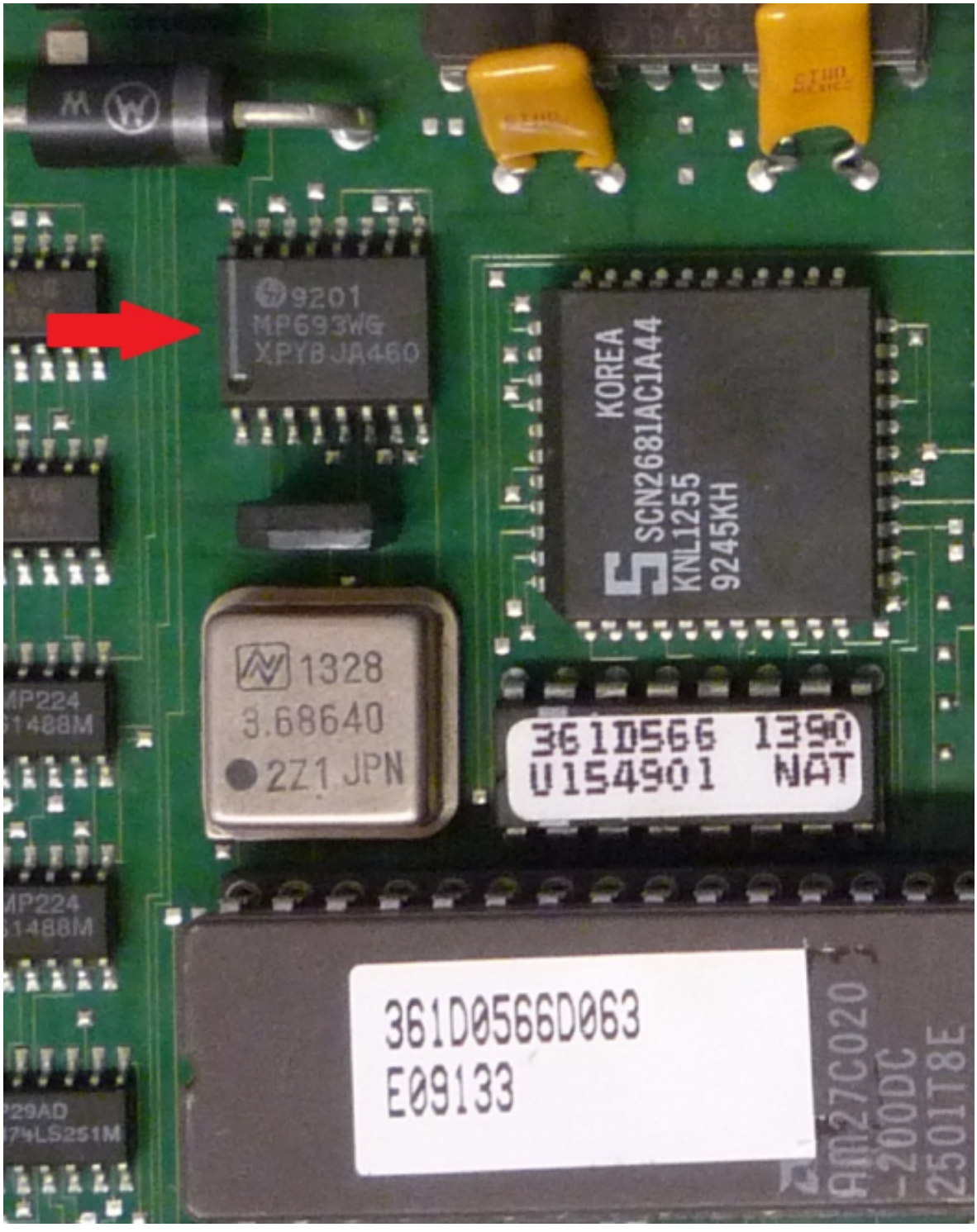
8-pin DIP

MP691 & MP693



top view

16-pin DIP


9201
MP693WG
XPYBJA460
KOREA
SCN2681AC1A44
KNL1255
9245KH
1328
3.68640
2Z1 JPN
361D566 1390
U154901 NAT
361D0566D063
E09133
AM27C020
-200DC
2501T8E