Zilog

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User's Manual

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Z-80 SIB
USER'S MANUAL

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SIB USER'S MANUAL

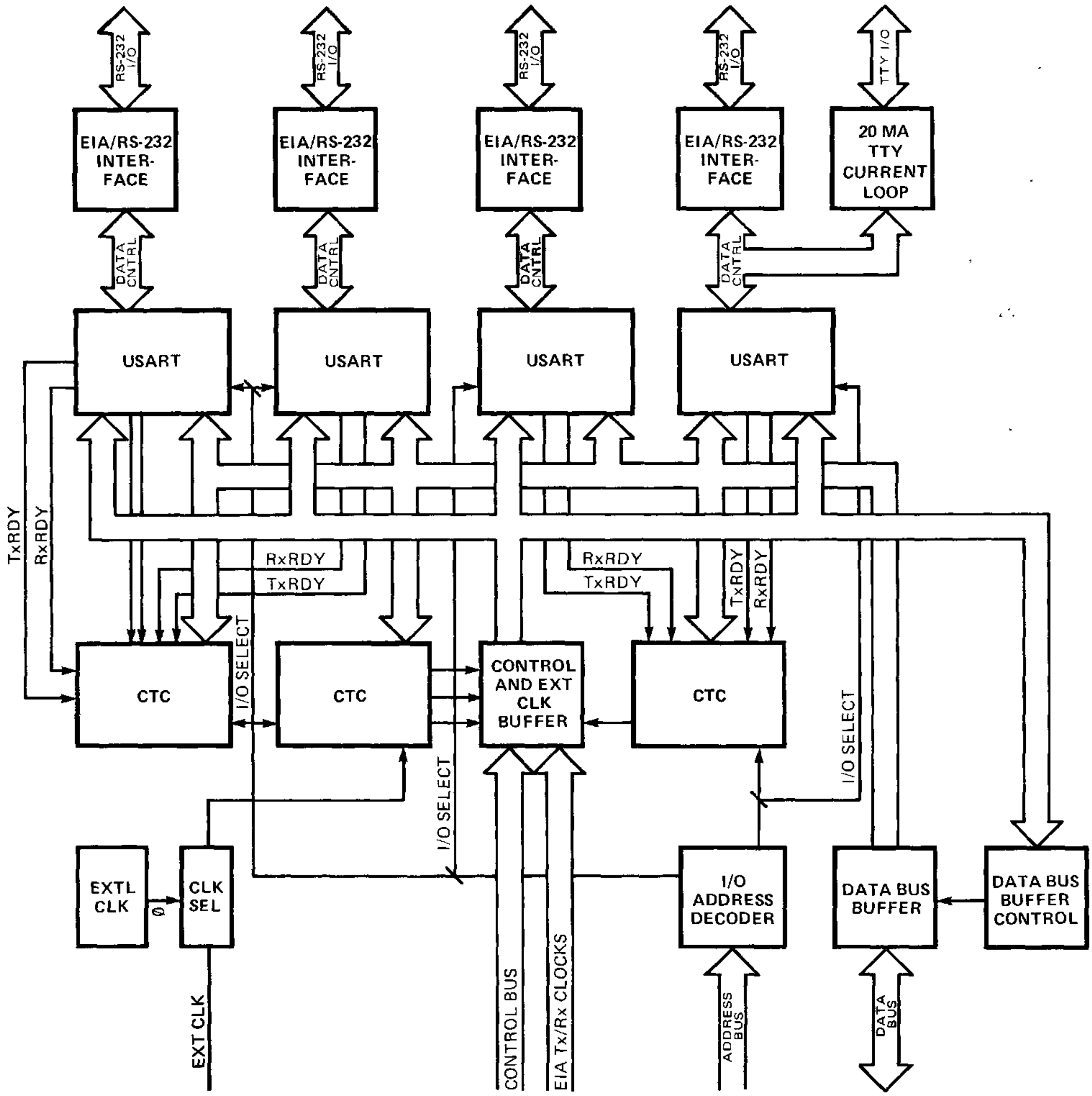
TABLE OF CONTENTS

SECTION 1. GENERAL INFORMATION

1.1 Product Description

The Z80-Serial Interface Board (SIB) provides four programmable, bi-directional serial communication channels for the MCB Series OEM products. Each bi-directional channel can support asynchronous or synchronous data transfer with half or full duplex signaling. Character length, parity, sync insertion and pattern, clock rate, and break character length are all under program control. Each channel is supported by separate modem control signals; DSR (Data Set Ready), DTR (Data Terminal Ready), RTS (Request to Send), CTS (Clear to Send). All four channels are RS232-buffered, and one channel will accommodate a 20mA TTY current-loop interface. Three Z80-CTC (Counter Timer Circuit) devices generate three independent baud rates and accommodate fully interrupt-driven operation.

1.2 Block Diagram



SERIAL INTERFACE BLOCK DIAGRAM

2.0 INSTALLATION

2.1 Initial Unpacking and Inspection

Inspect the product for shipping damage as soon as it is unpacked. Check for any physical damage that may be attributed to abuse and handling during shipment. If the product is damaged in any way, notify the carrier immediately.

2.2 Installation (MCZ-1)

The Serial Interface Boards may be installed in slot J4 in the MCZ-1/20 or MCZ-1/25 systems. J1, an undedicated and unwired position, may also be used. In the MCZ-1/30 System, J1, and J4 of each card cage, may be used in the identical manner as previously described. In the MCZ-1/05, and PDS systems, J1 (User's Option) will directly accommodate the Serial Interface Board.

2.3 Power and Signal Connections

The Z80-SIB is pin-compatible with the Z80-MCB bus structure. For convenience, the wire list for interconnection between the MCB and the SIB is provided:

TO	FROM	DESCRIPTION
SIB:1-3, 59-61	MCB:1-3, 59-61	+5V P.S.
SIB:4	MCB:4	IORQ-
SIB:5	MCB:5	DB5
SIB:8	MCB:8	DB3
SIB:9	MCB:9	MASTER RESET
SIB:12	MCB:12	DB6
SIB:13	MCB:13	DB0
SIB:23	MCB:23	WR-
SIB:26	MCB:26	AB7
SIB:29	MCB:29	AB5
SIB:30	MCB:30	AB6
SIB:62-64, 120-122	MCB:62-64, 120-122	GND
SIB:68	MCB:68	DB4
SIB:71	MCB:71	DB2
SIB:73	MCB:73	DB7
SIB:75	MCB:75	DB1
SIB:79	MCB:79	INT-
SIB:98	MCB:98	AB4
SIB:99	MCB:99	PHI-.(SYSTEM CLOCK-)
SIB:100	MCB:100	AB3
SIB:101	MCB:101	AB2
SIB:102	MCB:102	AB1
SIB:103	MCB:103	AB0
SIB:115	MCB:115	M1-
SIB:116	MCB:116	RD-

TABLE 2.3.1: MCB to SIB Wire List

3.0 OPERATION

3.1 Description

The Z80-SIB uses four 8251 USART devices to implement the serial communication channels. Two Z80-CTC devices are used to accommodate Z80 interrupt capability for receive and transmit operation for each bi-directional serial channel. A third Z80-CTC device is provided to accommodate programmable baud rates for each serial port from 50 to 9600 baud derived from an on-board crystal clock, the system clock, or an external clock.

Interrupt operation is accommodated by including the two CTC devices in the interrupt daisy chain, and after appropriate strapping to determine clock drivers for baud generation, the interrupt handling CTC devices are loaded with a count of one. After USART initialization, the CTC interrupts are enabled. (See Section 4.1 for a detailed description of initialization.) Consequently, when the transmitter buffer is empty or the receiver buffer is full, the TxRDY or RxRDY lines from the USART will go high, causing the CTC counter to decrement, and thus, generating an interrupt. The data bus control PROM detects that the interrupt is being generated from the USART interrupt handling CTC devices, IEI1(high) and IEO2(low) and turns the three-state bus buffers towards the CPU when M1- and IORQ- are active. Thus, the vector interrupt address from the interrupting CTC channel is read by the CPU. The CTC channel reloads with a count of one, becoming ready to generate another interrupt.

3.2 Interrupt Configuration

Interrupt requests may originate from eight sources on the SIB. Four interrupts can be generated by the CTC when any one of the USARTs is ready to accept a data character (TxRDY). The order of priority is channel 0 first, through channel 3. Another four interrupts can be generated when any one of the USARTs contains a character that is ready to be input to the CPU (RxRDY). Again, the order of priority is channel 0 first, through channel 3. However, the RxRDY lines will have priority over any of the TxRDY lines. Each interrupt is maskable under program control. Figure 3.2.1 indicates the priority order between the two daisy-chained CTC's.

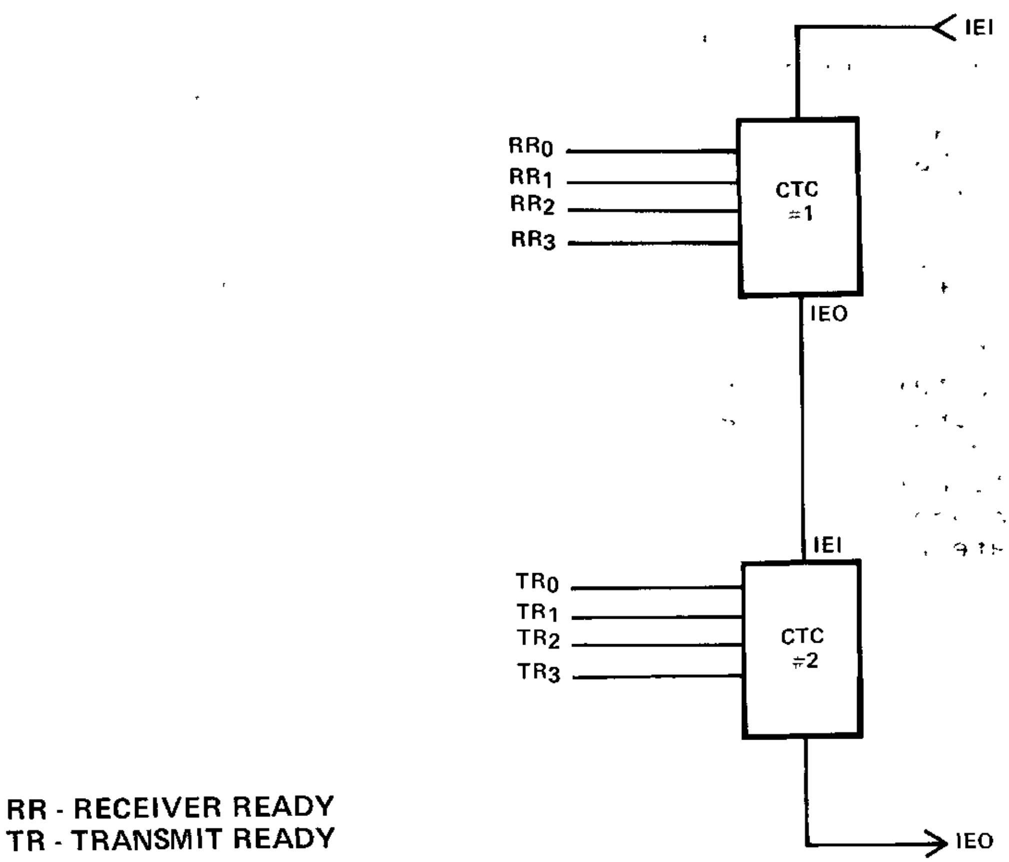


FIGURE 3.2.1 SIB INTERRUPT PRIORITY STRUCTURE

3.3 Port Address Selection

The SIB has 20 I/O ports associated with it; 12 for the three CTCs, and 8 for the four USARTs. To position these 20 ports in the I/O address space, jumpers at J1 and J4 are required (see schematics, page 3). The user can place the ports in one of eight address ranges, with each range having 32 available ports. Table 3.3.1 below shows the jumper connections corresponding to each address range:

ADDRESS RANGE	J4 JUMPERS
00 to 1F	5-16, 1-7, 3-6
20 3F	5-15, 1-7, 3-6
40 5F	5-16, 2-7, 3-6
60 7F	5-15, 2-7, 3-6
80 9F	5-16, 1-7, 4-6
A0 BF	5-15, 1-7, 4-6
C0 DF	5-16, 2-7, 4-6
E0 FF	5-15, 2-7, 4-6

TABLE 3.3.1 Port Address Range

Jumpers applied to J1 will position each I/O port into a unique address within the range selected. Each of the device select lines, GPM- through GPT-, is connected to one of the port decoder outputs, GP0- through GP7-. Tables 3.3.2 and 3.3.3 show the corresponding jumper connections at J1:

DEVICE SELECTS	DEVICE	JUMPER J1
GPM-	USART 0, 1	14
GPN-	USART 2, 3	13
GPR-	CTC0	12
GPS-	CTC1	11
GPT-	CTC2	10

TABLE 3.3.2 Device Select

DECODER OUTPUTS	UNIQUE ADDRESSES	JUMPER J1
GP0-	00 TO 03	1
GP1-	04 07	2
GP2-	08 0B	3
GP3-	0C 0F	4
GP4-	10 13	5
GP5-	14 17	7
GP6-	18 1B	8
GP7-	1C 1F	6

TABLE 3.3.3 Port Address Select

The two ports for each USART are further decoded by the two least significant address lines.

Addressing Example:

Assume that the 20 SIB ports will be in the range 80H-9FH. The following connections should be made at J4:.

J4 - 5 to J4 - 16
J4 - 1 to J4 - 7
J4 - 4 to J4 - 6

Next, unique addresses must be assigned to each CTC and USART I/O port.

DEVICE	J1 JUMPER	PORT ADDRESS
CTC0	12 - 1	80H - 83H
CTC1	11 - 2	84H - 87H
CTC2	10 - 5	90H - 93H
USART 0	14 - 7	94H - 95H
USART 1		96H - 97H
USART 2	13 - 8	98H - 99H
USART 3		9AH - 9BH

This example shows that only one jumper is needed for each pair of USARTs. The final port addresses are obtained by adding the addresses determined by J1 to the base address of the range selected by J4.

3.4 Baud Rate Generation

One Z80-CTC is dedicated to establishing one of 14 baud rates for each of the four USART channels. Since only three CTC outputs are available to the four USARTs, two of the USARTs must share a common CTC clock. However, the shared clock can be divided by 16 with one USART and by 64 with the other, allowing each of the four USARTs to have an independent baud rate.

The CTC may be programmed to operate in either a timer or counter mode. In the timer mode, the time base is derived from the system clock, while in the counter mode, an external clock is used. Jumpers on J3 determine which external clocks will be used if operating in the counter mode. The options available on the SIB for these external clocks are two clocks generated on the board (phi/2 and phi/32) and one clock generated by the MCB (phi/2). Table 3.4.1 summarizes the CTC clock/trigger (CK/Tx) inputs and external clocks available at J3.

	Jumper J3
External Clocks For Counter Operation	
MCB PHI/2	4
On Board PHI/32	5
On Board PHI/2	6
CTC Inputs For Counter Operation	
CK/T0	11
CK/T1	12
CK/T2	13

TABLE 3.4.1: CTC Clock/Trigger Inputs and External Clocks Available on J3

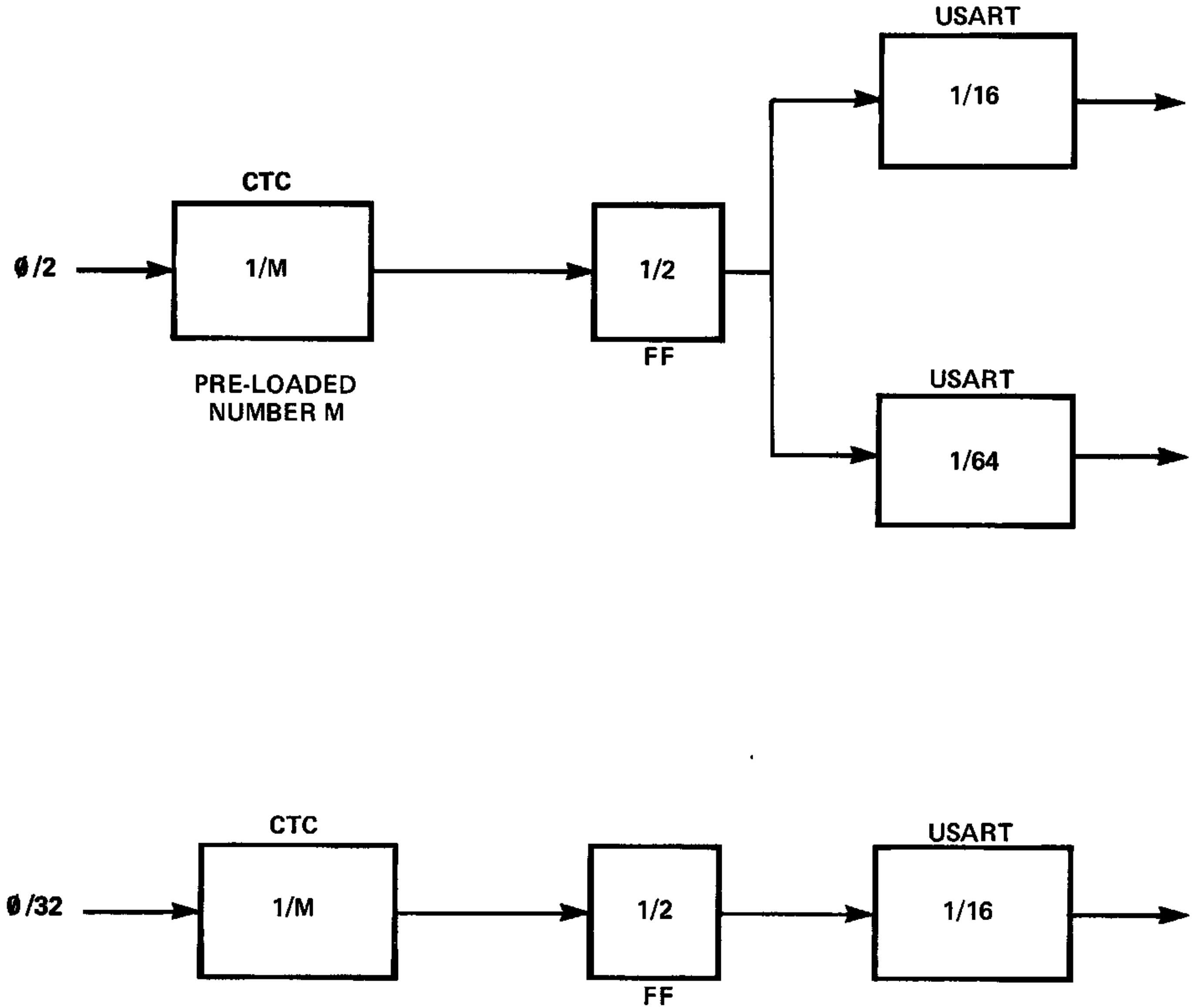


FIGURE 3.4.1 SAMPLE CONFIGURATIONS WITH CTC IN COUNTER MODE

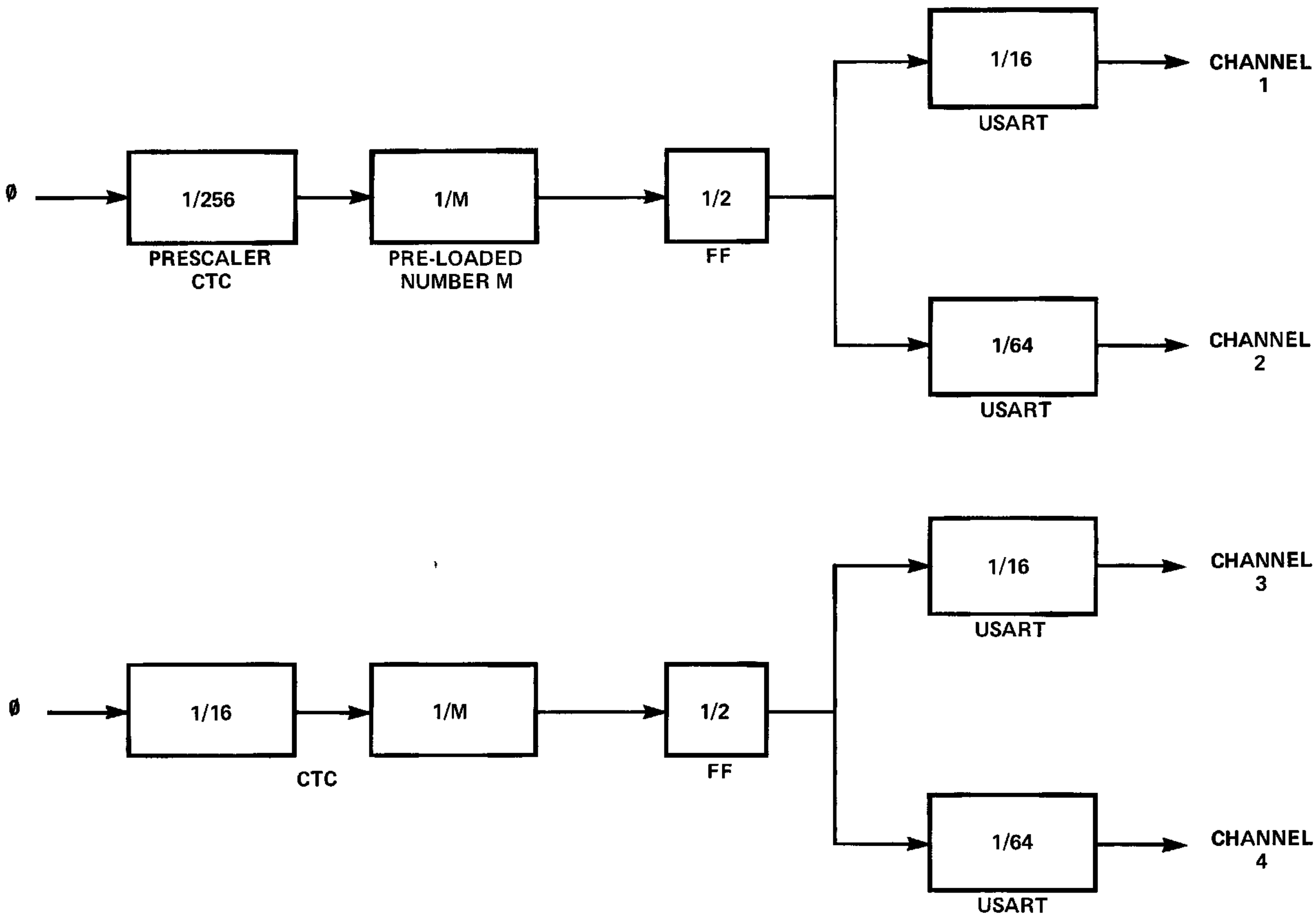


FIGURE 3.4.2: SAMPLE CONFIGURATIONS WITH CTC IN TIMER MODE

Figures 3.4.1 and 3.4.2 symbolically represent the function performed by the CTC in each mode. The flip-flop between the CTC and USART is used to convert the pulse signal from the CTC into a 50% duty cycle signal required by the USART. Table 3.4.3 shows the time constants to be loaded into the CTC in order to generate the indicated baud rate.

In addition to the baud rate clocks provided by the CTC, external RS232-level clocks may be used. This selection is made by applying jumpers at J2, as shown in Table 3.4.2:

SIGNAL	JUMPER J2
TxC0	14
RxC0	13
TxC1	6
RxC1	5
TxC2	16
RxC2	15
TxC3	1
RxC3	12
IN0	9
IN1	10
IN2	8
IN3	7
CTC CLK0	2
CTC CLK1	3
CTC CLK2	4

Where: TxC = USART Transmitter Clock
RxC = USART Receiver Clock
IN = External RS232 Clock
CTC CLK = 50% Duty Cycle CTC Clock

TABLE 3.4.2: USART Clock Inputs

BAUD RATE	PRE-LOAD NO. M						
	COUNTER MODE			TIMER MODE			
	Ø/2		Ø/32	CHANNEL			
	X16	X64	X16	1	2	3	4
50		192	48	6		96	24
75		128	32	4	1	64	16
110		87	22			44	11
134.5		72	18			36	9
150	256	64	16	2		32	8
200	192	48	12			24	6
300	128	32	8	1		16	4
600	64	16	4			8	2
1200	32	8	2			4	1
2400	16	4	1			2	
4800	8	2				1	
9600	4	1					
19200	2						
38400	1						

TABLE 3.4.3: PRE-LOAD NO. VS. BAUD RATE

The equation used to derive the CTC time constant 'M' for the counter mode is as follows:

$$M = \frac{CLK}{BR \times DF \times 2}$$

Where: M = CTC Time Constant
CLK = $\Phi/2$ or $\Phi/32$ (Φ=2.4576 x 10**6)
BR = Baud Rate
DF = USART Divider Factor

The equation used to derive the CTC time constant 'M' for the timer mode is as follows:

$$M = \frac{\Phi}{BR \times DF \times PR \times 2}$$

Where: M = CTC Time Constant
Φ = System Clock (2.4576 x 10**6)
BR = Baud Rate
DF = USART Divider Factor
PR = CTC Pre-Scaler

Notice that the factor of 2 which appears in each equation is a result of the symmetry flip-flop between the CTC and USART.

3.5 Serial Interface

The SIB may be customized to meet specified peripheral requirements. Each USART channel is provided with jumper points for interchanging I/O line drivers and receivers for interface to either a terminal or modem.

USART NO.	JUMPER LOCATION JX
0	J5
1	J6
2	J7
3	J8

Table 3.5.1 below identifies the jumper on the appropriate JX pin when using the SIB for interface to a terminal. Table 3.5.2 below identifies the jumpers on the appropriate JX pin when using the SIB for interface to a modem.

FROM		TO	
SIGNAL	JX PIN NO.	SIGNAL	JX PIN NO.
TXDB	1	TRXD	13
RXDB	2	TTXD	14
RTSB	3	TCTS	11
CTSB	4	TRTS	12
DSRB	5	TDTR	10
DTRB	6	TDSR	9
+12V	7	SPARE	8

TABLE 3.5.1: Modem Mode (SIB 'talks' to a terminal)

FROM		TO	
SIGNAL	JX PIN NO.	SIGNAL	JX PIN NO.
TXDB	1	TTXD	14
RXDB	2	TRXD	13
RTSB	3	TRTS	12
CTSB	4	TCTS	11
DSRB	5	TDSR	9
DTRB	6	TDTR	10
+12V	7	SPARE	8

TABLE 3.5.2: Terminal Mode (SIB 'talks' to a modem)

USART3 (A16) may be configured for either a TTY or an EIA interface. As shipped, jumper points J9-1 to J9-9 are connected with PC traces as follows:

J9	SIGNAL
1-2, 2-3	TxD
4-6	RxD
7-8, 8-9	DTR (TTY TAPE CONTROL)

The transmitted data from the USART (J9-1) is connected to both the EIA driver (J9-2) and the TTY driver (J9-3). The USART receiver data (J9-4) is connected to the TTY receiver (J9-6). Both DTRB (J9-8) and TTY tape control (J9-9) are connected to the USART DTR signal (J9-7). To be configured as an EIA interface, the trace from J9-4 to J9-6 must be cut and a jumper added from J9-4 to J9-5. Jumper points J9-1,2,3 and J9-7,8,9 are located just to the right of A6, and jumper points J9-4,5,6 are just above A23.

3.6 USART Operation

3.6.1 USART Signal Description

Data Bus (D0-D7)

This three-state, 8-bit bus is used for information exchange between the USART and the host processor. Data, control, and status bytes are exchanged upon execution of input and output instructions from the Z80.

Reset (RST)

The USART will assume an idle state when a high level is applied to the reset input. When the reset is returned low, the USART will remain in the idle state until it receives a new mode control instruction.

Clock (CLK)

This input is used for internal timing within the USART. It does not control the transmit or receive rate. However, it should be at least 30 times the receive or transmit rate in the synchronous mode and 4.5 times the receive or transmit rates in the asynchronous mode. The CLK frequency is also restricted by both an upper and a lower bound.

Control/Data (C/D)

During a read operation, if this input is at a high level, the status byte will be read, and if it is at a low level, the receive data will be read by the processor. When a write operation is being performed, this input will indicate to the USART that the bus information being written is a command if C/D is high and data if C/D is low.

C/D-	RD-	WR-	CS-	
0	0	1	0	USART DATA-->DATA BUS
0	1	0	0	DATA BUS-->USART DATA
1	0	1	0	USART STATUS-->DATA BUS
1	1	0	0	DATA BUS-->USART COMMAND
X	X	X	1	DATA BUS-->3-STATE

Read (RD-)

This active low input enables data or status to be transferred from the USART to the Z80.

Write (WR-)

This active low input enables data or control to be transferred to the USART from the Z80.

Chip Select (CS-)

This active low input enables the processor to access the USART for an I/O operation. When CS- is high, the data bus output is in the high impedance state.

Data Set Ready (DSR-)

This is a general-purpose input signal and forms part of the status byte that may be read by the processor. DSR- is generally used as a response to DTR by the modem to indicate that it is ready. The signal acts only as a flag and does not control any internal logic.

Data Terminal Ready (DTR-)

This output signal reflects the condition of bit 1 in the command byte from the Z80. The DTR signal is commonly used for data terminal ready or rate select in modem control.

Clear to Send (CTS-)

This is a general-purpose input signal used to enable the USART to transmit data if the TxEN bit in the command byte is a one. CTS- is generally used as a response to RTS- by a modem to indicate that transmission may begin. Designers not using CTS- in their systems should remember to tie it low so that USART data transmission will not be disabled.

Request to Send (RTS-)

This output signal reflects the condition of bit 5 in the command byte from the Z80. The RTS- signal is commonly used to initiate a data transmission by requesting the modem to prepare to send.

Transmit Data (TxD)

Data from the data bus is converted to a serial format with appropriate sync, start/stop, and parity information inserted into the data stream. This bit stream is then transmitted to the TxD output.

Transmitter Ready (TR)

The TR output signal goes high when data in the transmit data buffer has been shifted into the transmitter section allowing the transmit data buffer to accept the next byte from the processor. TR will be reset when information is written into the transmit data buffer. Loading the command register also resets TR. TR will be available on this output pin only when the USART is enabled to transmit (CTS-=0, TxEN=1). However, the TxRDY bit in the status buffer will always be set when the transmit data buffer is empty regardless of the state of TxEN and CTS-.

TR can be tested by checking bit 0 of the status register for polling operation or the TR signal can be used to generate an interrupt. On the SIB, CTC2 is used to receive the active high TR signal from the USART to decrement a counter from 1 to 0, and consequently, provide a Z80 mode 2 interrupt vector.

Transmitter Clock (TxC-)

The transmitter clock controls the serial character transmission rate. In the asynchronous mode, the TxC- frequency is a multiple of the actual baud rate. Bits 0 and 1 of the mode instruction select the multiple to be 1x, 16x, or 64x the baud rate. In the synchronous mode, the TxC- frequency is automatically selected to equal the actual baud rate.

Note that for both synchronous and asynchronous modes, serial data is shifted out of the USART by the falling edge of TxC-.

Receive data (RxD)

Composite serial data is received at this input and converted to a parallel format; sync, start/stop, and parity are checked, and then the assembled byte is prepared for buffering to the Z80. For communications requiring less than 8 bits per character, the extra bits are set to logical "zero".

Receiver Ready (RR)

The RR output signal indicates to the processor that data has been shifted into the receiver buffer from the receiver section and may be read. The signal is active high and will be reset when the buffer is read by the processor. RR can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver may be running. If the processor does not read the receiver buffer before the next character is shifted from the receiver section, then an overrun error will be indicated in the status buffer.

RR can be tested by checking bit 1 of the status register for polling operation or the RR signal can be used to generate an interrupt. On the SIB, CTC1 is used to receive the active high RR signal from the USART to decrement a counter from 1 to 0, and consequently, provide a Z80 mode 2 interrupt vector.

Receiver Clock (RxC-)

The receiver clock is the rate at which the incoming character is received. In the asynchronous mode, the RxC frequency may be 1, 16, or 64 times the actual baud rate, but in the synchronous mode, the RxC- frequency must equal the baud rate. Bits 0 and 1 in the mode instruction select asynchronous at 1x, 16x, or 64x or synchronous operation at 1x the baud rate.

Unlike TxC-, data is sampled by the USART on the rising edge of RxC-. Since the USART will frequently be handling both the reception and transmission for a given link, the receive and transmit baud rates will be the same. RxC- and TxC- then require the same frequency and may be tied together and connected to a single clock source or baud rate generator.

Sync Detect (SYNC)

This signal is used only in the synchronous mode. It can be an input or output depending on the USART mode instruction, programming the operation for external or internal synchronization, respectively. In the internal sync mode, the SYNC "output" will go to a logical one when the USART has identified the sync character in the receiver data stream. If the USART is programmed for "bi-sync" operation, the sync output will not go to a logical one until the second consecutive sync character has been identified. In both cases, the sync output transition from low to high will occur in the middle of the last bit of the respective sync character. Sync and bit 6 (sync) in the status register are reset when the status buffer is read or when a device RST occurs.

In the external sync mode, a positive edge on the sync "input" will cause the USART to start assembling a data byte on the next falling edge of RxC-. The sync signal should remain high for at least one RxC- period.

3.6.2 Operational Descriptions

Operational Description

A set of control words must be sent to the USART to define the desired mode and communications format. The control words will specify the baud rate factor (1x, 16x, 64x), character length (5 to 8), number of stop bits (1, 3/2, 2), asynchronous or synchronous mode, syndet (internal or external), parity, etc.

After receiving the control words, the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the USART may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

NOTE: The 8251 and 9551 USARTs may provide faulty data from the receiver buffer for the first read after power-on. A dummy read is recommended.

The USART cannot transmit until the TxEN (Transmitter Enable) bit has been set by a command instruction and until the CTS- (Clear to Send) input is a "zero".

USART Programming

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external reset is not available, three successive zeros followed by a reset command instruction can be used to initialize the USART. TxD is held in the "marking" state after reset, waiting for a new command instruction.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This control word specifies the general characteristics of the interface regarding the synchronous or asynchronous mode, baud rate factor, character length, parity, and number of stop bits. Once the mode instruction has been received, sync characters or command instructions may be inserted depending on the mode instruction content.

Command Instruction

This control word directs the actual operation of the format selected in the mode instruction. Functional control of transmit and receive, error reset, reset, and modem signals are accommodated in the command instruction.

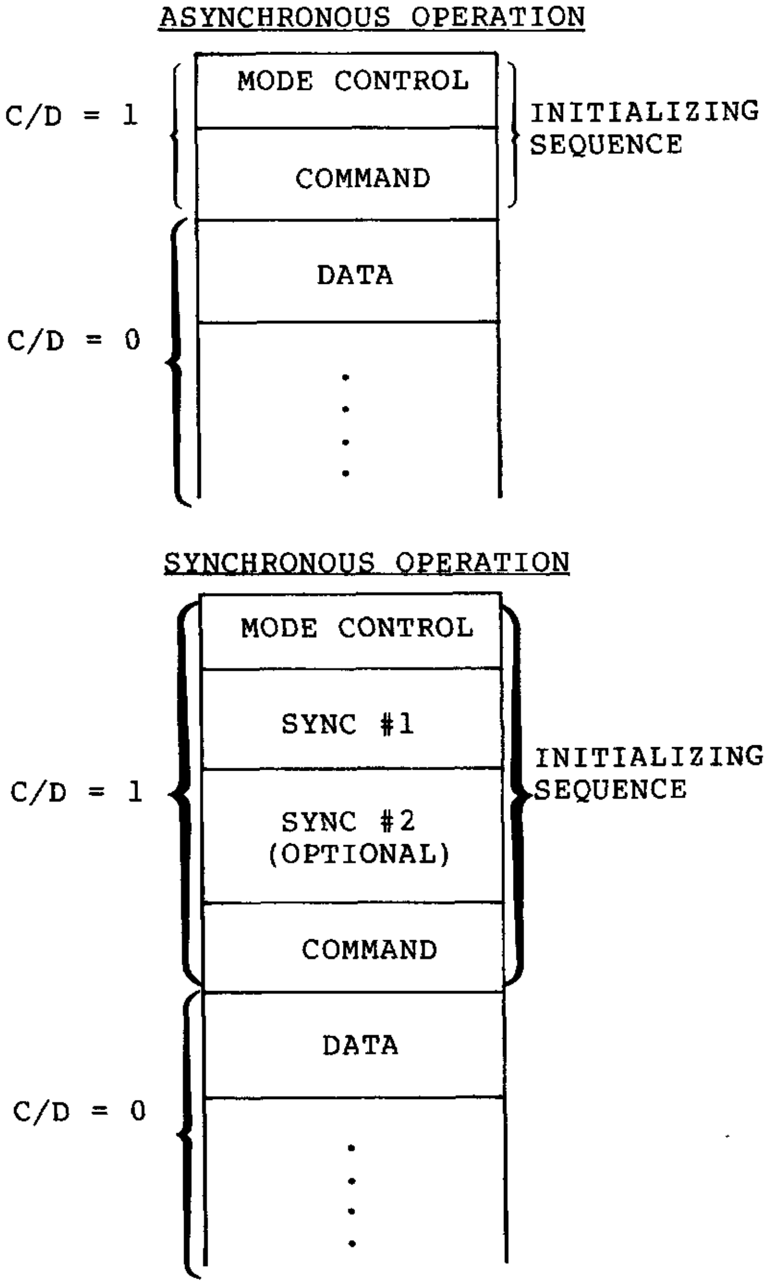


FIGURE 3.6.2.1: Control Word Sequence for Initialization

Only a single address is set aside for mode control bytes, command bytes, and sync character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as sync characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following an external reset signal or following an internal reset command.

Mode Control Codes

The USART interprets mode control codes as illustrated in Figures 3.6.2.2 and 3.6.2.3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between the data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus, in synchronous mode, a character will consist of five, six, seven, or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven, or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1 1/2, or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1 1/2 stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When syndet is an output, internal synchronization is specified; one or two sync characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

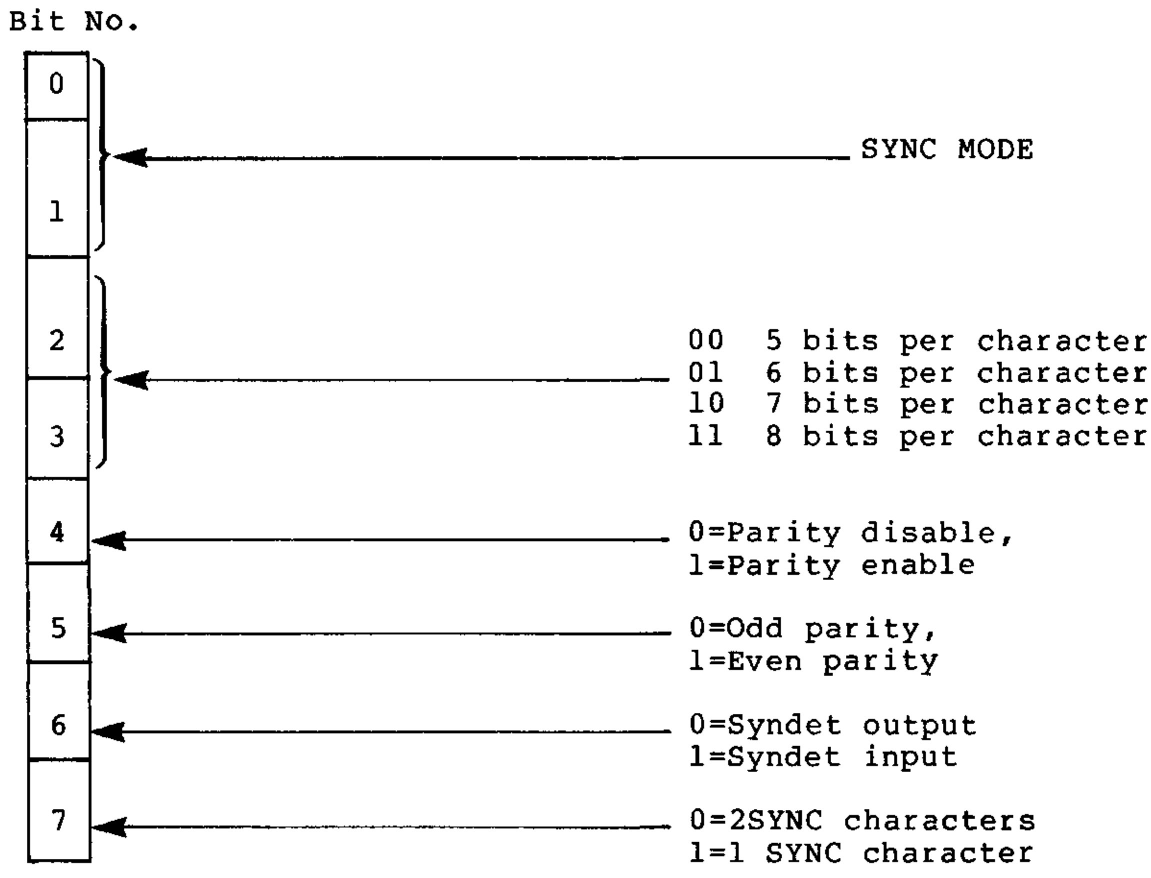


Figure 3.6.2.2: Synchronous Mode Control Codes

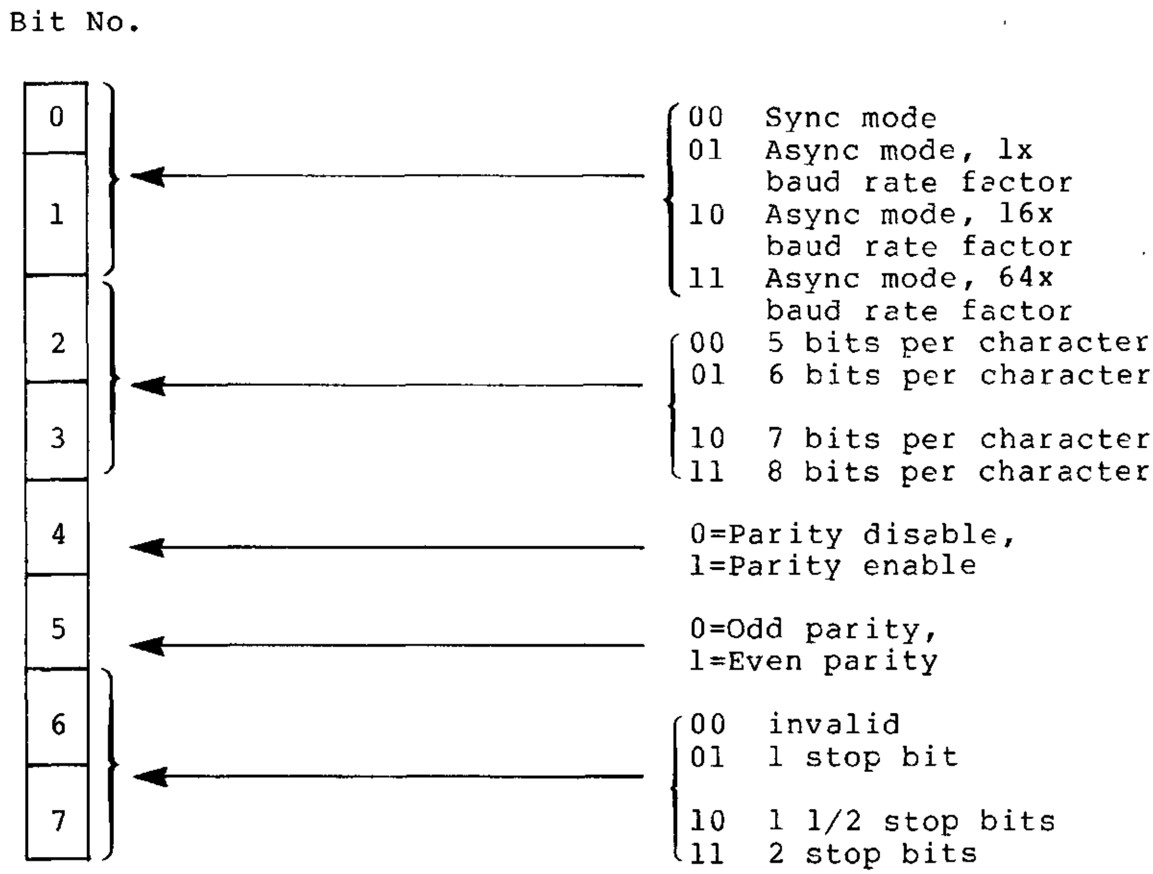


Figure 3.6.2.3: Asynchronous Mode Control Code

Mode Instruction Definition

The USART can operate in either asynchronous or synchronous communication modes. Understanding how the mode instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

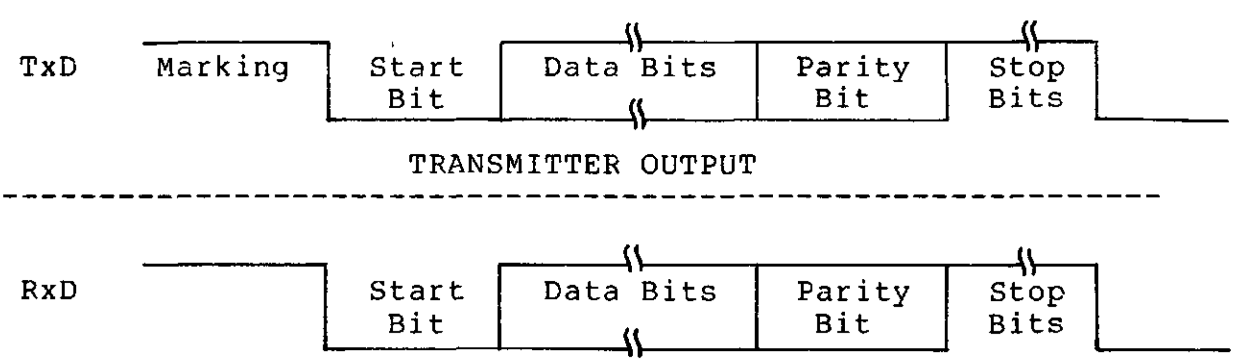
Asynchronous Mode

When a data character is written into the USART, it automatically adds a start bit (low level or "space") and the number of stop bits (high level or "mark") specified by the mode instruction. If parity has been enabled, an odd or even parity bit is inserted just before the stop bit(s), as specified by the mode instruction. Then, if CTS- and TxEN are active, the character is transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of TxC- at TxC-, TxC/16- or TxC-/64, as defined by the mode instruction.

If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the start bit of the next character provided by the processor. TxD may be forced to send a break (continuously low) by setting the correct bit in the command instruction.

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a start bit and a new character. The start bit is checked by testing for a "low" at its nominal center and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and stop bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of RxC-. If a high is not detected for the stop bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid stop bit, the input character is loaded into the parallel data bus buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the command instruction. Error flag conditions will not stop subsequent USART operation.

TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



RECEIVER INPUT

CPU BYTE (5-8 Bits/Char)

Data Character

ASSEMBLED SERIAL DATA OUTPUT (TxD)

Start Bit	Data Character	Parity Bit	Stop Bits

TRANSMISSION FORMAT

SERIAL DATA INPUT (RxD)

Start Bit	Data Character	Parity Bits	Stop Bits

CPU BYTE (5-8 bits/char)*

Data Character

* If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero"

RECEIVE FORMAT

Synchronous Transmission

As in asynchronous transmission, the TxD output remains "high" (marking) until the uPD8251 receives the first character from the processor which is usually a sync character. After a command instruction has set TxEN and after clear to send (CTS-) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of TxC- and the same rate as TxC-.

Once transmission has started, synchonronus mode format requires that the serial data stream at TxD continue at the TxC- rate or sync will be lost. If a data character is not provided by the processor before the uPD8251 transmitter buffer becomes empty, the sync character(s) loaded directly following the mode instruction will be automatically inserted in the TxD data stream. The sync character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the USART becomes empty, and must send the sync character(s), the TxEMPTY output is raised to signal the processor that the transmitter buffer is empty and sync characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

Synchronous Receive

In synchronous receive, character synchronization can be either external or internal. If the internal sync mode has been selected, and the enable hunt (EH) bit has been set by a command instruction, the receiver goes into the hunt mode.

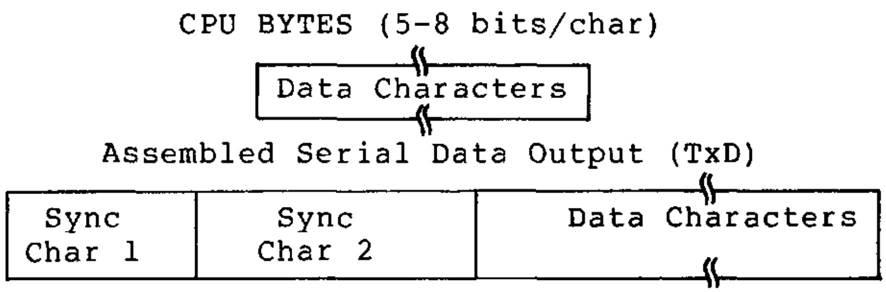
Incoming data on the RxD input is sampled on the rising edge of RxC-, and the receiver buffer is compared with the first sync character after each bit has been loaded until a match is found. If two sync characters have been programmed, the next received character is also compared. When the sync character(s) programmed have been detected, the USART leaves the hunt mode and is in character synchronization. At this time, the syndet (output) is set high. Syndet is automatically reset by a status read.

If external sync has been specified in the mode instruction, a "one" applied to the syndet (input) for at least one RxC-cycle will synchronize the USART.

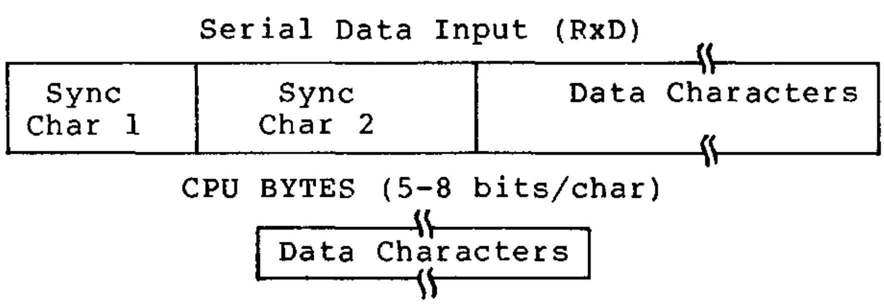
Parity and overrun errors are treated the same in the synchronous as in the asynchronous mode. Framing errors do not apply in the synchronous format.

The processor may command the receiver to enter the hunt mode with a command instruction which sets enable hunt (EH) if synchronization is lost.

TRANSMIT/RECEIVER FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Command Words

Command words are used to initiate specific functions within the USART, such as, "reset all error flags" or "start searching for sync". Consequently, command words may be issued by the microprocessor to the USART at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

A reset operation (internal via CMD IR or external via the reset input) will cause the USART to interpret the next "control write", which must immediately follow the reset, as a mode instruction. Following the mode instruction, a command word, of the format shown in FIG 3.6.2.5, is issued to the USART.

Bit No.	
0	TxEN 1=Enable tranmission 0=Disable transmission
1	DTR 1=DTR- output is forced to 0
2	RxE 1=Enable RxRDY 0=Disable RxRDY
3	SBRK 1=TxD is forced low 0=Normal operation
4	ER 1=Resets all error flags in status register (PE,OE,FE)
5	RTS 1=RTS- output is forced to 0
6	IR 1=Reset format
7	EH 1=Enter hunt mode

Figure 3.6.2.5: USART Control Command

Bit 0 of the command word is the transmit enable bit (TxEN). Data transmission from the USART cannot take place unless TxEN is set in the command register. Figure 5 defines the way in which TxEN, TxE, and TxRDY combine to control transmitter operations.

Bit 1 is the data terminal ready (DTR) bit. When the DTR command bit is set, the DTR- output connection is active (low). DTR is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the receiver enable command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the receive character buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the receiver character buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

TxEN	TxE	TxRDY	
1	1	1	Transmit output register and transmit character buffer empty. TxD continues to mark if USART is in the asynchronous mode. TxD will send sync pattern if USART is in the synchronous mode. Data can be entered into buffer.
1	0	1	Transmit output register is shifting a character. Transmit character buffer is available to receive a new byte from the processor.
1	1	0	Transmit register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit register is currently sending and an additional character is stored in the transmit character buffer for transmission.
0	X	X	Transmitter is disabled.

Figure 3.6.2.5. Operation of the Transmitter Section as a Function of TxE, TxRDY, and TxEN.

Bit 3 is the send break command bit (SBRK). When SBRK is set, the transmitter ouput (TxD) is interrupted and a continuous binary "0" level (spacing), is applied to the TxD output signal. The break will continue until a subsequent command word is sent to the USART to remove SBRK.

Bit 4 is the error reset bit (ER). When a command word is transmitted with the ER bit set, all three error flags in the status register are reset. Error reset occurs when the command word is loaded into the USART. No latch is provided in the command register to save the ER command bit.

Bit 5, the request to send command bit (RTS), sets a latch to reflect the RTS signal level. The output of this latch is created independently of other signals in the USART. As a result, data transfers may be made by the microprocessor to the transmit register, and data may be actively transmitted to the communication line through TxD regardless of the status of RTS.

Bit 6, the internal reset (IR), causes the USART to return to the idle mode. All functions within the USART cease, and no new operation can be resumed until the circuit is reinitiallized. If the operating mode is to be altered during the execution of a microprocessor program, the USART must first be reset. Either the external reset connection can be activated, or the internal reset command can be sent to the USART. Internal reset is a momentary function performed only when the command is used.

Bit 7 is the enter hunt command bit (EH). The enter hunt mode command is only effective for the USART when it is operating in the synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "enter hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent command word is sent, when the IR command is sent to the USART, or when sync characters are recognized.

Status Read Format

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The USART has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the C/D- input "high" to obtain device status information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both polled and interrupt driven environments.

Bit No.

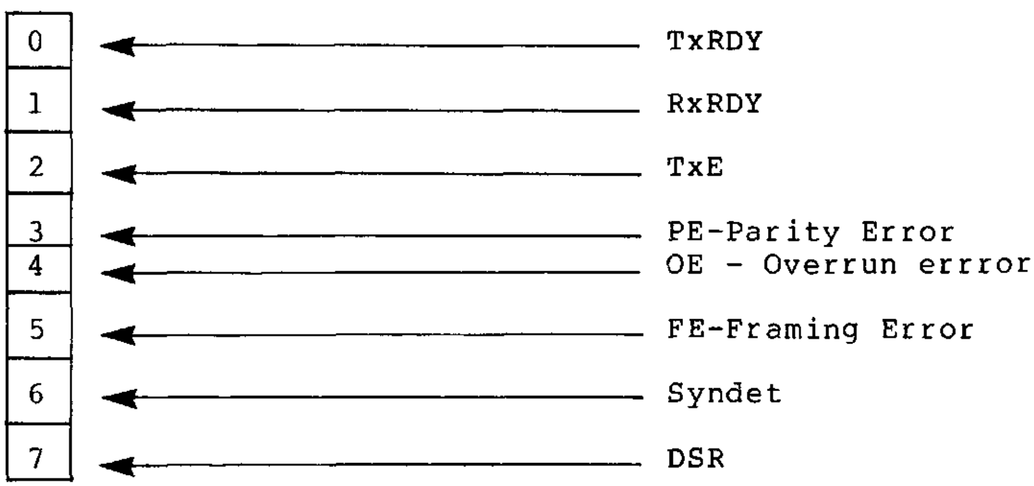


Figure 3.6.2 6: The USART Status Registeer

TxRDY signals the processor that the transmit character buffer is empty and that the USART can accept a new character for transmission.

RxRDY signals the processor that a completed character is holding in the receive character buffer register for transfer to the processor.

TxE signals the processor that the transmit register is empty.

PE is the parity error signal indicating to the CPU that the character stored in the receive character buffer was received with an incorrect number of binary "1" bits. The PE flag is cleared by setting the ER bit in a subsequent command instruction. PE being set does not inhibit USART operation.

OE is the receiver overrun error. OE is set whenever a byte stored in the receiver character register is overwritten with a new byte before being transferred to the processor. The OE flag is cleared by setting the ER bit in a subsequent command instruction. OE being set does not inhibit USART operation.

FE is the character framing error which indicates that the asynchronous mode byte stored in the receiver character buffer was received with an incorrect character bit format (stop bit), as specified by the current mode. The FE flag is cleared by setting the ER bit in a subsequent command instruction. FE being set does not inhibit USART operation.

3.7 CTC Operation

3.7.1 CTC Pin Description

D7-D0

Z80-CPU Data Bus (bi-directional, tri-state)

This bus is used to transfer all data and command words between the Z80-CPU and the Z80-CTC. There are 8 bits on this bus, of which D0 is the least significant.

CS1,CS0

Channel Select (input, active high)

These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O write or read. (See truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

CE-

Chip Enable (input, active low)

A low level on this pin enables the CTC to accept control words, interrupt vectors, or time constant data words from the Z80 data bus during an I/O write cycle, or to transmit the contents of the down counter to the CPU during an I/O ready cycle. In most applications, this signal is decoded from the 8 least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter/timer channels.

Clock (phi)

System Clock (input)

This single-phase clock is used by the CTC to synchronize certain signals internally.

M1-

Machine Cycle One Signal from CPU (input, active low)

When M1- is active and the RD- signal is active, the CPU is fetching an instruction from memory. When M1- is active and the IORQ- signal is active, the CPU is acknowledging an interrupt, alerting the CTC to place an interrupt vector on the Z80 data bus if it has daisy chain priority and one of its channels has requested an interrupt.

IORQ-

Input/Output Request from CPU (input, active low)

The IORQ- signal is used in conjunction with the CE- and RD- signals to transfer data and channel control words between the Z80-CPU and the CTC. During a CTC write cycle, IORQ- and CE- must be true and RD- false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid RD- signal. In a CTC read cycle, IORQ-, CE-, and RD- must be active to place the contents of the down counter on the Z80 data bus. If IORQ- and M1- are both true, the CPU is acknowledging an interrupt request, and the highest-priority interrupting channel will place its interrupt vector on the Z80 data bus.

RD-

Read Cycle Status from the CPU (input, active low)

The RD- signal is used in conjunction with the IORQ- and CE- signals to transfer data and channel control words between the Z80-CPU and the CTC. During a CTC write cycle, IORQ- and CE- must be true and RD- false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid RD- signal. In a CTC read cycle, IORQ-, CE-, and RD- must be active to place the contents of the down counter on the Z80 data bus.

IEI

Interrupt Enable In (input, active high)

This signal is used to help form a system-wide interrupt daisy chain which establishes priorities when more than one peripheral device in the system has interrupting capability. A high level on this pin indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z80-CPU.

IEO

Interrupt Enable Out (output, active high)

The IEO signal, in conjunction with IEI, is used to form a system-wide interrupt priority daisy chain. IEO is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. Thus, this signal blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced by the CPU.

INT-

Interrupt Request (output, open drain, active low)

This signal goes true when any CTC channel which has been programmed to enable interrupts has a zero-count condition in its down counter.

RESET-

Reset (input, active low)

This signal stops all channels from counting and resets channel interrupt enable bits in all control registers, thereby disabling CTC-generated interrupts. The ZC/TO and INT- outputs go to their inactive states, IEO reflects IEI, and the CTC's data bus output drivers go to the high impedance state.

CLK/TRG3-CLK/TRG0

External Clock/Timer Trigger (input, user-selectable active high or low)

There are four CLK/TRG pins, corresponding to the four independent CTC channels. In the counter mode, every active edge on this pin decrements the down counter. In the timer mode, an active edge on this pin initiates the timing function. The user may select the active edge to be either rising or falling.

ZC/TO2-C/TO0

Zero Count/Timeout (output, active high)

There are three ZC/TO pins, corresponding to CTC channels 2 through 0. (Due to package pin limitations, channel 3 has no ZC/TO pin.) In either counter mode or timer mode, when the down counter decrements to zero, an active high going pulse appears at this pin.

3.7.2 CTC Programming

Before a Z80-CTC channel can begin counting or timing operations, a channel control word and a time constant data word must be written to it by the CPU. These words will be stored in the channel control register and the time constant register of that channel. In addition, if any of the four channels have been programmed with bit 7 of their channel control words to enable interrupts, an interrupt vector must be written to the appropriate register in the CTC. Due to automatic features in the interrupt control logic, one pre-programmed interrupt vector suffices for all four channels.

Loading the Channel Control Register

To load a channel control word, the CPU performs a normal I/O write sequence to the port address corresponding to the CTC channel. Two CTC input pins, namely CS0 and CS1, are used to form a 2-bit binary address to select one of four channels within the device. In many system architectures, these two input pins are connected to address bus lines A0 and A1, respectively, so that the four channels in a CTC device will occupy contiguous I/O port addresses. A word written to a CTC channel will be interpreted as a channel control word, and loaded into the channel control register, with bit 0 being a logic 1. The other seven bits of this word select operating modes and conditions as indicated in the diagram below. Following the diagram, the meaning of each bit will be discussed in detail.

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Enable	Mode	Range*	Slope	Trigger*	Load Time Constant	Reset	1

* Used in Timer Mode only

Bit 7=1

The channel is enabled to generate an interrupt request sequence every time the down counter reaches a zero-count condition. To set this bit to 1 in any of the four channel control registers necessitates that an interrupt vector also be written to the CTC before operation begins. Channel interrupts may be programmed in either counter mode or timer mode. If an updated channel control word is written to a channel already in operation with bit 7 set, the interrupt enable selection will not be retroactive to a preceding zero-count condition.

Bit 7=0

Channel interrupts disabled.

Bit 6=1

Counter mode selected. The down counter is decremented by each triggering edge of the external clock (CLK/TRG) input. The prescaler is not used.

Bit 6=0

Timer mode selected. The prescaler is clocked by the system clock , and the output of the prescaler in turn, clocks the down counter. The output of the down counter (the channel's ZC/TO output) is a uniform pulse train of periods given by the product

t * P * TC

where t is the period of system clock , P is the prescaler factor of 16 or 256, and TC is the time constant data word.

Bit 5=1

(Defined for timer mode only.) Prescaler factor is 256.

Bit 5=0

(Defined for timer mode only.) Prescaler factor is 16.

Bit 4=1

Timer mode - positive edge trigger starts timer operation. Counter mode - positive edge decrements the down counter.

Bit 4=0

Timer mode - negative edge trigger starts timer operation. Counter mode - negative edge decrements the down counter.

Bit 3=1

Timer mode only - external trigger is valid for starting timer operation after rising edge of T of the machine cycle following the one that loads the time constant. The prescaler is decremented two clock cycles later if the setup time is met, otherwise, three clock cycles.

Bit 3=0

Timer mode only - timer begins operation on the rising edge of T of the machine cycle following the one that loads the time constant.

Bit 2=1

The time constant data word for the time constant register will be the next word written to this channel. If an updated channel control word and time constant data word are written to a channel while it is already in operation, the down counter will continue decrementing to zero before the new time constant is loaded into it.

Bit 2=0

No time constant data word for the time constant register should be expected to follow. To program bit 2 to this state implies that this channel control word is intended to update the status of a channel already in operation, since a channel will not operate without a correctly programmed data word in the time constant register, and a set bit 2 in this channel control word provides the only way of writing to the time constant register.

Bit 1=1

Reset channel. Channel stops counting or timing. This is not a stored condition. Upon writing into this bit, a reset pulse discontinues current channel operation, however, none of the bits in the channel control register are changed. If both bit 2=1 and bit 1=1, the channel will resume operation upon loading a time constant.

Bit 1=0

Channel continues current operation.

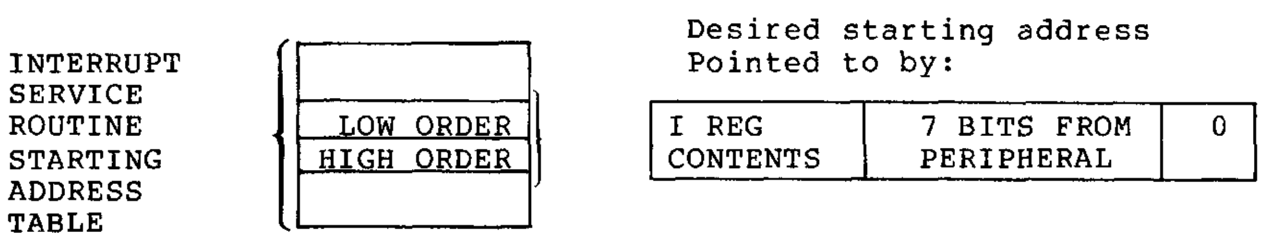
A channel may not begin operation in either timer mode or counter mode unless a time constant data word is written into the time constant register by the CPU. This data word will be expected on the next I/O write to this channel following the I/O write of the channel control word, provided bit 2 of the channel control word is set. The time constant data word may be any integer value in the range 1-256. If all eight bits in this word are zero, it is interpreted as 256. If a time constant data word is loaded to a channel already in operation, the down counter will continue decrementing to zero before the new time constant is loaded from the time constant register to the down counter.

Time Constant Register

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC2	TC0
MSB							LSB

The Z80-CTC has been designed to operate with the Z80-CPU programmed for mode 2 interrupt response. Under the requirements of this mode, when a CTC channel requests an interrupt and is acknowledged, a 16-bit pointer must be formed to obtain a corresponding interrupt service routine starting address from a table in memory. The upper 8 bits of this pointer are provided by the CPU's I register, and the lower 8 bits of the pointer are provided by the CTC in the form of an interrupt vector unique to the particular channel that requested the interrupt.

MODE 2 INTERRUPT OPERATION



The high order 5 bits of this interrupt vector must be written to the CTC in advance as part of the initial programming sequence. To do so, the CPU must write to the I/O port addresses corresponding to the CTC channel 0, just as it would if a channel control word were being written to that channel, except that bit 0 of the word being written must contain a 0. (As explained above in Section 3.1, if bit 0 of a word written to a channel were set to 2, the word would be interpreted as a channel control word, so a 0 in bit 0 signals the CTC to load the incoming word into the interrupt vector register.) Bits 1 and 2, however, are not used when loading this vector. At the time when the interrupting channel must place the interrupt vector on the Z80 data bus, the interrupt control logic of the CTC automatically supplies a binary code in bits 1 and 2 identifying which of the four CTC channels is to be serviced.

INTERRUPT VECTOR REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	X	X	0

D7–D3: Supplied by User

D2	D1	
0	0	Channel 0 (highest priority)
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3 (lowest priority)

D2–D0: Automatically inserted by Z80-CTC

4.0 PROGRAMMING AND INITIALIZATION

4.1 Initialization

This section describes the programming techniques for the Serial Interface Board (SIB). It is assumed that the board has been correctly installed and that all necessary jumpers have been connected. Before any data can be transmitted or received, the SIB must be initialized. The SIB is intended to be interrupt driven, in which case the CTC interrupts must be enabled and interrupt handlers must be coded.

4.1.1 Disabling Interrupts

It is important, especially during program development, to start any program by disabling all of the CTC interrupt generators (CTC 1 and 2). This may not need to be done if the previously run program terminated normally and disabled the CTC, and if the USART is enabled and cleared before interrupts are re-enabled. Programming the USART with interrupts enabled can often cause spurious interrupts during the enabling process.

The following routine stops all four channels of both CTCs involved in interrupt triggering. The CTC command byte has the stop operation bit set and the interrupt enable bit reset (see Z80-CTC Product Specification).

Clear All CTCs - Interrupt Off

```
CLCTCS    LD      B,4           ; DO RECEIVER CHANNELS
          LD      C,CTC1
          LD      A,OFFMOD
CLLP1     OUT     (C),A
          INC     C
          DJNZ    CLLP1
          LD      B,4           ; AND TRANSMITTER CHANNELS
          LD      C,CTC2
          LD      A,OFFMOD
CLLP2     OUT     (C),A
          INC     C
          DJNZ    CLLP2
          RET
;-------------
OFFMOD    EQU     43H           ; NO INTS AND STOPPED
```

4.1.2 Enabling USARTs

Enabling the USART requires careful attention. It should be enabled before the baud rate generator is turned on since its initial state is indeterminate and it may try to transmit a character or cause an interrupt. The process involves four steps which should proceed in the following order:

a. Reset the USART;
b. Send a mode byte (see 8251 Product Spec.) to the control port;
c. Send a command byte to the control port; and
d. Read one character from the data port (the data port address is one less than the control port address by convention).

A USART may be reset by sending three zero bytes followed by a reset command (40H). The zero bytes are recommended since the USART may have been in the synchronous mode, and therefore, would have interpreted the first two characters as sync characters. USART application information suggests that sending three reset commands will cause a reset, thus, enabling the USART to receive a mode byte. Since the MCZ System reset button is connected to the USART's external reset pin, pushing the system reset followed by three internal reset commands will not cause the USART to accept a mode byte, but rather cause the USART to treat the intended mode byte as a commmand byte.

The next byte sent to the USART must be a mode byte. The value 8EH sets the mode to 1.5 stop bits, no parity, eight bit characters, and a 16x baud rate factor. The mode byte must be followed by a command byte. The value 37H enables the USART for both transmitting and receiving. Request to Send (RTS) (bit 5) and Data Terminal Ready (DTR) (bit 1) should be turned on since USARTs and most modems only work if Clear to Send (CTS) is low, and one of these pins will be connected to CTS. One character must be read from the USART data port to clear the receiver data buffer. The routine should look like:

RESET AND INITIALIZE ALL FOUR USARTS

```
USART      LD      C,USART0+1    ;LOWEST PORT - CONTROL
           LD      B,4
UL01       LD      A,0
           OUT     (C),A         ; THREE INTERNAL RESETS-EXT RESET
           OUT     (C),A
           OUT     (C),A
           LD      A,RESCOM
           OUT     (C),A
           LD      A,SIBMOD      ; SET UP TESTING MODE
           OUT     (C),A
           LD      A,SIBCOM      ; AND ENABLE BOTH TR AND RCV
           OUT     (C),A
           DEC     C
           IN      A,(C)         ; CLEAR OUT RECEIVER BUFFER
           INC     C
           INC     C
           INC     C
           DJNZ    UL01
           RET
;-------------------------------
RESCOM     EQU     40H           ; RESET USART TO ACCEPT
                                   MODE BYTE
SIBMOD     EQU     8EH           ; 8 BIT ASYNCHRONOUS
SIBCOM     EQU     37H           ; TRANSMIT AND RECEIVE-
                                   ERROR RESET
```

4.1.3 Baud Rate Generation

The SIB will not function unless the three baud rate generators are running (actually only the baud rates connected to the channels in use must be functioning). The first three channels of CTC 0 are used to generate baud rates. There are three possible clock inputs to the baud rate CTC: 1/2 phi from the MCB, 1/2 phi from the SIB, and 1/32 phi from the SIB. Jumper connections at J3 determine which of these clocks are input to the CTC when in the counter mode. In the timer mode, the system clock is used as a time base. Jumper connections at J2 determine which CTC outputs drive each of the USART transmit and receive clocks. The CTCs may be programmed to operate in either the counter mode (47H) or the timer mode (07H) (see Z80-CTC Product Spec.). The following routine will generate one baud clock in the timer mode and two others in the counter mode:

```
        SET UP CTC0 TO GENERATE THE THREE BAUD RATES

BAUDR   LD      A,CNTMOD      ; CHAN 0 IN COUNTER MODE
        OUT     (CTC0),A
        LD      A,RATE0       ; WITH TIME CONSTANT=RATE0
        OUT     (CTC0),A
        LD      A,CNTMOD      ; CHAN 1 IN COUNTER MODE
        OUT     (CTC0+1),A
        LD      A,RATE1       ; WITH TIME CONSTANT=RATE1
        OUT     (CTC0+1),A
        LD      A,TIMMOD      ; CHAN 2 IN TIMER MODE
        OUT     (CTC0+2),A
        LD      A,RATE2       ; WITH TIME CONSTANT=RATE2
        OUT     (CTC0+2),A
        RET                   ; CAN'T USE FOURTH CHANNEL
                                FOR BAUD RATE
;---------------------------

; THE FOLLOWING BAUD RATES ASSUME THAT THE USARTS HAVE BEEN
; PROGRAMMED FOR A X16 BAUD CLOCK.
;
CNTMOD  EQU     47H           ; COUNTER MODE
TIMMOD  EQU     07H           ; TIMER MODE WITH PRESCALER=16
RATE0   EQU     16            ; PHI/2 CLOCK IN CNT
                                MODE=2400 BAUD
RATE1   EQU     08            ; PHI/32 CLOCK IN CNT
                                MODE=300 BAUD
RATE2   EQU     04            ; IN TIMER MODE=1200 BAUD
```

4.1.4 CTC Interrupt Handling

The SIB should be used in interrupt mode 2 (see Z80-CPU Reference Manual). It is possible to use mode 0, but since MCZ system software uses mode 2, running in mode 0 is difficult. MCZ software expects the I register (interrupt page pointer) to be set to 13H. It is best to also put the SIB interrupt vectors into this page since it allows program development using MCZ system software. The last half of page 13 is reserved for MCZ vectors (1380-13FF) but the lower half (1300-137F) is unused. The interrupt vector is set up by copying the interrupt handler addresses for each of the four channels of a CTC into a contiguous 8-byte area in the free part of page 13H. The CTC interrupt address must be set to the offset of the vector within that page. The following routine sets up the interrupt vectors and enables the CTCs (the interrupt addresses are assumed to be at location IOVEC with the receive interrupt handler pointers preceding the transmit interrupt handler pointers):

```
            SET UP CTC1 AND CTC2 INTERRUPT VECTORS
            FOR USARTS     WARNING - 3KMON USE OF
            00-0F IN PAGE WILL DESTROY THIS PROG

SETIVC      LD        HL,IOVEC     ; COPY INTERRUPT HANDLER ADDRESSES
            LD        A,I          ; GET PAGE ADDR
            LD        D,A
            LD        E,00H        ; PLACE TO PUT ADDRS
            LD        BC,16        ; 8 CHANNNELS-2 PER USART
            LDIR
            LD        A,00H        ; USES UNUSED 3K MON INT PAGE SPACE
            OUT       (CTC1),A     ; USART RECEIVER VECTOR
            LD        A,08H
            OUT       (CTC2),A    ; TRANSMIT VECTOR (4 CHANNELS/CTC)
```

The final step in initializing the SIB involves actually enabling CTC 1 and CTC 2 to generate interrupts when a character has been received or when the USART is ready to transmit a character. The CTC is enabled by sending a command byte to the desired channel with the interrupt enable bit on, counter mode enabled, the slope bit on for positive triggering, the load time constant bit on, and the stop until time constant loaded bit on. The command value is 0D7H (see Z80-CTC Product Spec.). Both the receive interrupt, which occurs when RxRDY goes high, and the transmit interrupt, which occurs when TxRDY goes high, must be triggered by a positive slope. The command byte is followed by a counter value of 1, causing an interrupt to occur on every character. channel before data transmission begins, and for every CTC interrupt which occurs thereafter:

```
            SET UP A CTC TO INTERRUPT (PORT IN C)

SETINT      LD        A,INTMP      ; SET UP CTC MODE
            OUT       (C),A
            LD        A,1          ; INTERRUPT ON EVERY CHAR
            OUT       (C),A
            RET
;----------------------------------------------------
INTMP       EQU       0D7H         ; EI,CNT MOD, POS SLOPE
                                     TRIGGER,LD CONST, STOP
```

4.2 Transmitting and Receiving Characters

Actual character transmission and reception may begin once the SIB has been initialized. A character is transmitted by writing it to the given USART's data port. When the USART is ready to accept another character for transmission, the TxRDY bit in the status byte comes on. TxRDY is also connected to the transmit interrupt CTC, causing an interrupt to occur whenever the USART is ready to accept another character. Normally, the transmit interrupt handler does the actual transmission and checks if there are any more characters to send.

Whenever a given USART receives a character, the RxRDY status bit comes on. Since RxRDY is connected to the receive interrupt CTC, the interrupt occurs whenever a character is ready to be read by the Z80. After reading a character, the 3 error bits in the status byte should be checked. If an error occurs, an error routine should be called. To restart, a command byte with the error reset bit (bit 4) turned on should be sent, followed by the original command to put the USART back into its state previous to the error. If the USART is run with the error reset bit turned on and if the data character is read before the status, no error will ever be detected since the data read will always reset any errors.

4.3 Writing Interrupt Handlers

Interrupt handlers will differ depending on the intended application, but there are a few general principles which should be understood. The Z80 peripheral device family uses a hardwired daisy chain interrupt priority scheme. In the chain, the SIB has a priority which is determined by the backplane connections of IEI and IEO. Within the SIB, each CTC is ordered by channel number (lowest number has highest priority) with receive interrupts (CTC 1) having higher priority than transmit interrupts (CTC 2). When an interrupt occurs, it disables further interrupts and disconnects the daisy chain. An interrupt service routine must terminate by enabling interrupts and issuing a RETI instruction which reconnects the daisy chain. After the RETI has been executed, the highest priority pending interrupt will be recognized.

The receive interrupt handler for a given SIB channel needs to read a character and check the USART's status. Inputting a character from a USART turns RxRDY off and allows it to trigger an interrupt the next time a character arrives. As a general rule, and especially while running at high data rates, the part of the interrupt handler which executes with interrupts disabled should be as short as possible. If more processing is required, the interrupt handler should set a flag which will indicate to a routine executing with interrupts enabled to complete the processing. The interrupt CTC must be reloaded after each interrupt.

The transmit interrupt handler needs to determine if there are more characters to send, and if there are, transmits them. When the USART is ready to accept another character for transmission (not finished transmitting the previous character), it turns the TxRDY bit on and causes an interrupt (if interrupts are enabled). Since USARTs are double buffered, if the USART is completely empty, the TxRDY interrupt will occur immediately (as soon as the character has been moved to the transmit buffer) inside the interrupt handler. When the handler is ended with a RETI, the pending interrupt will be lost. The RETI instruction causes any pending interrupts on the channel being serviced to be reset, but all pending interrupts on other channels will not be reset. An easy method of handling this problem is to read the USART's status byte immediately before returning from the interrupt handler. The routine needs to check if the TxRDY bit has come on. If it has, jump to the beginning of the handler and repeat it as if the interrupt had occurred. Notice that this jump can never be taken more than once per interrupt handler entry and normally will only occur the very first time the interrupt occurs. There must be some delay before testing the TxRDY status bit after outputting a character or the TxRDY bit will not have had time to be turned off by the transmission. The delay should be on the order of 40 t states for a 2.4 MHz machine.

BLANK

5.0 TECHNICAL DESCRIPTION

5.1 Description

Sheet 1

Sheet 1 contains the buffers for the Z80 control signals and address lines used by the SIB. The data bus buffers for the least significant four bits of the Z80 data bus are also shown. The outputs of decoder A3 are used to decode the chip selects for the four USARTs.

Sheet 2

The CTC which generates the transmit and receive clocks for the USARTs is shown on Sheet 2. The CTC may be programmed to operate in either the timer mode or counter mode. Jumper J3 is strapped to select the external time base clocks when operating in the counter mode. The zero count/timeout outputs are divided by 2 to produce 50% duty cycle clocks which are required by the USARTs. The +12V and -10V power supply voltages needed by the EIA interface are produced by the TL-497 switching regulator.

Sheet 3

Sheet 3 contains the buffers for the most significant four bits of the data bus, and the control PROM which determines the direction of the data bus buffers. The bit map of the control PROM is shown in Figure 6.1.1. The SIB I/O port addresses are decoded by A27. Jumper J4 is strapped to select one of eight 32-port address segments. The outputs of A27 (GP0- to GP7-) each represent four I/O ports within the 32-port segment selected by J4. Jumper J1 selects which four port address segments correspond to the various CTC and USART I/O ports (GPM- to GPT-).

FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF
FEFEFFFF	FEFEFFFF	FEFEFFFF	FEFEFFFF
FEFEFFFF	FEFEFFFF	FEFEFFFF	FEFEFFFF
FEFEFFFF	FEFEFFFF	FEFEFFFF	FEFEFFFF
FEFEFFFF	FEFEFFFF	FEFEFFFF	FEFEFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FEFFFFFF
FEFFFFFF	FEFFFFFF	FEFFFFFF	FFFFFFFF

TABLE 5.1.1: Data Bus Control PROM (A14) Bit Map

Sheet 4

Sheet 4 contains the two CTC's which generate interrupts for the USART transmitter ready and receiver ready signals. The receiver ready signals have interrupt priority over the transmitter ready signals. The interrupt modes and vectors are software-programmble in the CTC's.

Sheets 5, 6, 7, 8

Sheets 5, 6, 7, and 8 show the four USARTs and their associated I/O buffers and jumper areas. USARTs 0, 1, and 2 are configured as RS232 interfaces while USART 3 may be either an RS232 or 20mA current-loop interface. The transmit and receive clocks are strapped at J2 and may be generated externally or by CTC 0.

Sheet 9

Sheet 9 contains the on-board oscillator and divider counters which produce clocks for the CTC USART clock generator (Sheet 2). External RS232-level clocks are buffered by A43 and are made available to the USARTs at Jumper J2.

5.2 SIB Specifications

SERIAL I/O:
Four serial input and four serial output channels

SERIAL MODES:
Synchronous or asynchronous using virtually any serial protocol.

SERIAL INTERFACE:

CHANNEL	INTERFACE
0	RS232
1	RS232
2	RS232
3	RS232 OR 20MA current loop

CONTROL INTERFACE:
TTL interface with MCZ series data, address, and control signals.

I/O PORT ADDRESSING:
20 jumper selectable I/O ports.

ELECTICAL SPECIFICATIONS:

+5 VDC +/-5%

Maximum Current = 1.5 amps

CONNECTOR:

122-pin edge (100 mil spacing)

PHYSICAL CHARACTERISTICS:

Length: 7.7 in/19.7 cm

Depth: 7.5 in/19.1 cm

Thickness: .062 in/0.16 cm

Spacing Between Cards: 0.5 in/1.27 cm centers

Maximum Component Height: 0.4 in/102 cm

Etch Layers: Two

ENVIRONMENT:

0 to 50 degrees centigrade.

6.0 DRAWINGS

6.1 Standard Carrier Configuration

```
33-0173-12 16-pin carrier, SIB, labelled J1-12
Wired as follows:
J1-01 to J1-12    PORTS 80-83 (CTC0)
J1-02 to J1-11    PORTS 84-87 (CTC1)
J1-03 to J1-10    PORTS 88-8B (CTC2)
J1-04 to J1-14    PORTS 8C-8F (USARTS 0,1)
J1-05 to J1-13    PORTS 90-93 (USARTS 2,3)

33-0173-13 16-pin carrier, SIB, labelled J2-13
Wired as follows:
J2-01 to J2-16    TxC3-TxC2
J2-16 to J2-15    TxC2-RxC2
J2-15 to J2-04    RxC2-CTC CLK2
J2-04 to J2-12    CTC CLK2-RxC3
J2-02 to J2-14    CTC CLK0-TxC0
J2-14 to J2-13    TxC0-RxC0
J2-03 to J2-05    CTC CLK1-RxC1
J2-05 to J2-06    RxC1-TxC1

33-0173-14 16-pin carrier, SIB, labelled J3-14
Wired as follows:
J3-04 to J3-11    MCB PHI/2-CK/T0
J3-05 to J3-13    PHI/32-CK/T2
J3-06 to J3-12    PHI/2-CK/T1

33-0173-15 16-pin carrier, SIB, labelled J4-15
Wired as follows:
J4-01 to J4-07    PORTS 80-9F
J4-04 to J4-06
J4-05 to J4-16

33-0174-02 14-pin carrier, SIB, labelled J5-8/2
Wired as follows:
Pin 1 to Pin 14    TERMINAL MODE
Pin 2 to Pin 13
Pin 3 to Pin 12
Pin 4 to Pin 11
Pin 5 to Pin 10
Pin 6 to Pin 9
```

6.2 SIB Edge Connector Pin List

PINOUT FOR "SIB" BOARD - 09-0037-01
J=SIB

PIN #	SIGNAL NAME
001	(+5V).
002	(+5V).
003	(+5V).
004	IORQ-
005	DB5
006	CK/T3
007	IN2.(SERIAL CLOCK IN)
008	DB3
009	MASTER.RESET
010	.
011	.
012	DB6
013	DB0
014	.
015	.
016	.
017	.
018	.
019	.
020	.
021	SYNC2
022	.
023	WR-
024	.
025	20mA.DATA.RTN.1
026	AB7
027	.
028	TTY.TAPE.CNTRL.RTN.1
029	AB5
030	AB6
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.

PIN #	SIGNAL NAME
040	SPARE0
041	SPARE1
042	SPARE2
043	.
044	SYNC0
045	SYNC1
046	TRXD0
047	TDSR0
048	TCTS0
049	TRXD1
050	TDSR1
051	TCTS1
052	TRXD2
053	TDSR2
054	TCTS2
055	SYNC3
056	TRXD
057	TDSR
058	TCTS
059	(+5V).
060	(+5V).
061	(+5V).
062	(GND).
063	(GND).
064	(GND).
065	IN0.(SERIAL CLOCK IN)
066	IN1.(SERIAL CLOCK IN)
067	IN3.(SERIAL CLOCK IN)
068	DB4
069	[#IEI.SIB.CTC0]
070	.
071	DB2
072	.
073	DB7
074	.
075	DB1
076	.
077	.
078	IEO.SIB.CTC2
079	INT-
080	IEO.SIB.CTC0
081	[#IEI.SIB.CTC1]
082	TTY.TAPE.CNTRL
083	.
084	.
085	.

PIN #	SIGNAL NAME
086	1/2.PHI.(HALF SYSTEM CLOCK)
087	.
088	.
089	.
090	20mA.RECVR.1
091	.
092	20mA.DATA.1
093	.
094	.
095	.
096	.
097	.
098	AB4
099	PHI-.(SYSTEM CLOCK-)
100	AB3
101	AB2
102	AB1
103	AB0
104	SPARE3
105	20mA.REC.RTN.1
106	TTXD0
107	TRTS0
108	TDTR0
109	TTXD1
110	TRTS1
111	TDTR1
112	TTXD2
113	TRTS2
114	TDTR2
115	M1-
116	RD-
117	TTXD
118	TRTS
119	TDTR
120	(GND).
121	(GND).
122	(GND).

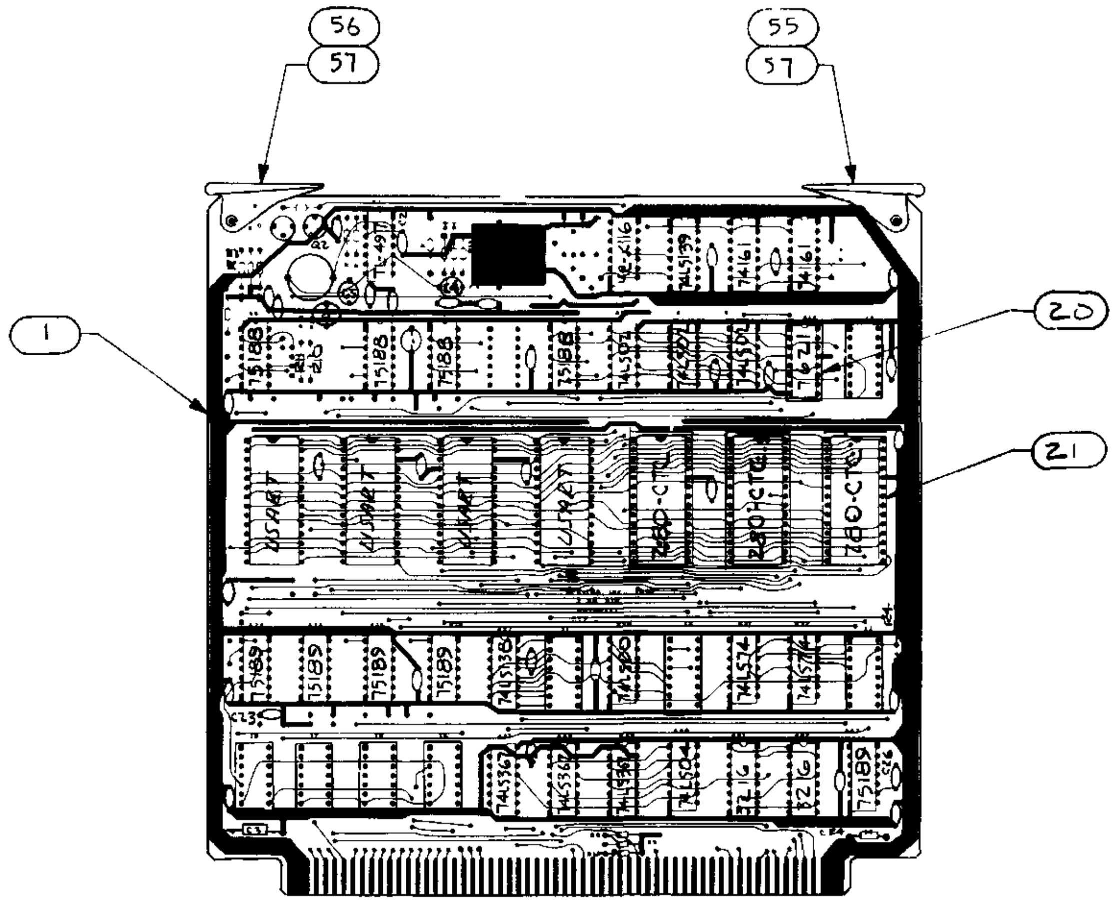
6.3 Parts List

1	LOGIC-DIAGRAM	DZ-0037-01	REF	
1A	TEST-SPEC,BOARD	FT-0037-01	REF	
1B	TEST-SPEC,SYSTEM	FT-0037-02	REF	
1C	PCB,BLANK,REV.B	10-0037-01	1	
2	I.C.,TL497	33-0075-01	1	A1
3	I.C.,MC-K116	33-0088-01	1	A2
4	I.C.,74LS139	33-0069-01	1	A3
5	I.C.,74161	33-0036-01	2	A4,5
6	I.C.,75188	33-0010-01	4	A6,7,8,10
7				
8	I.C.,774LS02	33-0046-01	3	A11,12,13
9	I.C.,PROM	33-0053-23	1	A14
10	I.C.,USART	33-0079-02	4	A16,17,18,19
11	I.C.,Z80-CTC	33-0078-01	3	A20,21,22
12	I.C.,75189	33-0011-01	5	A23,24,25,26,43
13	I.C.,74LS138	33-0068-01	1	A27
14	I.C.,74LS00	33-0058-01	1	A29
15	I.C.,74LS74	33-0066-01	2	A31,32
16	I.C.,74LS367	33-0055-01	3	A37,38,39
17	I.C.,74LS04	33-0059-01	1	A40
18	I.C.,3216	33-0089-01	2	A41,42
19	SOCKET,14-PIN	21-1000-06	4	J5-J8
20	SOCKET,16-PIN	21-1000-02	5	A14,J1-J4
21	SOCKET,28-PIN	21-1000-04	7	A16,17,18,19,20,21,22
22	CRYSTAL,19.668MHZ	23-0000-02	0	Y1 (NOT USED)
23				
24	RES,1/4W,5%,9.1K	47-1001-02	1	R2
25	RES,1/4,5%,1K	47-1000-63	3	R3,4,18
26	RES,1/4W,5%,51K	47-1001-20	1	R5
27	RES,1/4W,5%,2.4K	47-1000-72	1	R6
28	RES,1/4W,5%,220	47-1000-47	3	R7,8,9
29	RES,1/4W,5%,2.7K	47-1000-73	2	R10,11
30	RES,1/4W,5%,47	47-1000-31	2	R12,13
31	RES,1/4W,5%,27K	47-1001-13	0	R15 (NOT USED)
32	RES,1/4W,5%,360	47-1000-52	0	R16 (NOT USED)
33	RES,1/4W,5%,180	47-1000-45	0	R17 (NOT USED)
34	RES,1/4W,5%,18K	47-1001-09	0	R14 (NOT USED)
35	RES,1/2W,1%,1-OHM	47-3000-16	1	R1
36				
37				
38	CAP,150UF,15V,AXIAL	15-0003-36	2	C1,6
39	CAP,220PF	15-0000-15	1	C2
40	CAP,0.1UF,50V	15-0000-50	30	C27-56
41	CAP,22UF,16V,RADIAL	15-0003-24	2	C4,5
42	CAP,390PF,500V	15-0001-20	2	C23,26
43	CAP,22PF	15-0001-05	0	C24 (NOT USED)

44	CAP,68PF	15-0001-11	0	C25 (NOT USED)
45	CAP,22UF,16V	15-0003-25	1	C3
46	DIODE,1N914	48-1002-01	2	CR1,2
47	DIODE,1N5231B	48-1001-02	1	CR3
48	DIODE,1N4001	48-1000-01	1	CR4
49				
50	INDUUCTOR,0.27UH	15-9000-01	1	L1
51				
52	TRANSISTOR,2N2905	48-0001-01	2	Q1,2
53	TRANSISTOR,2N2907	48-0002-01	0	Q3 (NOT USED)
54				
55	EJECTOR,ENGRAVED	24-0000-03	1	
56	EJECTOR,BLANK	24-0001-01	1	
57	PIN,EJECTOR	91-3000-01	2	

6.4 ASSEMBLY DRAWINGS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	ECN 00126	11/14/7	A~
D	ECN 00170	12 13-77	A~
D1	RECORD CHANGE	1-6-78	A~
E	ECN 00189	1 23 78	A~
E1	RECORD CHANGE - ECR 246	2-16-78	A~
E2	RECORD CHANGE-ECR 274	3-7-78	A~



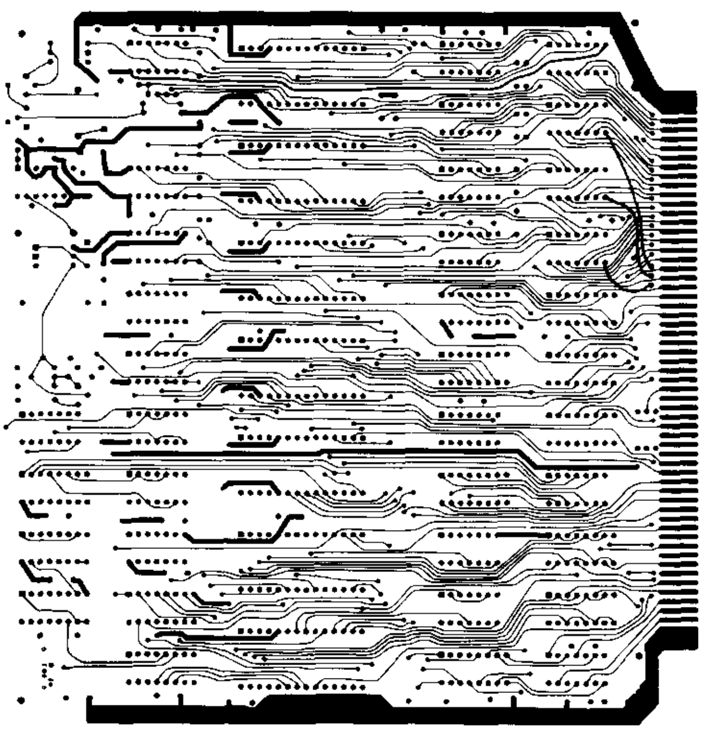
7 PLC'S

NOTES:

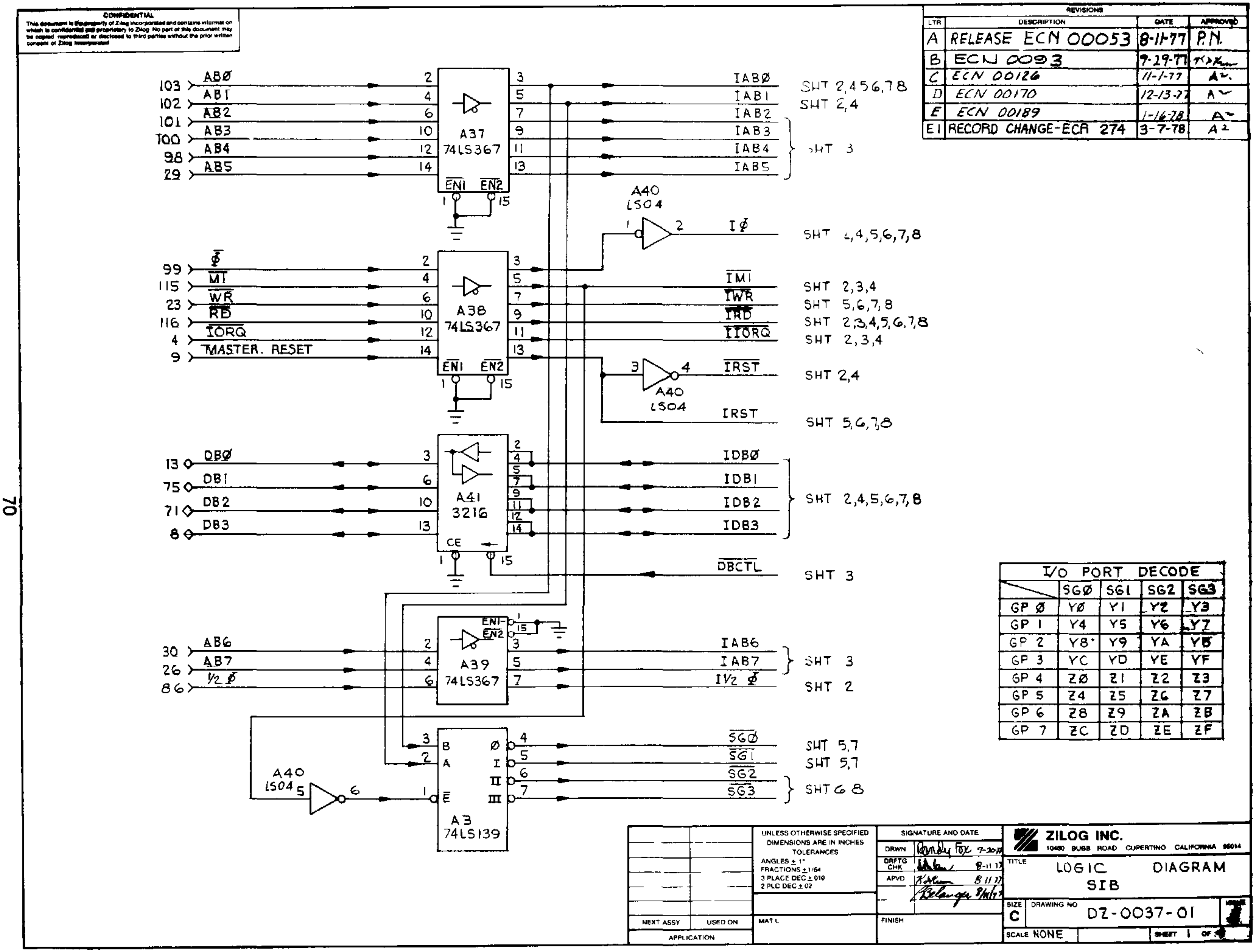
1. ASSEMBLE PER ZILOG MANUFACTURING SPECS.
2. RUBBER STAMP SERIAL NO. AND LATEST REV LEVEL.
3. ALL ○ WITHOUT REF DESIGNATIONS ARE 0.1 UF FILTER CAPS

FAB B

NEXT ASSY / USED ON / APPLICATION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1 64 3 PLACE DEC ± 010 2 PLC DEC ± 02	SIGNATURE AND DATE DRWN [signature] 11-3-77 DRFTG CHK APVD [signature] 11/14/7	ZILOG INC. 10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
	MAT L	FINISH	TITLE PRINTED WIRING ASS'Y, SIB
			SIZE C DRAWING NO 09-0037-01 ISSUE E
			SCALE SHEET OF 2



6.5 SCHEMATICS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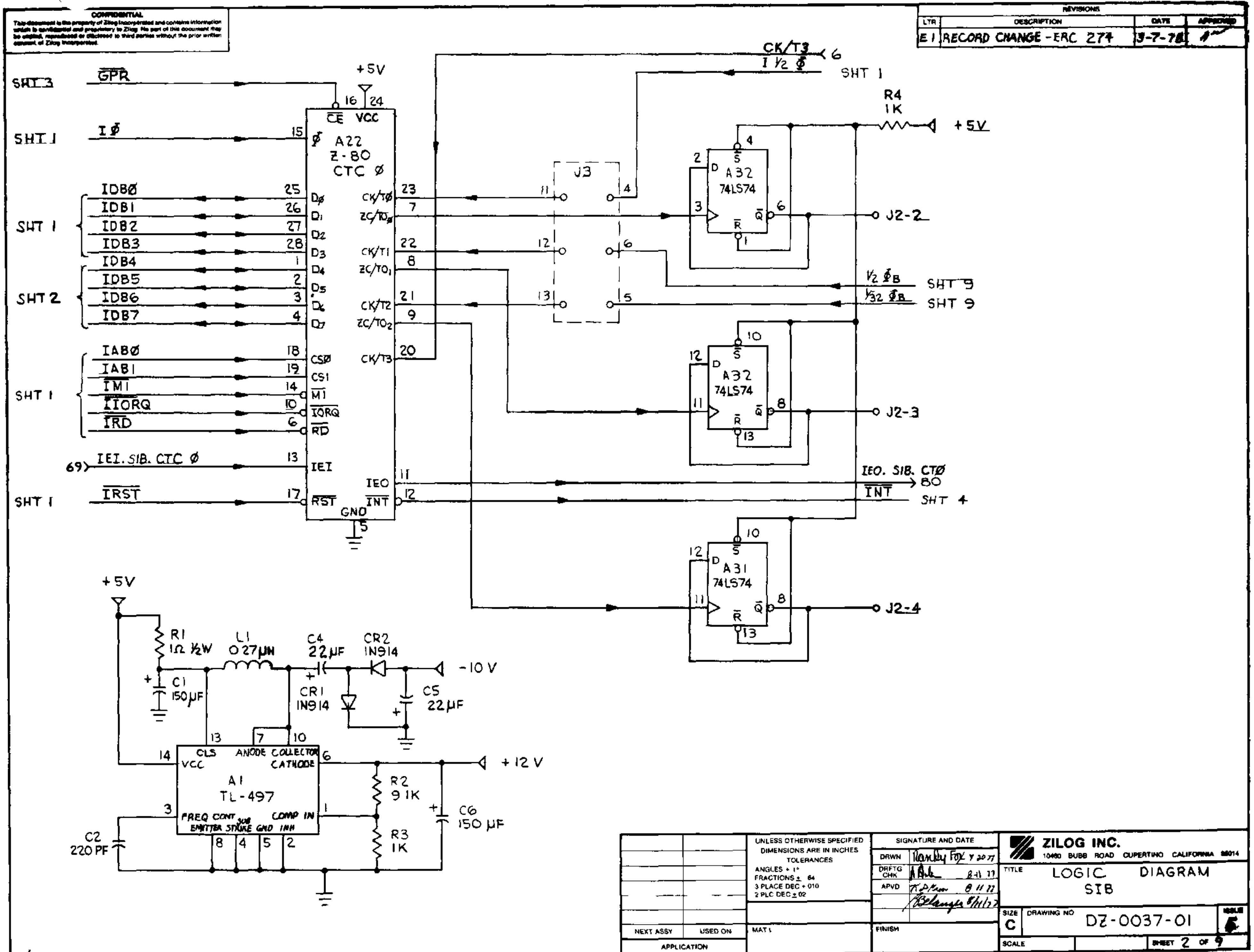
REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
A | RELEASE ECN 00053 | 8-1-77 | P.N.
B | ECN 0093 | 9-29-77
C | ECN 00126 | 11-1-77
D | ECN 00170 | 12-13-77
E | ECN 00189 | 1-16-78
E1 | RECORD CHANGE-ECR 274 | 3-7-78
103 ABØ
102 AB1
101 AB2
100 AB3
98 AB4
29 AB5
A37 74LS367
IABØ SHT 2,4,5,6,7,8
IAB1 SHT 2,4
IAB2
IAB3
IAB4
IAB5 SHT 3
99 Φ
115 M1
23 WR
116 RD
4 IORQ
9 MASTER. RESET
A38 74LS367
A40 LS04
IΦ SHT 4,5,6,7,8
IM1 SHT 2,3,4
IWR SHT 5,6,7,8
IRD SHT 2,3,4,5,6,7,8
IIORQ SHT 2,3,4
IRST SHT 2,4
IRST SHT 5,6,7,8
13 DBØ
75 DB1
71 DB2
8 DB3
A41 3216
CE
IDBØ
IDB1
IDB2
IDB3 SHT 2,4,5,6,7,8
DBCTL SHT 3
30 AB6
26 AB7
86 1/2 Φ
A39 74LS367
EN1 EN2
IAB6
IAB7 SHT 3
I1/2 Φ SHT 2
A3 74LS139
SGØ SHT 5,7
SG1 SHT 5,7
SG2
SG3 SHT 6,8
I/O PORT DECODE
| SGØ | SG1 | SG2 | SG3
GP Ø | YØ | Y1 | Y2 | Y3
GP 1 | Y4 | Y5 | Y6 | Y7
GP 2 | Y8 | Y9 | YA | YB
GP 3 | YC | YD | YE | YF
GP 4 | ZØ | Z1 | Z2 | Z3
GP 5 | Z4 | Z5 | Z6 | Z7
GP 6 | Z8 | Z9 | ZA | ZB
GP 7 | ZC | ZD | ZE | ZF
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02
SIGNATURE AND DATE
DRWN Randy Fox 7-20-77
DRFTG CHK 8-11-77
APVD 8-11-77
NEXT ASSY
USED ON
APPLICATION
MAT'L
FINISH
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
TITLE LOGIC DIAGRAM SIB
SIZE C
DRAWING NO DZ-0037-01
SCALE NONE
SHEET 1 OF


CONFIDENTIAL
REVISIONS
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SHT 3 GPR
SHT 1 IØ
SHT 1 IDBØ IDB1 IDB2 IDB3
SHT 2 IDB4 IDB5 IDB6 IDB7
SHT 1 IABØ IAB1 IM1 IIORQ IRD
69 IEI. SIB. CTC Ø
SHT 1 IRST
+5V
A22 Z-80 CTC Ø
CE VCC Ø
CK/TØ ZC/TOØ CK/T1 ZC/TO1 CK/T2 ZC/TO2 CK/T3
CSØ CS1 M1 IORQ RD IEI RST IEO INT GND
J3
CK/T3 6
I 1/2 Ø SHT 1
R4 1K +5V
A32 74LS74
A31 74LS74
J2-2
J2-3
J2-4
1/2 ØB SHT 9
1/32 ØB SHT 9
IEO. SIB. CTØ 80
INT SHT 4
R1 1Ω 1/2W
L1 0.27µH
C4 22µF
CR2 1N914
-10V
C1 150µF
CR1 1N914
C5 22µF
A1 TL-497
CLS ANODE COLLECTOR CATHODE VCC
FREQ CONT EMITTER 308 STROBE GND COMP IN INH
+12V
R2 9.1K
R3 1K
C6 150µF
C2 220PF
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02
SIGNATURE AND DATE
DRWN DRFTG CHK APVD
NEXT ASSY USED ON APPLICATION MAT'L FINISH
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
TITLE LOGIC DIAGRAM SIB
SIZE C DRAWING NO DZ-0037-01
SCALE SHEET 2 OF 9

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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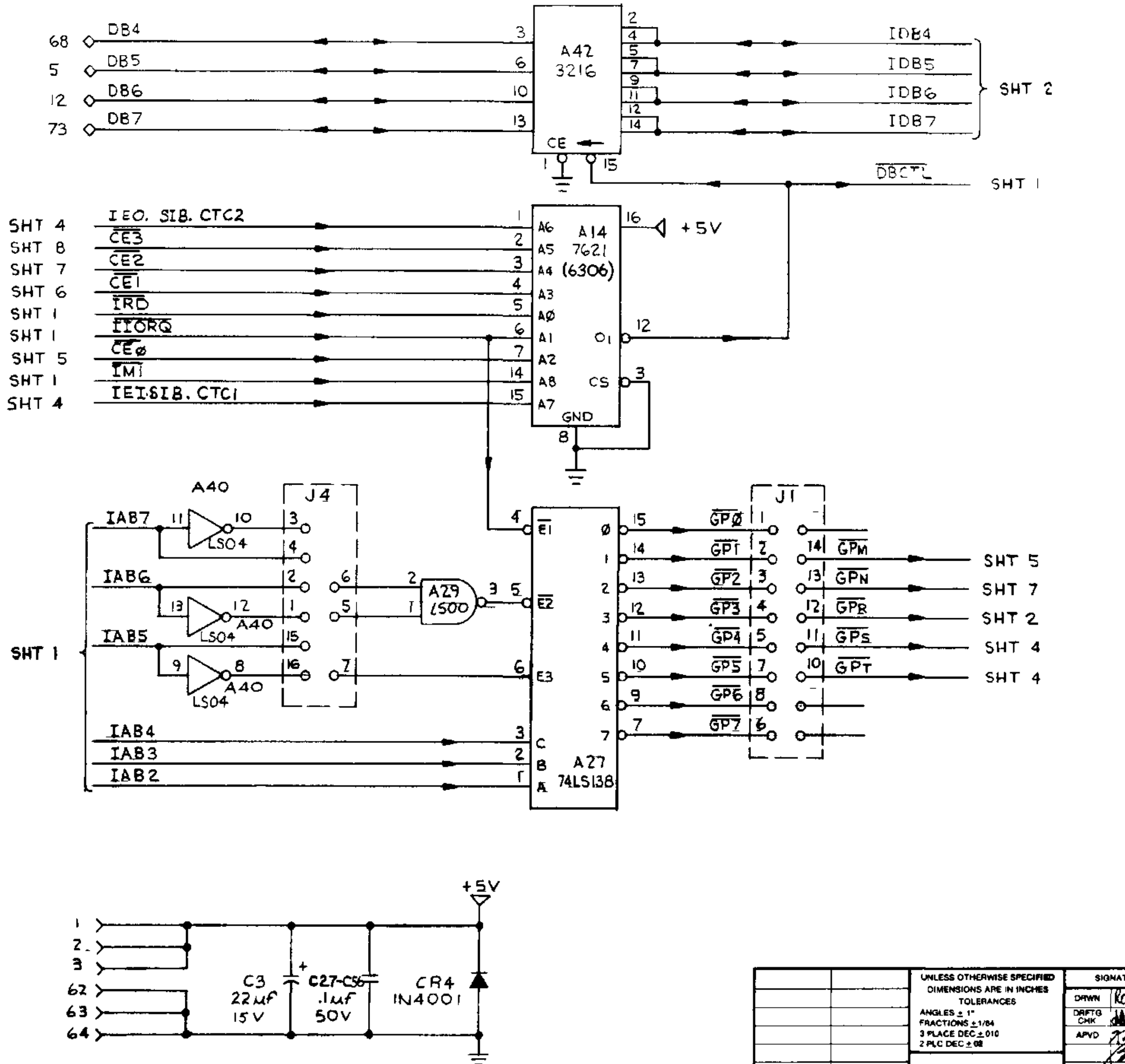


PORT GROUP DECODE

Y	Z	JUMPER PINS OF J4		
Ø	1	5-16	1-7	3-6
2	3	5-15	1-7	3-6
4	5	5-16	2-7	3-6
6	7	5-15	2-7	3-6
8	9	5-16	1-7	4-6
A	B	5-15	1-7	4-6
C	D	5-16	2-7	4-6
E	F	5-15	2-7	4-6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

SIGNATURE AND DATE
DRWN Randy Fox 7-20-77
DRFTG CHK 8-11-77
APVD 8-11-77

NEXT ASSY | USED ON | APPLICATION | MAT'L | FINISH

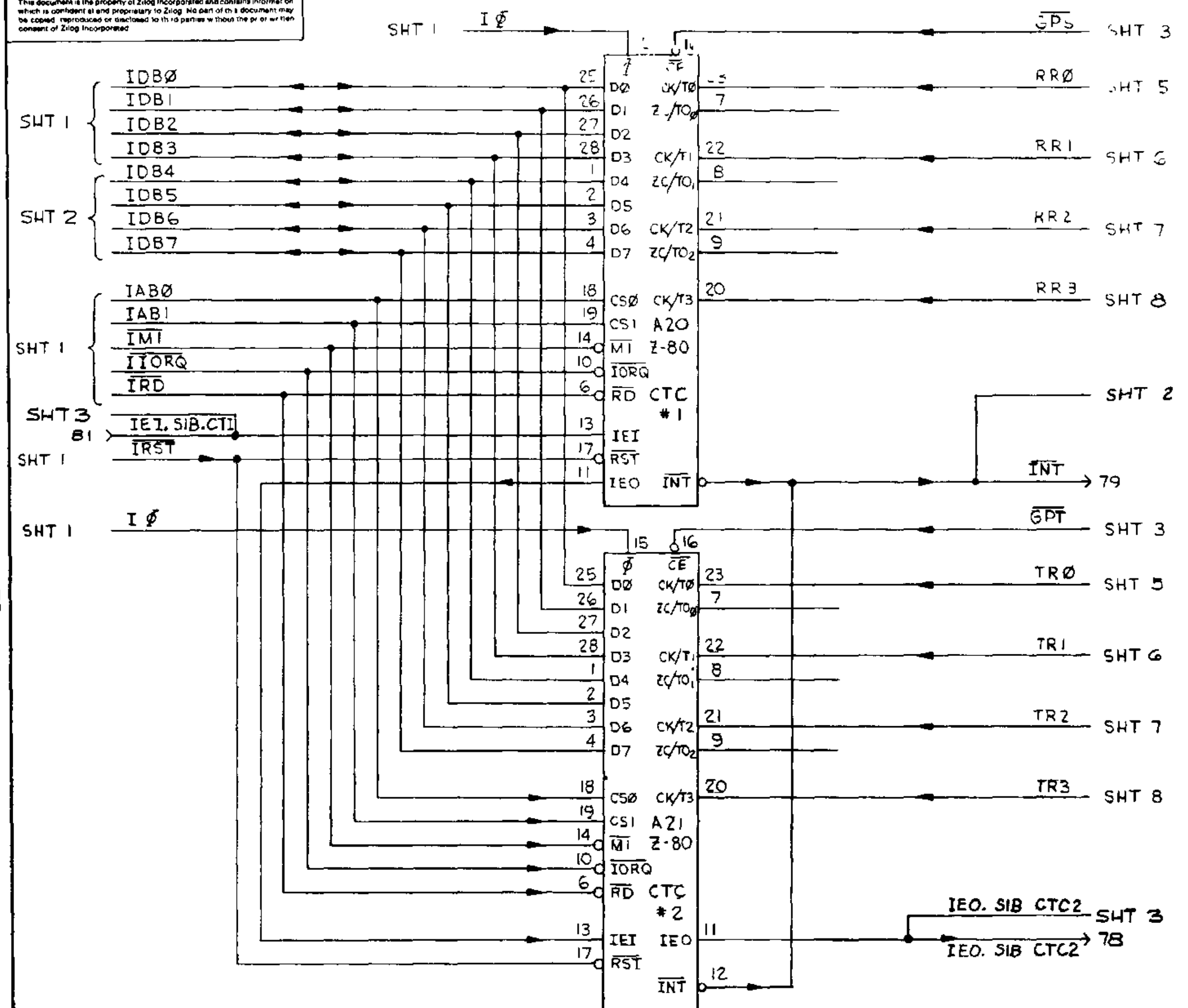
ZILOG INC.
10460 BUBB ROAD CUPERTINO, CALIFORNIA

TITLE LOGIC DIAGRAM SIB

SIZE C DRAWING NO DZ-0037-01

SCALE NONE

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E/	RECORD CHANGE - ECR 274	3-8-78	

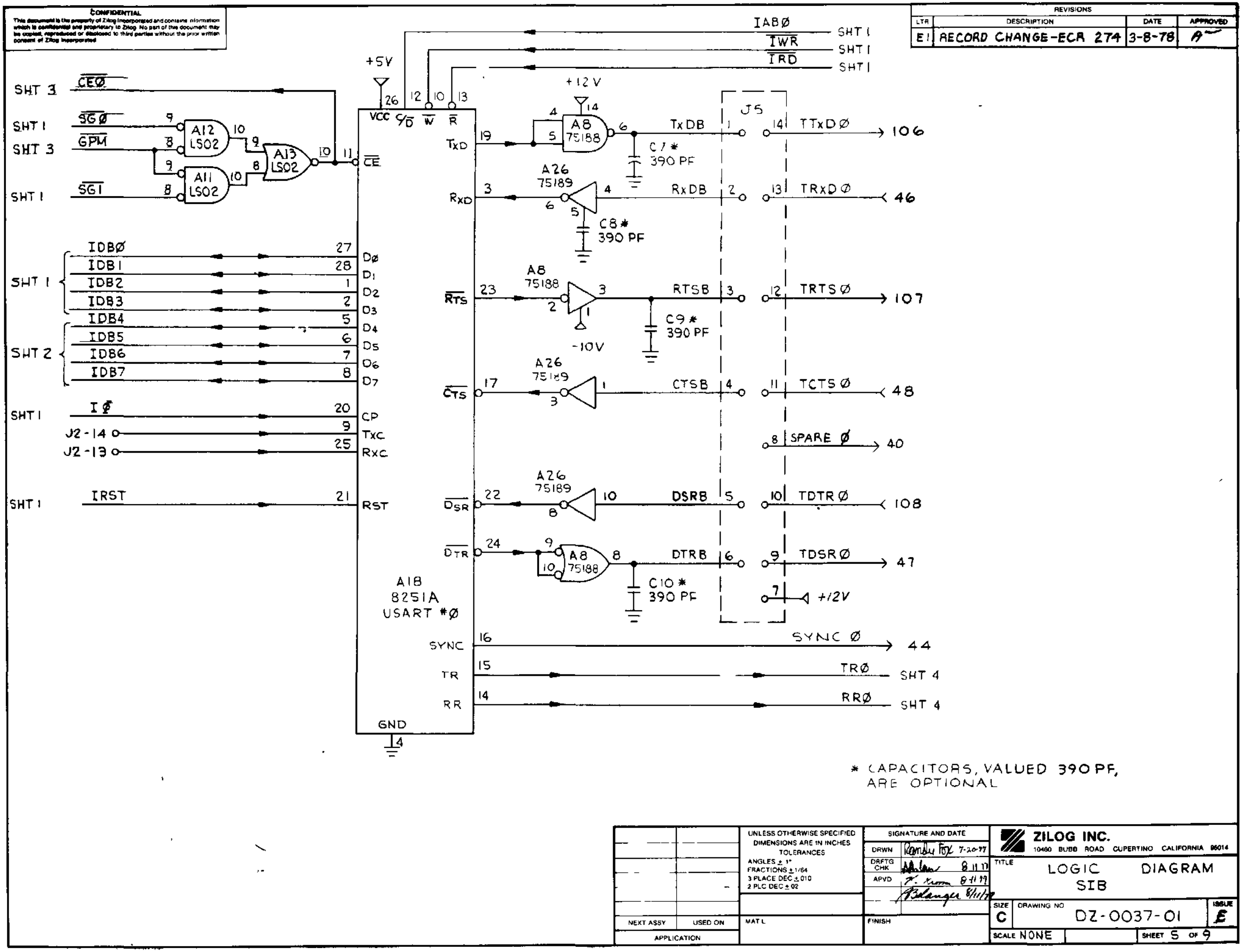


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES	ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02
SIGNATURE AND DATE	DRWN 7-26-77; DRFTG CHK 8-11-78; APVD 8-11-77
NEXT ASSY	USED ON
APPLICATION	
MAT L	FINISH

ZILOG INC.
10460 BUBB ROAD, CUPERTINO CALIFORNIA

TITLE: LOGIC DIAGRAM SIB

SIZE C | DRAWING NO DZ-0037-01 | SCALE NONE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REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
E1 | RECORD CHANGE-ECR 274 | 3-8-78
IABØ SHT 1
IWR SHT 1
IRD SHT 1
+5V
+12V
SHT 3 CEØ
SHT 1 SGØ
SHT 3 GPM
SHT 1 SG1
A12 LS02
A11 LS02
A13 LS02
VCC C/D W R
TxD
RxD
RTS
CTS
DSR
DTR
A8 75188
A26 75189
-10V
TxDB
RxDB
RTSB
CTSB
DSRB
DTRB
C7* 390 PF
C8* 390 PF
C9* 390 PF
C10* 390 PF
J5
TTxDØ 106
TRxDØ 46
TRTSØ 107
TCTSØ 48
SPARE Ø 40
TDTRØ 108
TDSRØ 47
+12V
SHT 1 IDBØ IDB1 IDB2 IDB3
SHT 2 IDB4 IDB5 IDB6 IDB7
DØ D1 D2 D3 D4 D5 D6 D7
SHT 1 IΦ CP
J2-14 TxC
J2-13 RxC
SHT 1 IRST RST
A18
8251A
USART #Ø
SYNC
TR
RR
GND
SYNC Ø 44
TRØ SHT 4
RRØ SHT 4
* CAPACITORS, VALUED 390 PF, ARE OPTIONAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02
NEXT ASSY
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SIGNATURE AND DATE
DRWN 7-20-77
DRFTG CHK 8-11-77
APVD 8-11-77
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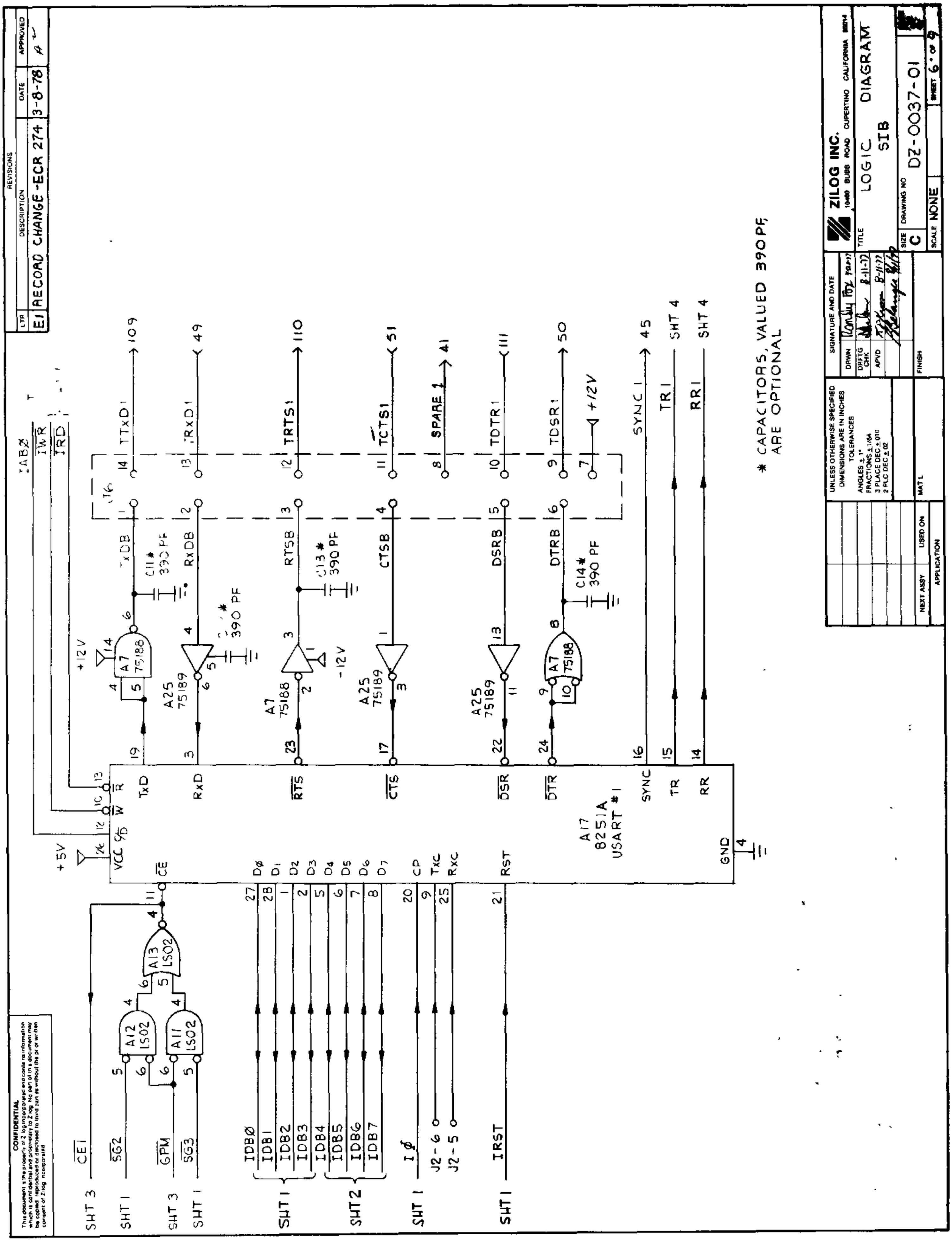
TITLE LOGIC DIAGRAM SIB
SIZE C
DRAWING NO DZ-0037-01
ISSUE E
SCALE NONE
SHEET 5 OF 9


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
E1 RECORD CHANGE -ECR 274 3-8-78
A17
8251A
USART #1
VCC
CE
TxD
RxD
RTS
CTS
DSR
DTR
SYNC
TR
RR
GND
CP
TxC
RxC
RST
TTxD1
TRTS1
TCTS1
SPARE 1
TDTR1
TDSR1
+12V
SYNC 1
TR1
RR1
SHT 4
IAB0
IWR
IRD
TxDB
RxDB
RTSB
CTSB
DSRB
DTRB
C11 * 390 PF
C13 * 390 PF
C14 * 390 PF
A7 75188
A25 75189
-12V
+5V
A13 LS02
A12 LS02
A11 LS02
CE1
SG2
GPM
SG3
IDB0
IDB1
IDB2
IDB3
IDB4
IDB5
IDB6
IDB7
I0
J2-6
J2-5
IRST
SHT 1
SHT 2
SHT 3
* CAPACITORS, VALUED 390 PF, ARE OPTIONAL
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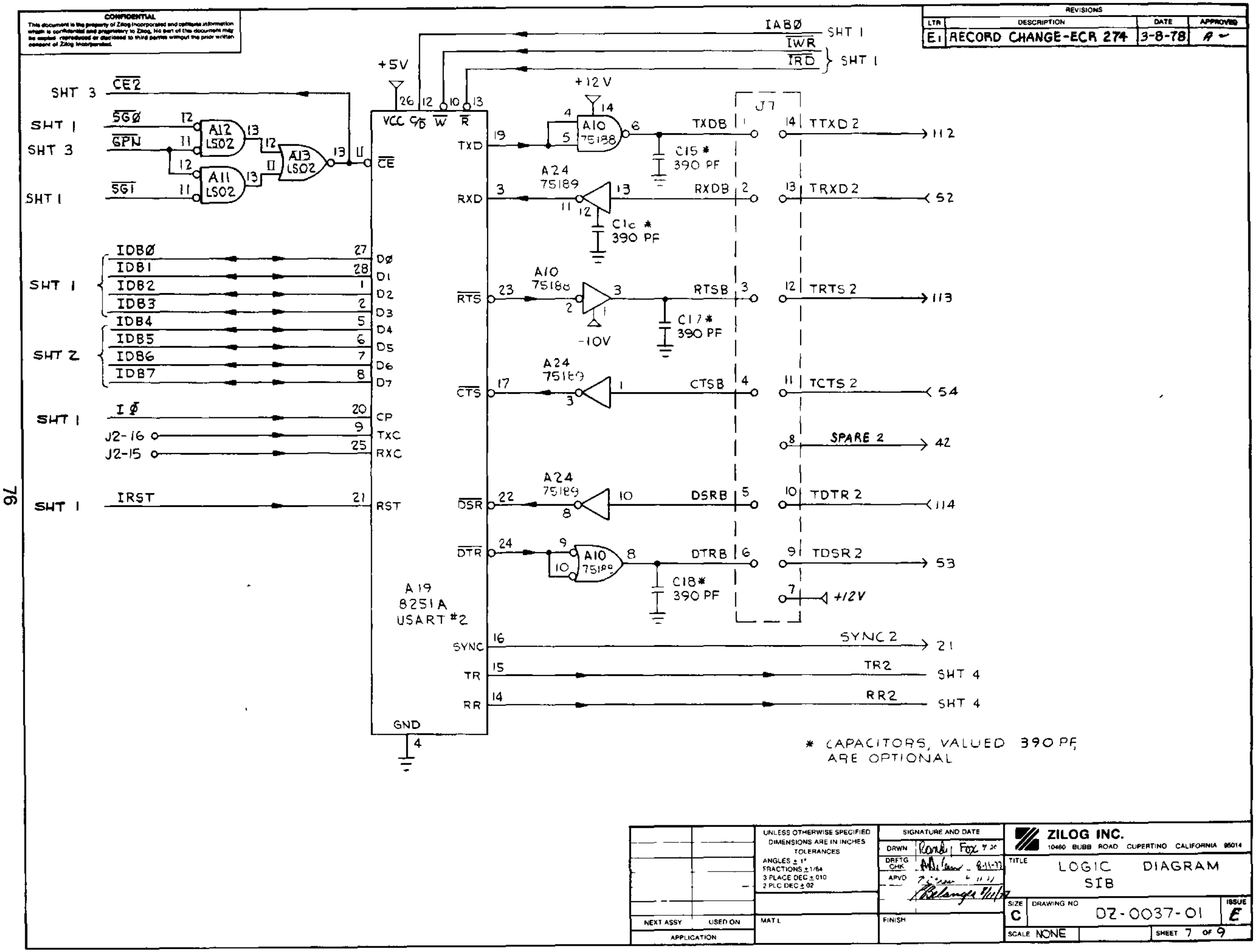
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02
SIGNATURE AND DATE
DRWN
DRFTG CHK
APVD
MAT'L
FINISH
NEXT ASSY
USED ON
APPLICATION
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA
TITLE
LOGIC DIAGRAM
SIB
SIZE C
DRAWING NO
DZ-0037-01
SCALE NONE
SHEET 6 OF 9



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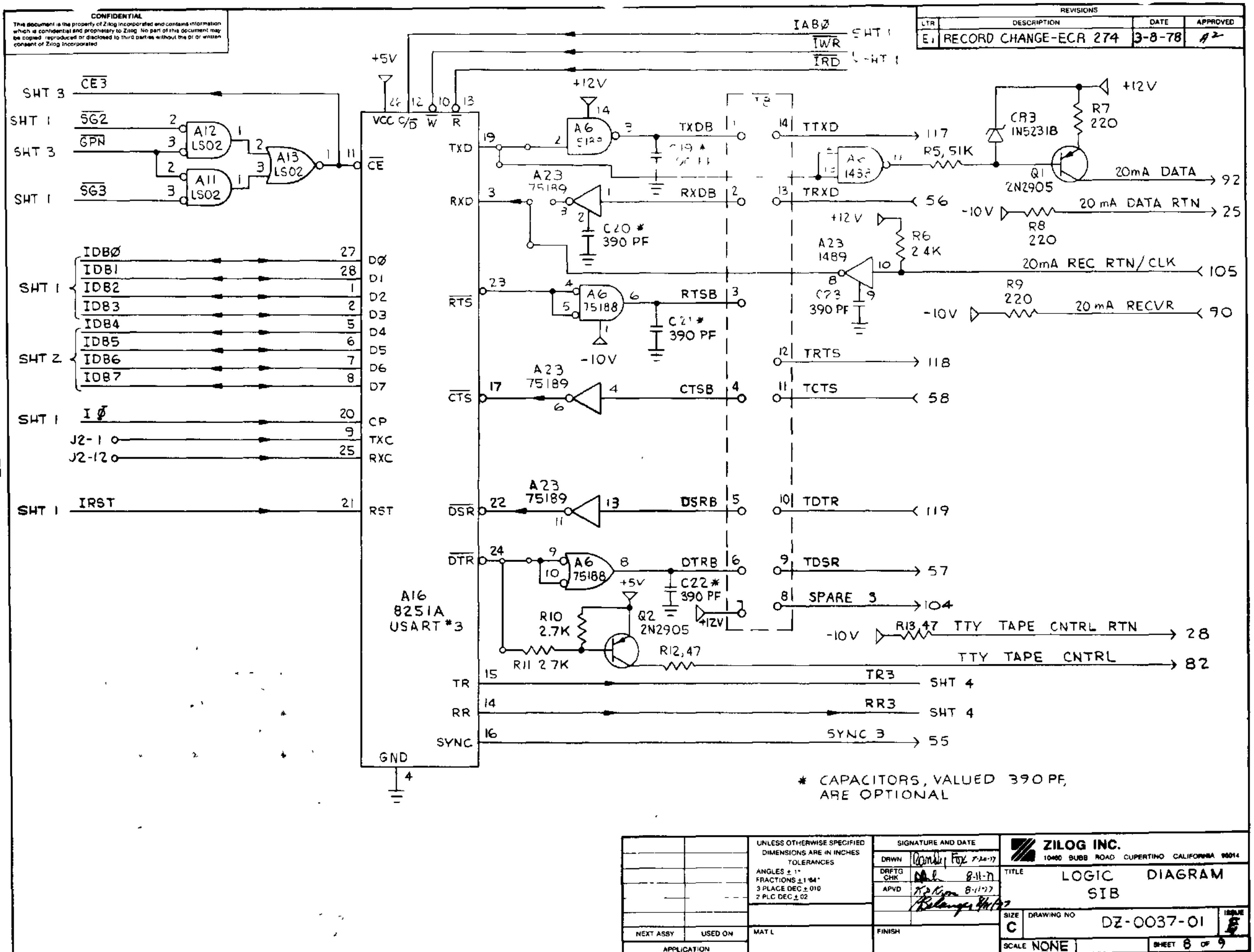
REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
E1 RECORD CHANGE-ECR 274 3-8-78
IABØ SHT 1
IWR
IRD SHT 1
SHT 3 CE2
SHT 1 5GØ
SHT 3 GPN
SHT 1 5G1
A12 LS02
A11 LS02
A13 LS02
SHT 1 IDBØ IDB1 IDB2 IDB3
SHT 2 IDB4 IDB5 IDB6 IDB7
SHT 1 IØ
J2-16
J2-15
SHT 1 IRST
+5V
VCC C/D W R
TXD RXD RTS CTS DSR DTR
CE DØ D1 D2 D3 D4 D5 D6 D7 CP TXC RXC RST
A19 8251A USART #2
SYNC TR RR GND
+12V
A10 75188
A24 75189
A10 75188
-10V
A24 75189
A24 75189
A10 75188
C15 * 390 PF
C1c * 390 PF
C17 * 390 PF
C18 * 390 PF
TXDB RXDB RTSB CTSB DSRB DTRB
J7
TTXD 2 → 112
TRXD 2 ← 52
TRTS 2 → 113
TCTS 2 ← 54
SPARE 2 → 42
TDTR 2 ← 114
TDSR 2 → 53
+12V
SYNC 2 → 21
TR2 SHT 4
RR2 SHT 4
* CAPACITORS, VALUED 390 PF, ARE OPTIONAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02
SIGNATURE AND DATE
DRWN
DRFTG CHK
APVD
MAT L
FINISH
NEXT ASSY
USED ON
APPLICATION
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
TITLE LOGIC DIAGRAM SIB
SIZE C
DRAWING NO DZ-0037-01
ISSUE E
SCALE NONE
SHEET 7 OF 9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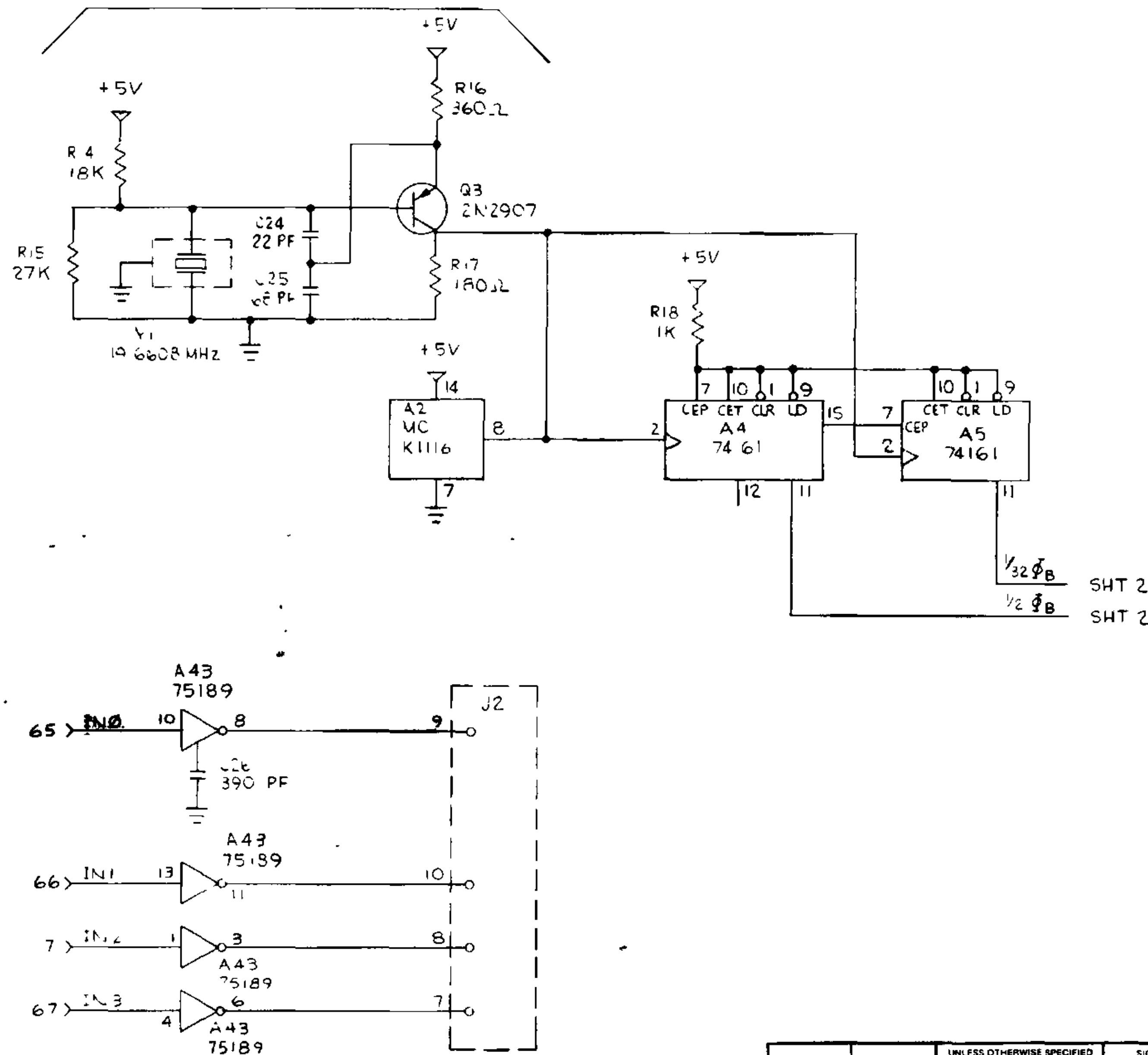
REVISIONS
E1 RECORD CHANGE-ECR 274 3-8-78
A16
8251A
USART *3
20mA DATA
20 mA DATA RTN
20mA REC RTN/CLK
20 mA RECVR
TTY TAPE CNTRL RTN
TTY TAPE CNTRL
* CAPACITORS, VALUED 390 PF, ARE OPTIONAL
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
LOGIC DIAGRAM
SIB
DZ-0037-01
SIZE C
SCALE NONE
SHEET 8 OF 9

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E	RECORD CHANGE-ECR 274	3-8-78	A



NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE
APPLICATION		MAT'L	FINISH

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TITLE LOGIC DIAGRAM SIB

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Zilog

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DOCUMENT CHANGE NOTICE

Zilog

DATE: 01-02-79

DCN NUMBER: E3-0051-00, Rev. B

PUBLICATION NUMBER: 03-0051-00, Rev. B

TITLE: Z-80 SIB USER MANUAL

PREVIOUS DCN's, BY NUMBER: E3-0051-00, Rev. A

EFFECTIVE DATE: 01-02-79

This Document Change Notice provides change pages for the publication specified above. These change pages supersede and obsolete those provided in the previous DCN package, E3-0051-00, Revision A, and will remain in effect for subsequent releases unless specifically amended by another DCN or superseded by a publication revision. The following pages are to be treated as described below:

Replace page 45 and 46
Replace pages 69-78 (schematics: Z-80 SIB)

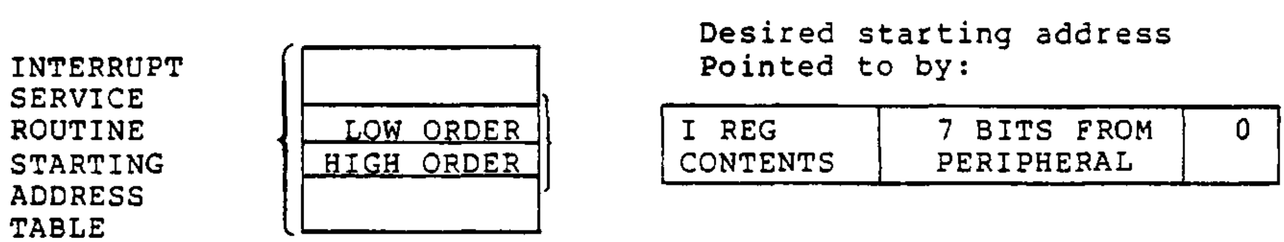
Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of the manual to provide a record of changes.

Time Constant Register							
D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC2	TC0
MSB							LSB

The Z80-CTC has been designed to operate with the Z80-CPU programmed for mode 2 interrupt response. Under the requirements of this mode, when a CTC channel requests an interrupt and is acknowledged, a 16-bit pointer must be formed to obtain a corresponding interrupt service routine starting address from a table in memory. The upper 8 bits of this pointer are provided by the CPU's I register, and the lower 8 bits of the pointer are provided by the CTC in the form of an interrupt vector unique to the particular channel that requested the interrupt.

MODE 2 INTERRUPT OPERATION



The high-order five bits of this interrupt vector must be written to the CTC in advance, as part of the initial programming sequence. To do so, the CPU must write to the I/O port addresses corresponding to the CTC Channel 0, just as it would if a channel control word were being written to that channel, except that Bit 0 of the word being written must contain a zero. As explained in Section 3.1, above, if Bit 0 of a word written to a channel were set to 1, the word would be interpreted as a Channel Control Word; consequently, a zero in Bit 0 signals the CTC to load the incoming word into the Interrupt Vector register. Bits 1 and 2, however, are not used when loading this vector. At the time when the interrupting channel must place the interrupt vector on the Z80 data bus, the interrupt control logic of the CTC automatically supplies a binary code in Bits 1 and 2, identifying which of the four CTC channels is to be serviced.

INTERRUPT VECTOR REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	X	X	0

Supplied by User (D7–D3)

D2	D1	
0	0	Channel 0 (highest priority)
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3 (lowest priority)

Automatically inserted by Z80-CTC

6.5 SCHEMATICS

LTR	DESCRIPTION	DATE	APPROVED
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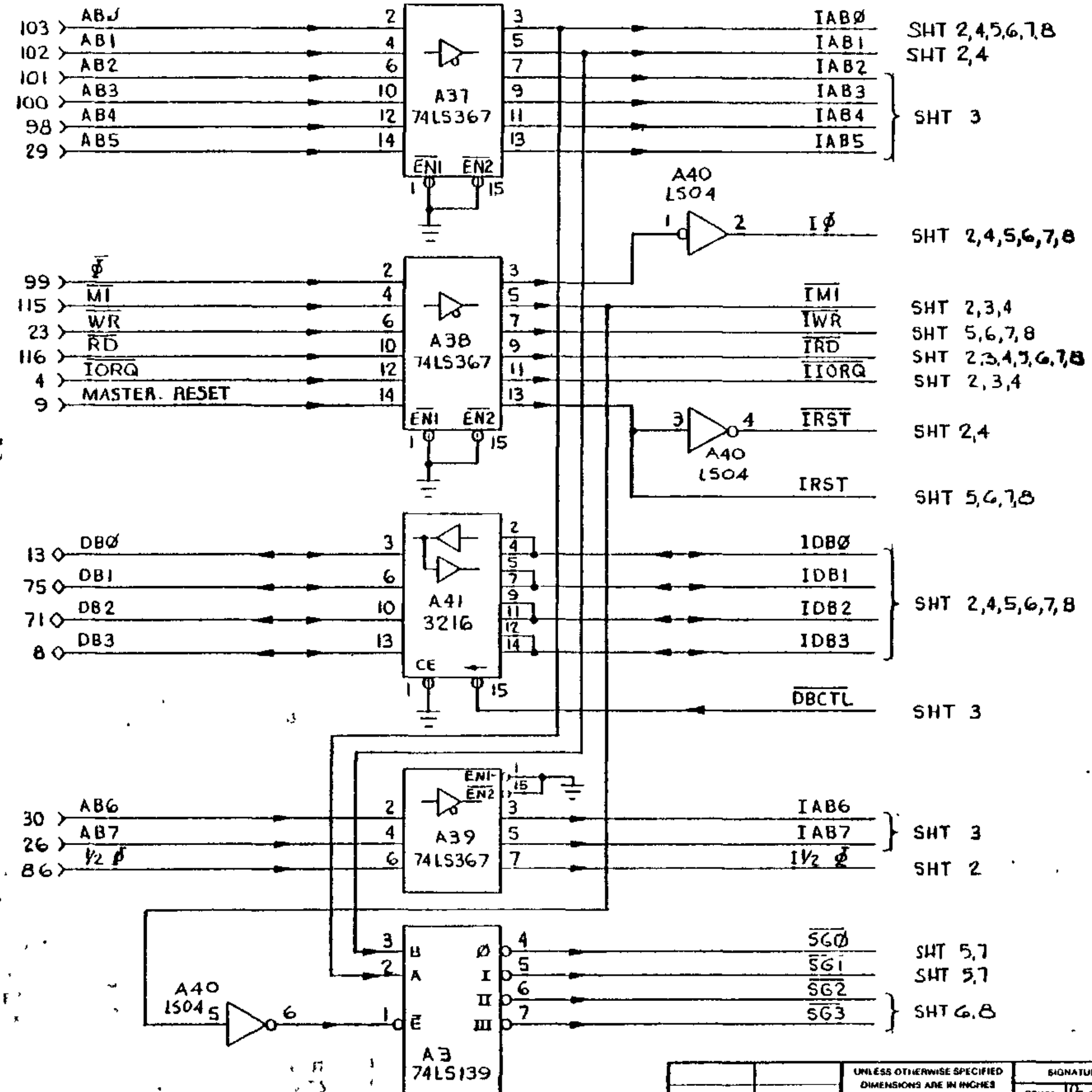

I/O PORT DECODE	SGØ	SG1	SG2	SG3
GP Ø	YØ	Y1	Y2	Y3
GP 1	Y4	Y5	Y6	Y7
GP 2	Y8	Y9	YA	YB
GP 3	YC	YD	YE	YF
GP 4	ZØ	Z1	Z2	Z3
GP 5	Z4	Z5	Z6	Z7
GP 6	Z8	Z9	ZA	ZB
GP 7	ZC	ZD	ZE	ZF

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02

NEXT ASSY | USED ON | APPLICATION | MAT'L | FINISH

SIGNATURE AND DATE: DRAWN; DRFTG CHK; APVD

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TITLE: LOGIC DIAGRAM Z80 SIB

SIZE C | DRAWING NO DZ-0037-02 | ISSUE A

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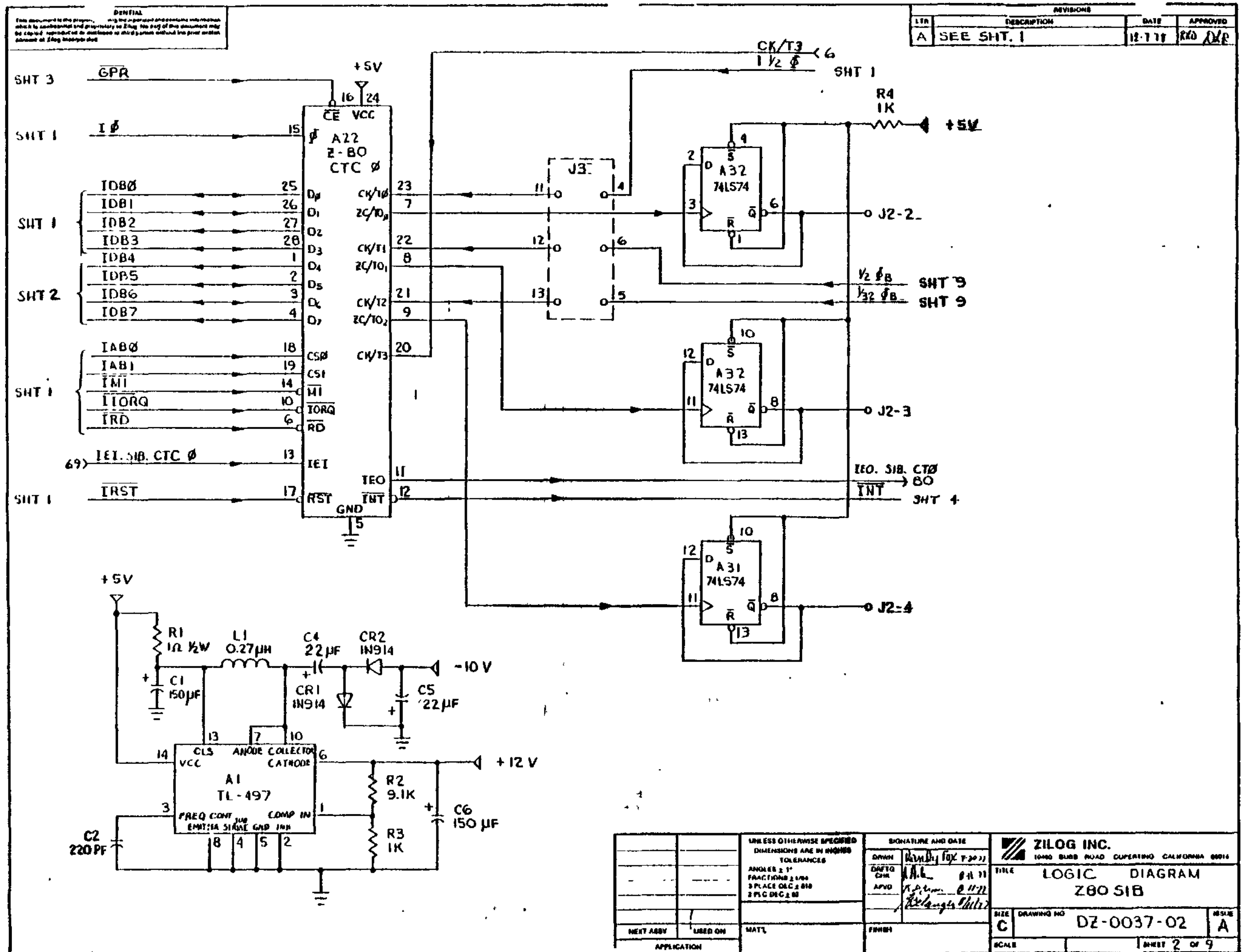

REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
A | SEE SHT. 1
SHT 3 GPR
SHT 1 I Ø
SHT 1 IDBØ IDB1 IDB2 IDB3
SHT 2 IDB4 IDB5 IDB6 IDB7
SHT 1 IABØ IAB1 IM1 IIORQ IRD
69) IEI. SIB. CTC Ø
SHT 1 IRST
+5V
A22 Z-80 CTC Ø
CE VCC
CK/TØ ZC/TOØ CK/T1 ZC/TO1 CK/T2 ZC/TO2 CK/T3
IEO INT GND IEI RST
CSØ CS1 M1 IORQ RD
J3
CK/T3 1 1/2 Ø
SHT 1
R4 1K
+5V
A32 74LS74
A31 74LS74
J2-2
J2-3
J2-4
1/2 ØB SHT 9
1/32 ØB SHT 9
IEO. SIB. CTØ 80
INT SHT 4
R1 1Ω 1/2W
L1 0.27μH
C4 22μF
CR2 1N914
-10 V
C1 150μF
CR1 1N914
C5 22μF
A1 TL-497
CLS VCC ANODE COLLECTOR CATHODE FREQ CONT EMITTER SUB STRATE GND COMP IN INH
+12 V
R2 9.1K
R3 1K
C6 150 μF
C2 220 PF
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES ± 1°
SIGNATURE AND DATE
DRAWN
DRFTG CHK
APVD
NEXT ASSY
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TITLE LOGIC DIAGRAM Z80 SIB
SIZE C
DRAWING NO DZ-0037-02
ISSUE A
SCALE
SHEET 2 OF 9

REVISIONS			
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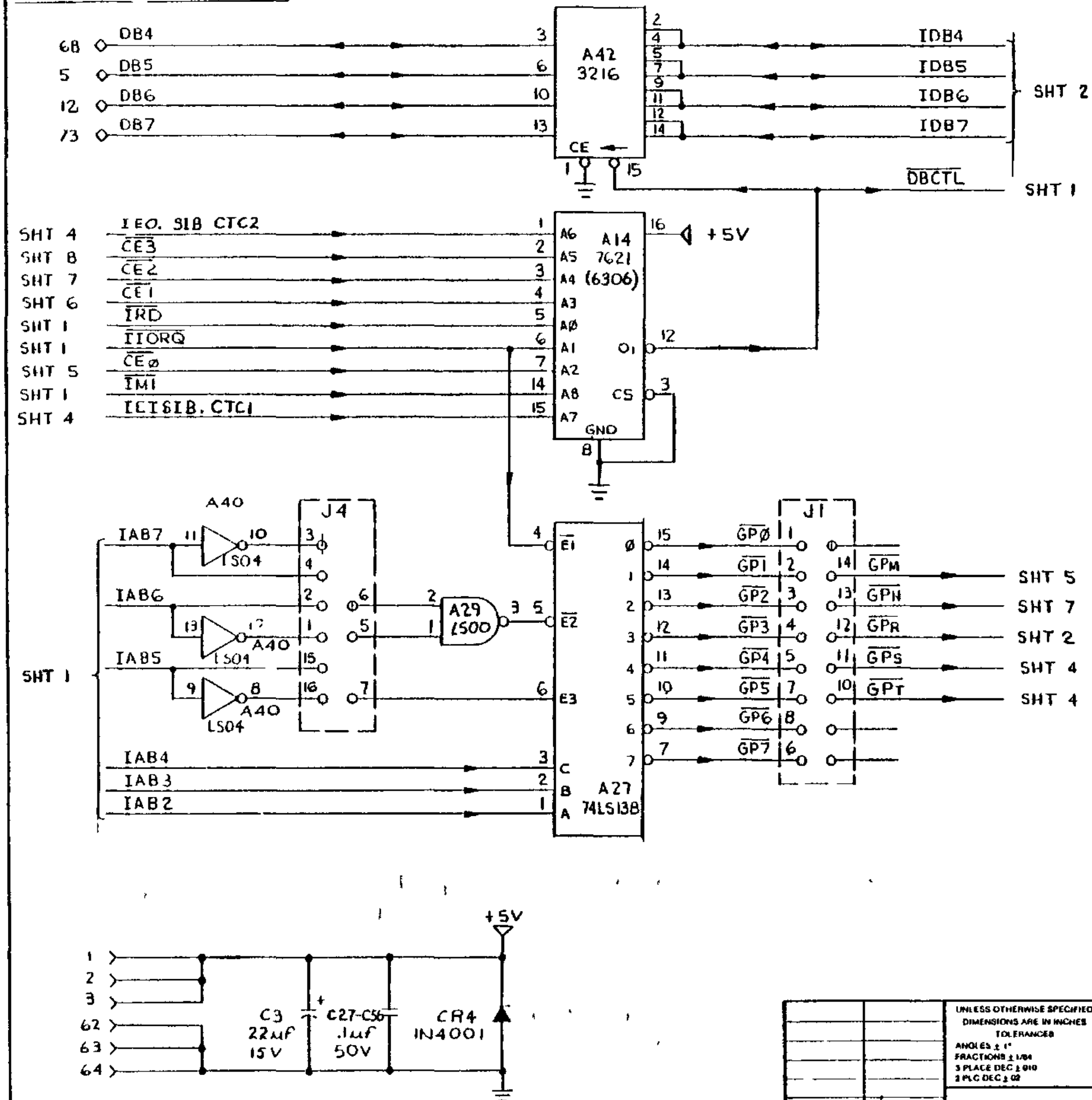

PORT GROUP DECODE		
Y	Z	JUMPER PINS OF J4
Ø	1	5-16 1-7 3-6
2	3	5 16 1 7 3 6
4	5	5 16 2-7 3-6
6	7	5-16 2-7 3-6
8	9	5 16 1-7 4-6
A	B	5 16 1-7 4-6
C	D	5 16 2-7 4-6
E	F	5 16 2-7 4-6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

NEXT ASSY | USED ON | APPLICATION | MAT'L | FINISH

SIGNATURE AND DATE
DRWN Randy Fox 7-20-77
DRFTG CHK 8-11-77
APVD 8-11-77

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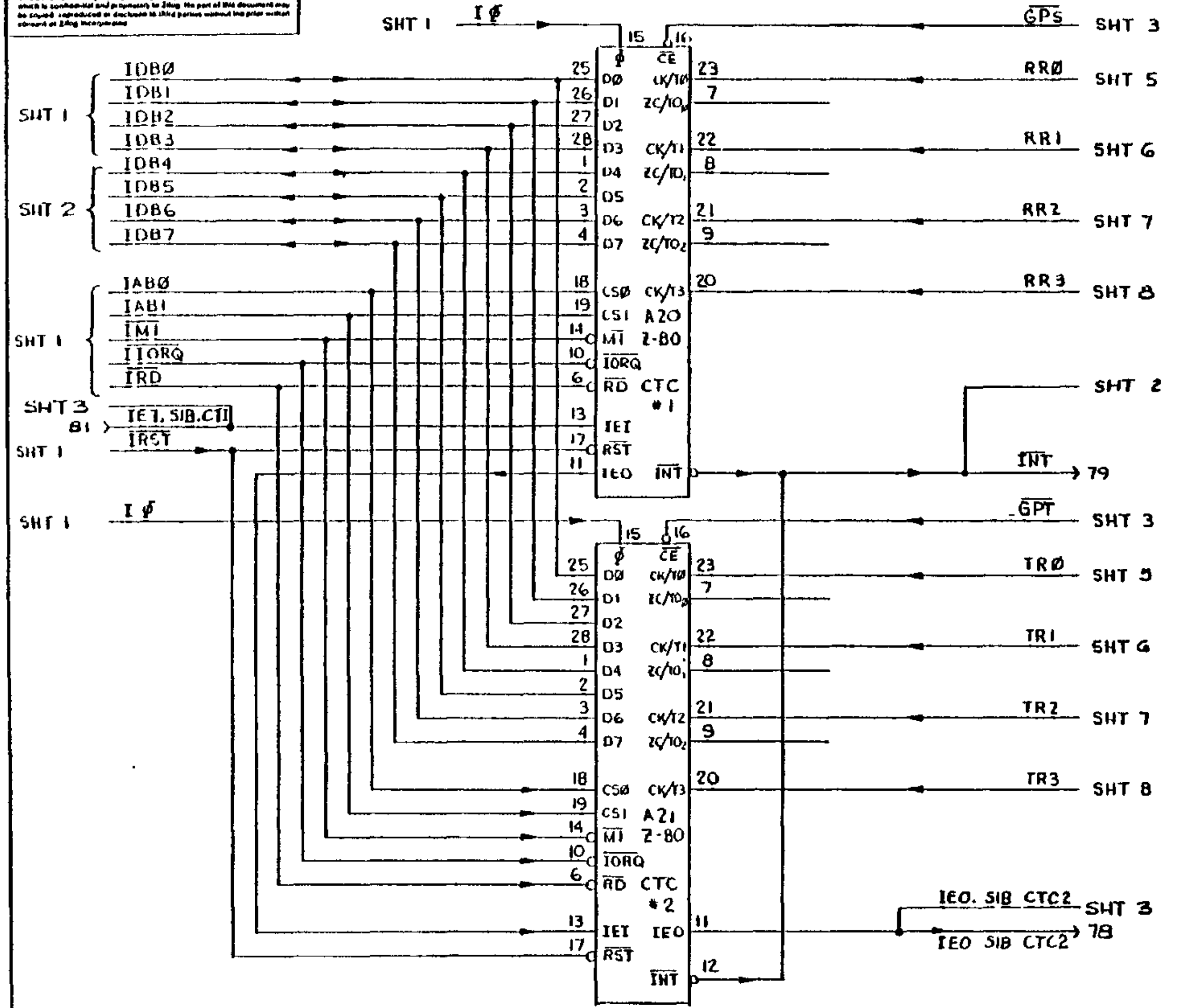
TITLE LOGIC DIAGRAM
Z80 SIB

SIZE C | DRAWING NO DZ-0037-02 | ISSUE A

SCALE NONE | SHEET 3 OF 9



LTR	DESCRIPTION	DATE	APPROVED
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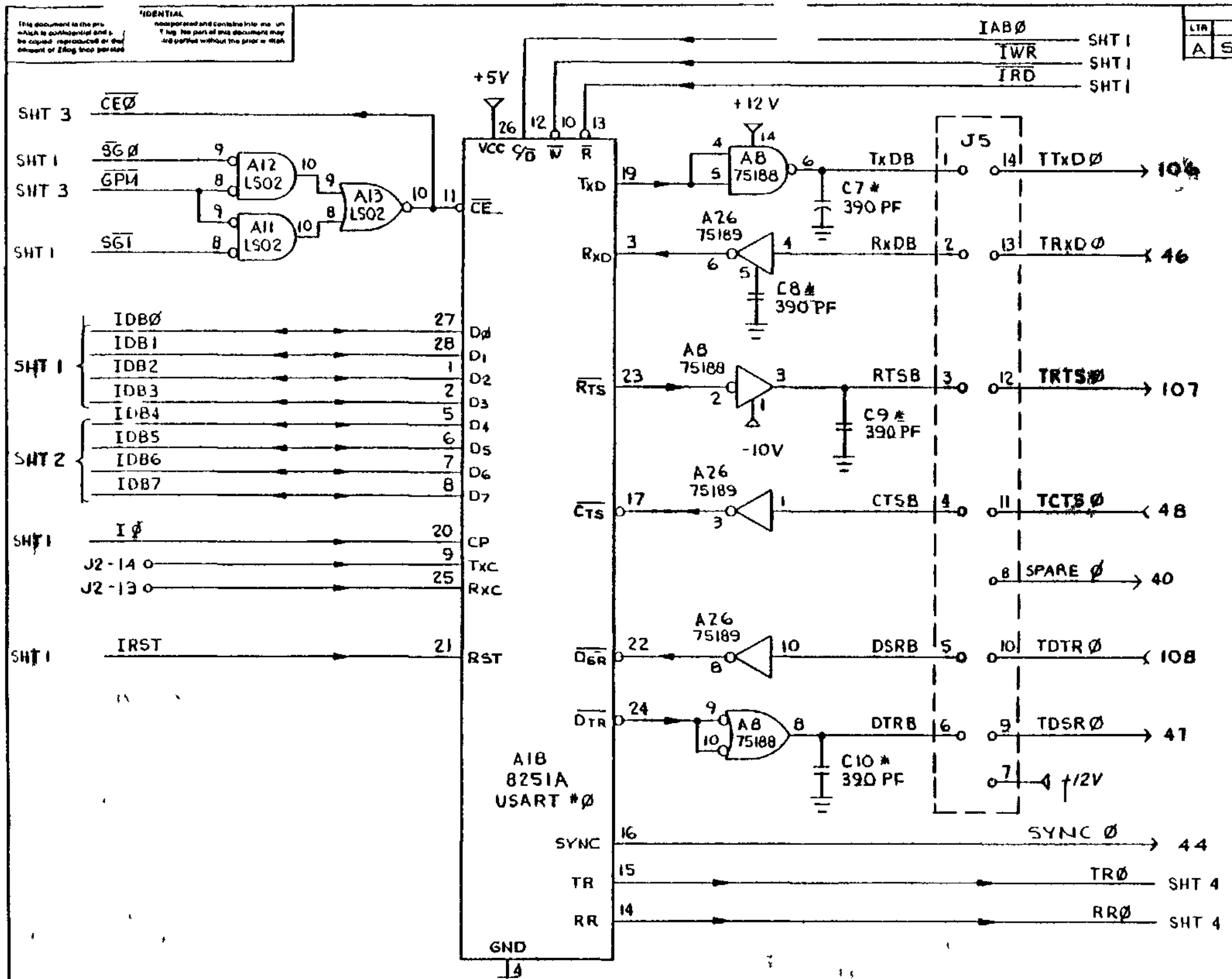
TITLE: LOGIC DIAGRAM Z80 SIB

SIZE: C DRAWING NO: DZ-0037-02 ISSUE: A

SCALE: NONE SHEET 4 OF 9

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02

NEXT ASSY | USED ON | APPLICATION | MAT'L | FINISH



* CAPACITORS, VALUED 390 PF, ARE OPTIONAL

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	1 1 78	RKJ

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TITLE LOGIC DIAGRAM Z80 SIB

SIZE C DRAWING NO DZ-0037-02 ISSUE A

SCALE NONE SHEET 5 OF 9

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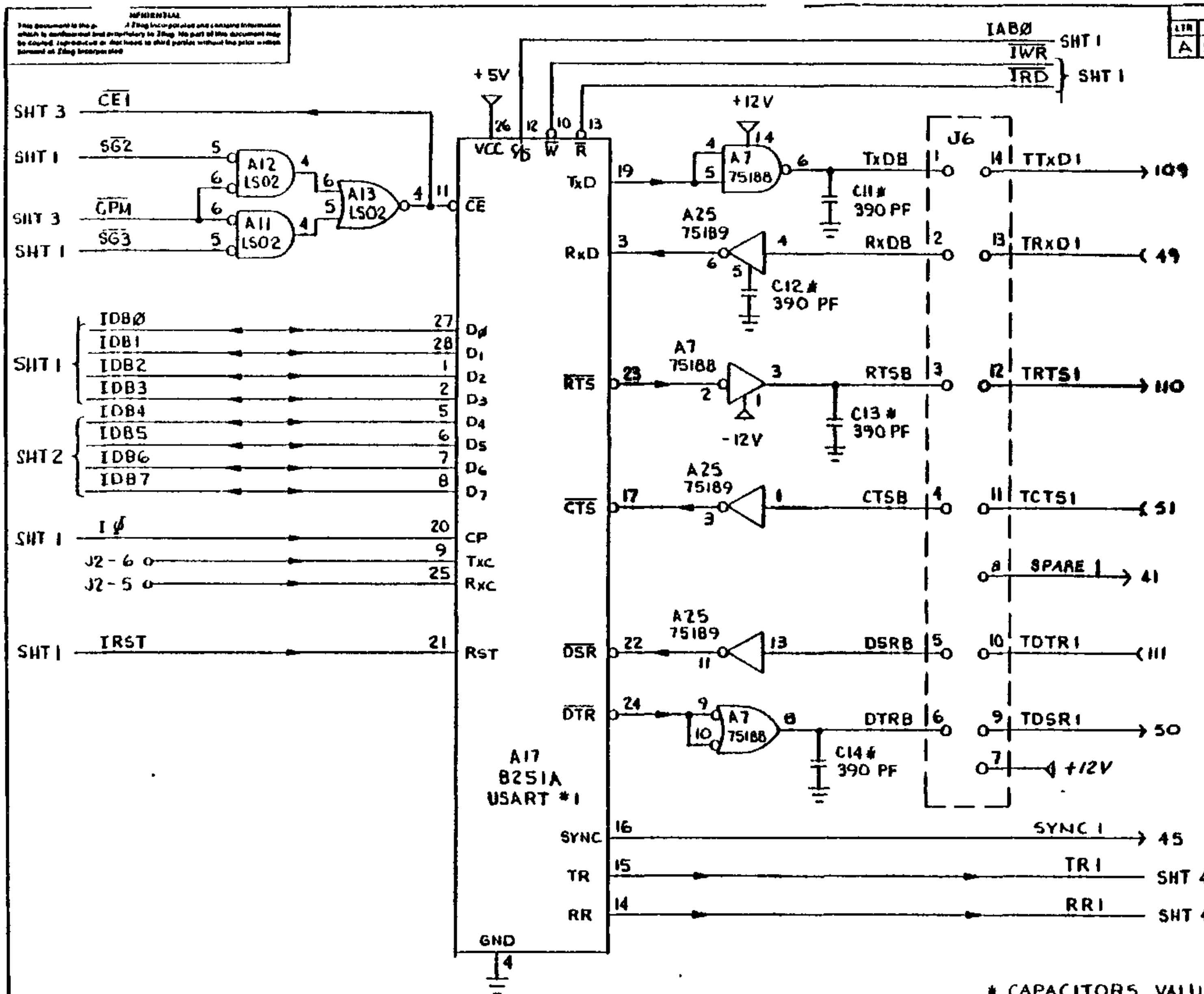

* CAPACITORS, VALUED 390PF,
ARE OPTIONAL

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TITLE	LOGIC DIAGRAM Z80 SIB
SIZE	C
DRAWING NO	DZ-0037-02
ISSUE	A
SCALE	NONE
SHEET	6 of 9

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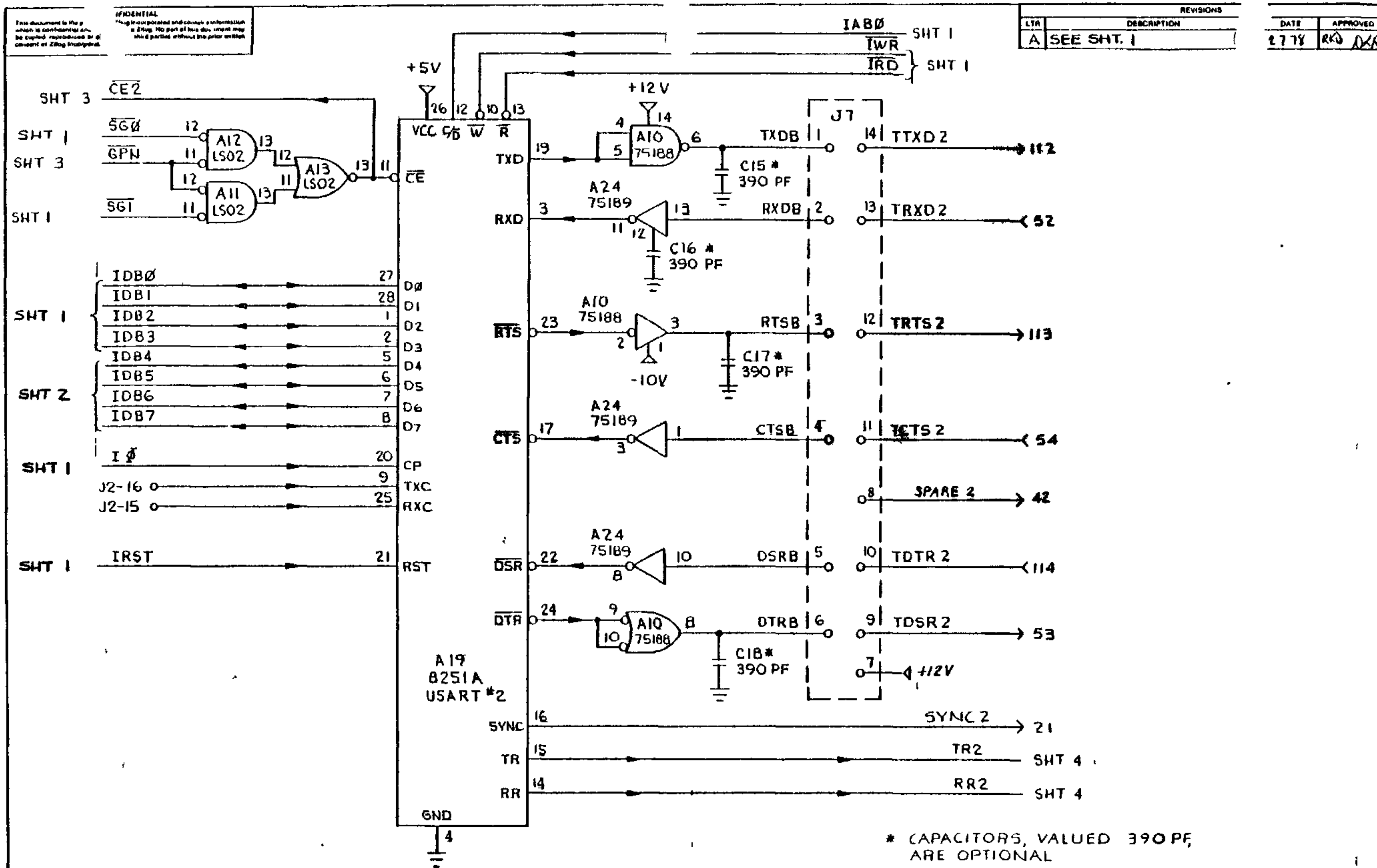
SIGNATURE AND DATE — DRAWN, DRFTG CHK, APVD

NEXT ASSY | USED ON — APPLICATION | MAT'L | FINISH



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

SIGNATURE AND DATE
DRAWN Randy Fox 7 ...
DRFTG CHK ... 8-11-77
APVD ... 8 11 77
... Belanger ...

NEXT ASSY | USED ON
APPLICATION
MATL
FINISH

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TITLE LOGIC DIAGRAM Z80 SIO

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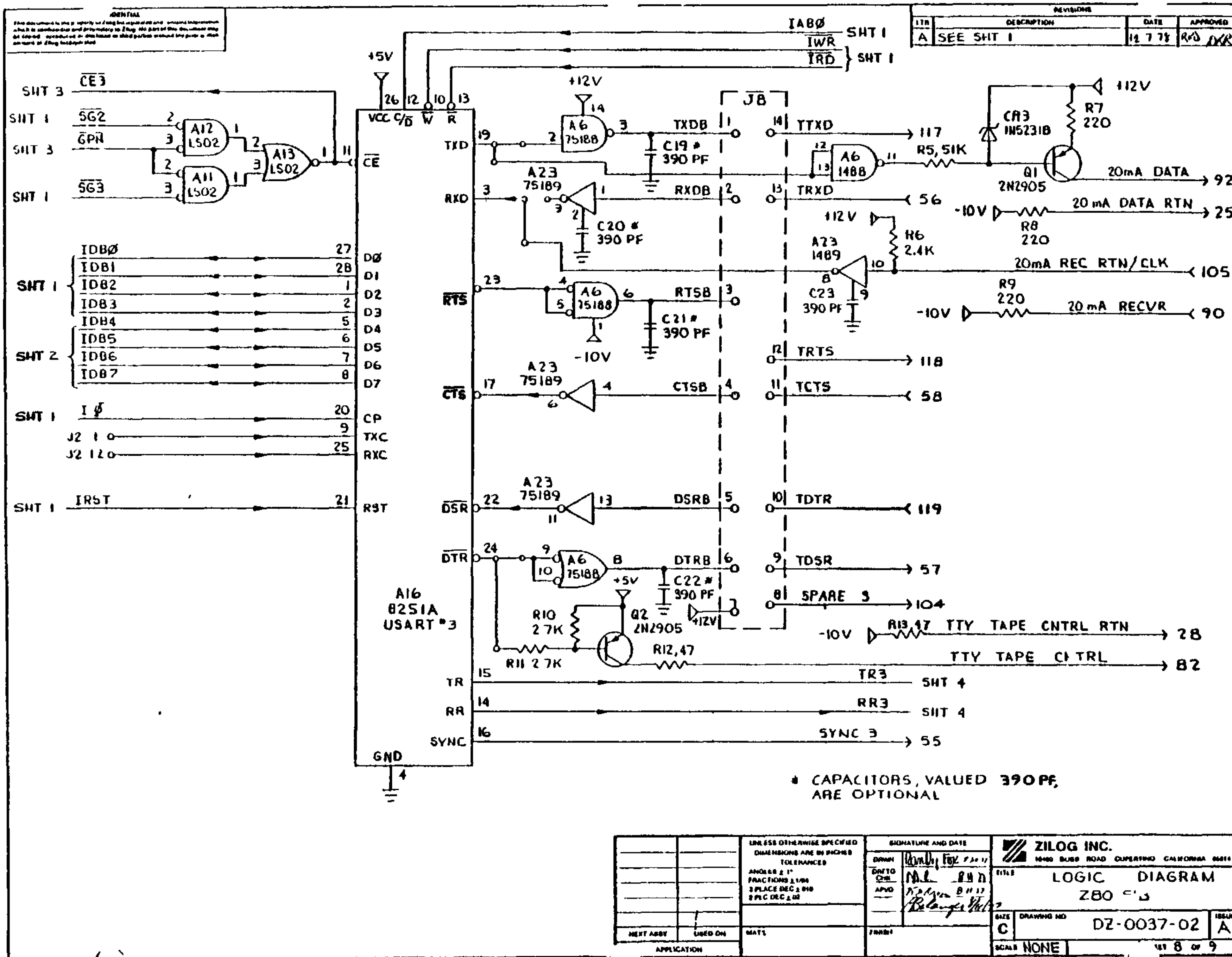
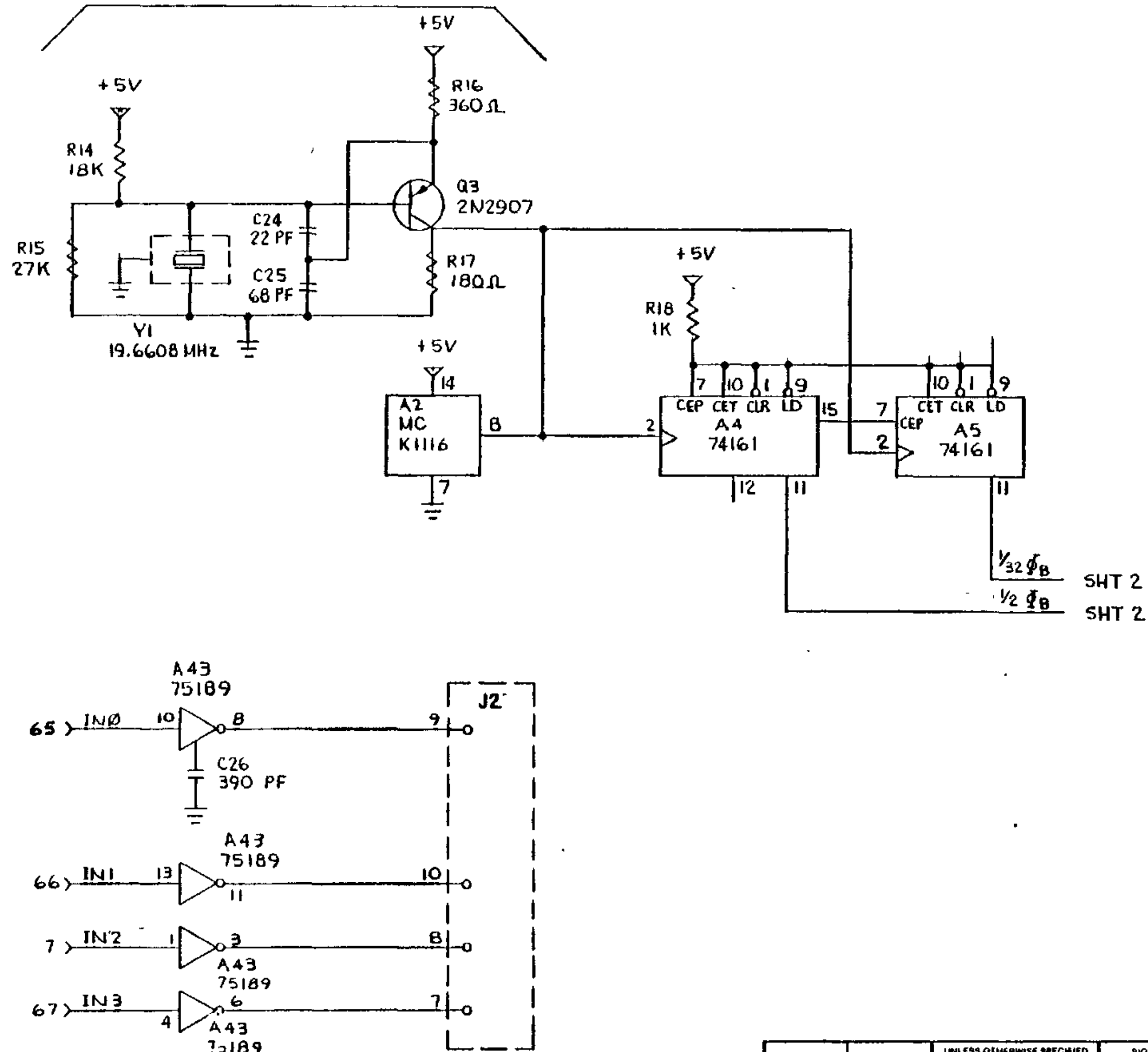
SCALE NONE | SHEET 7 OF 9



SHT 3
CE3
SHT 1
SG2
SHT 3
GPN
SHT 1
SG3
A12 LS02
A11 LS02
A13 LS02
IABØ
SHT 1
IWR
IRD
SHT 1
+5V
VCC C/D W R
CE
IDBØ
IDB1
IDB2
IDB3
IDB4
IDB5
IDB6
IDB7
SHT 1
SHT 2
DØ D1 D2 D3 D4 D5 D6 D7
SHT 1
I Ø
J2 1
J2 12
CP
TXC
RXC
SHT 1
IRST
RST
A16
8251A
USART #3
GND
TXD
RXD
RTS
CTS
DSR
DTR
TR
RR
SYNC
+12V
A6 75188
A23 75189
TXDB
C19 # 390 PF
RXDB
C20 # 390 PF
RTSB
C21 # 390 PF
-10V
CTSB
DSRB
DTRB
C22 # 390 PF
+5V
Q2 2N2905
R10 2.7K
R11 2.7K
R12,47
J8
TTXD
TRXD
TRTS
TCTS
TDTR
TDSR
SPARE 3
A6 1488
A23 1489
C23 390 PF
R5, 51K
R6 2.4K
CR3 1N5231B
R7 220
Q1 2N2905
R8 220
R9 220
R13,47
20mA DATA
20 mA DATA RTN
20mA REC RTN/CLK
20 mA RECVR
TTY TAPE CNTRL RTN
TTY TAPE CNTRL
TR3
RR3
SYNC 3
SHT 4
SHT 4
117
56
118
58
119
57
104
92
25
105
90
28
82
55
* CAPACITORS, VALUED 390PF, ARE OPTIONAL
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
A
SEE SHT 1
ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA
LOGIC DIAGRAM
Z80
DZ-0037-02
SIZE C
ISSUE A
SCALE NONE
SHT 8 OF 9
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
NEXT ASSY
USED ON
APPLICATION

LTR	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	2-7-78	RHb DKR

ALTERNATE OSCILLATOR



NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

MAT'L

FINISH

SIGNATURE AND DATE
DRWN
DWG [...] CHK
APVD

ZILOG INC. 10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM
Z80 SIB

SIZE	DRAWING NO	ISSUE
C	DZ-0037-02	A

SCALE NONE — SHEET 9 OF 9