

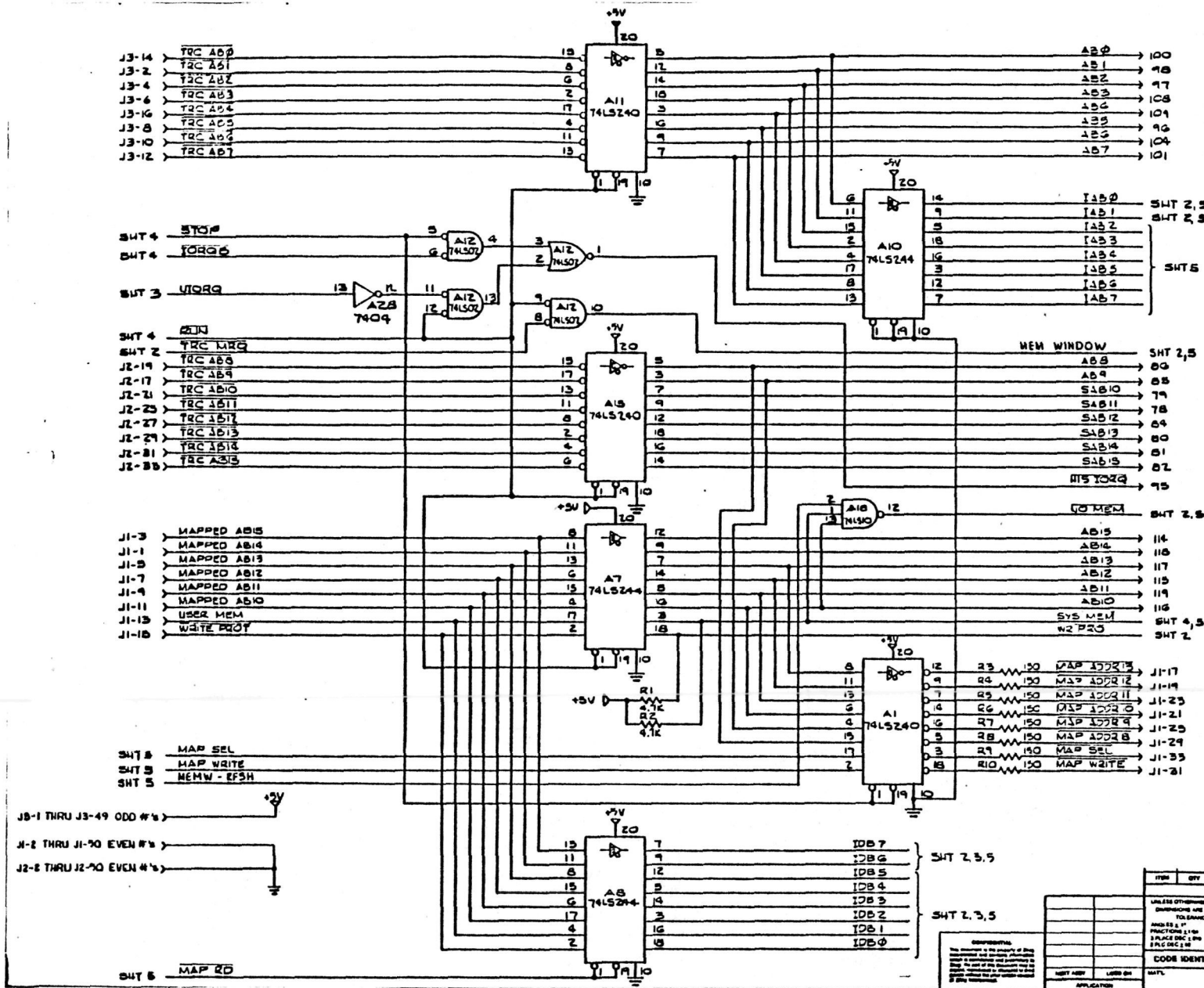
APPENDIX E  
LOGIC DIAGRAMS

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LOGIC DIAGRAMS, USER POD CONTROLLER

REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECN 01026	5-4-78	MSJ/22



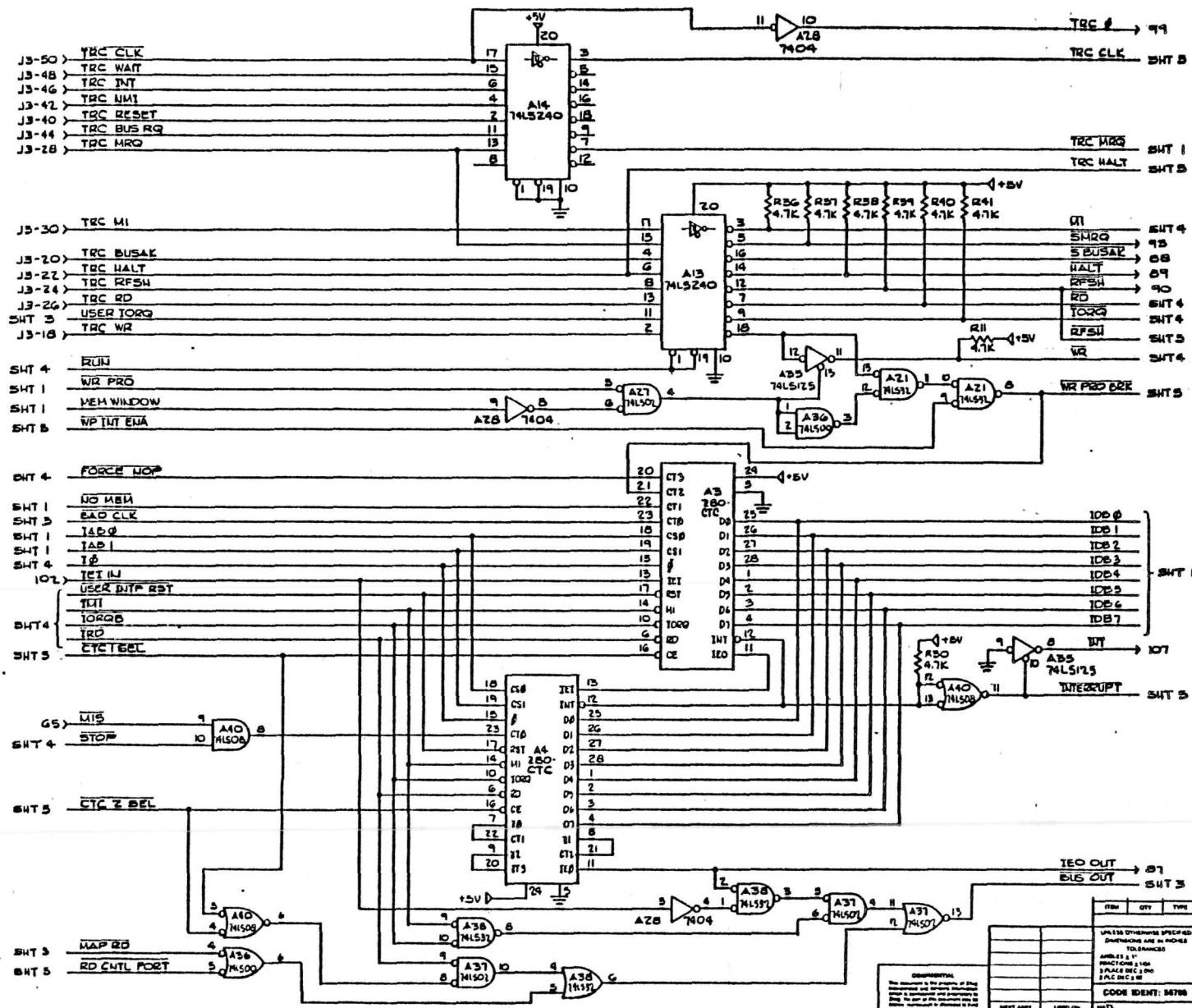
NOTES:  
 UNLESS OTHERWISE SPECIFIED:  
 1. RESISTORS ARE IN OHMS, 1/4 W, 5%.  
 2. CAPACITORS ARE IN MICROFARADS.

LAST REF DES USED			
A42	Z21	CRT	R46
REF DES NOT USED			
			R29

IC'S	
TYPE	SPARE
74LS244	A16-F
9602	A26-B
74LS175	441-D

ITEM	QTY	TYPE	GLOBAL PART NO	PARTS LIST	DESCRIPTION	REF DES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES						
DRAWN BY: 5-1-78						
CHECKED BY: 5-1-78						
DATE: 5-1-78						
SCALE: 1:1						
CODE IDENT: 58708						
Z8000 USER POD CONTROLLER						
REV	ISSUE NO	SCALE	SHEET		OF 5	
D	02-C055-02	1A				

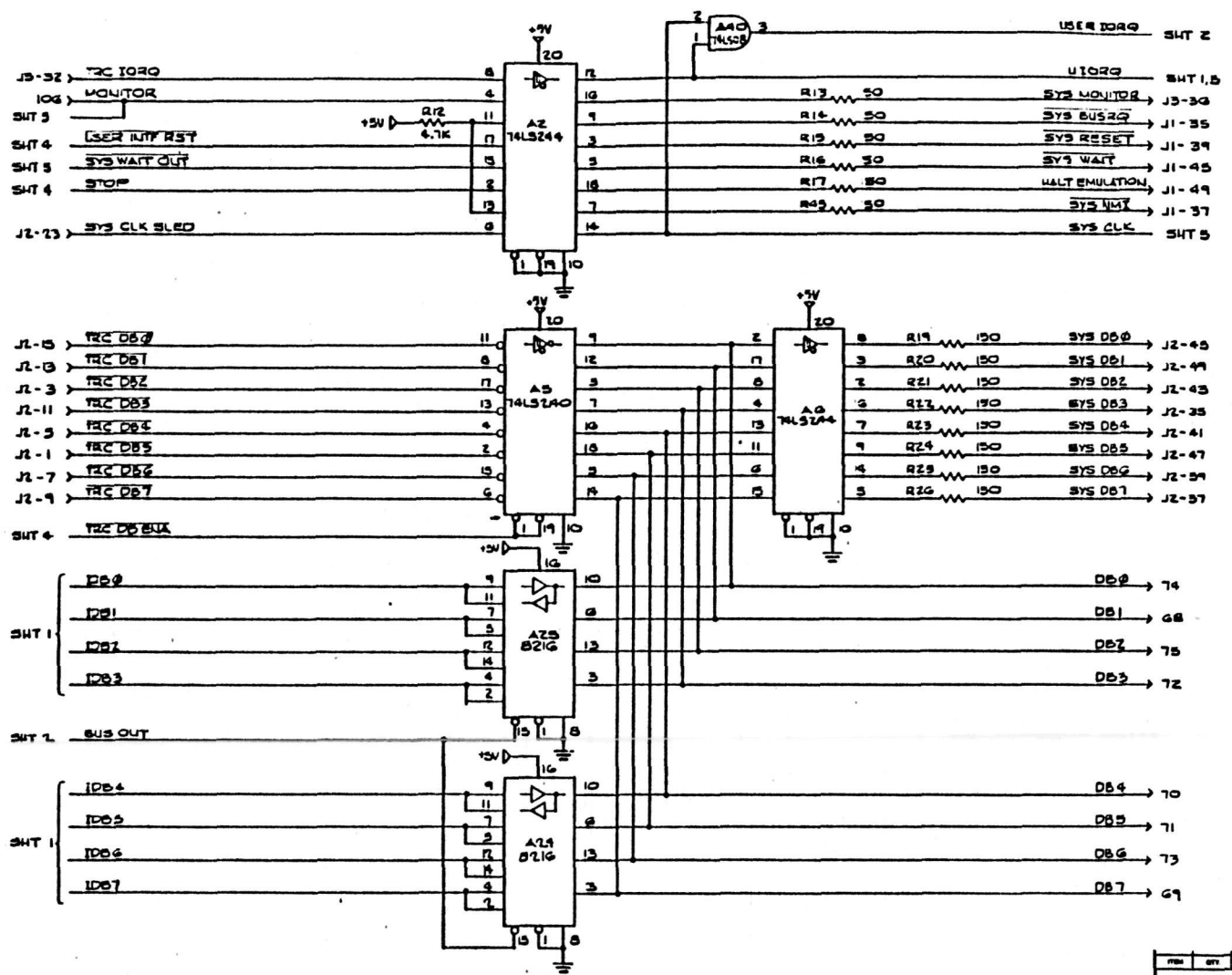
REV	DESCRIPTION	DATE	APPROVED
A	SEE SH1.1	9-4-77	1200/ML



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ITEM	QTY	TYPE	ZILOG PART NO.	DESCRIPTION	REP. DES.
PARTS LIST					
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES: .010, .005, .0025, .0015, .0010, .0005, .00025.					
SIGNATURE AND DATE: [Signature] 5-17-77					
TITLE: LOGIC DIAGRAM, USER ROD CONTROLLER					
CODE IDENT: 8678					
REV D					
DATE: 02-0055-02					
SCALE: SHEET 1 OF 3					

REV	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	5-4-73	DDO [Signature]

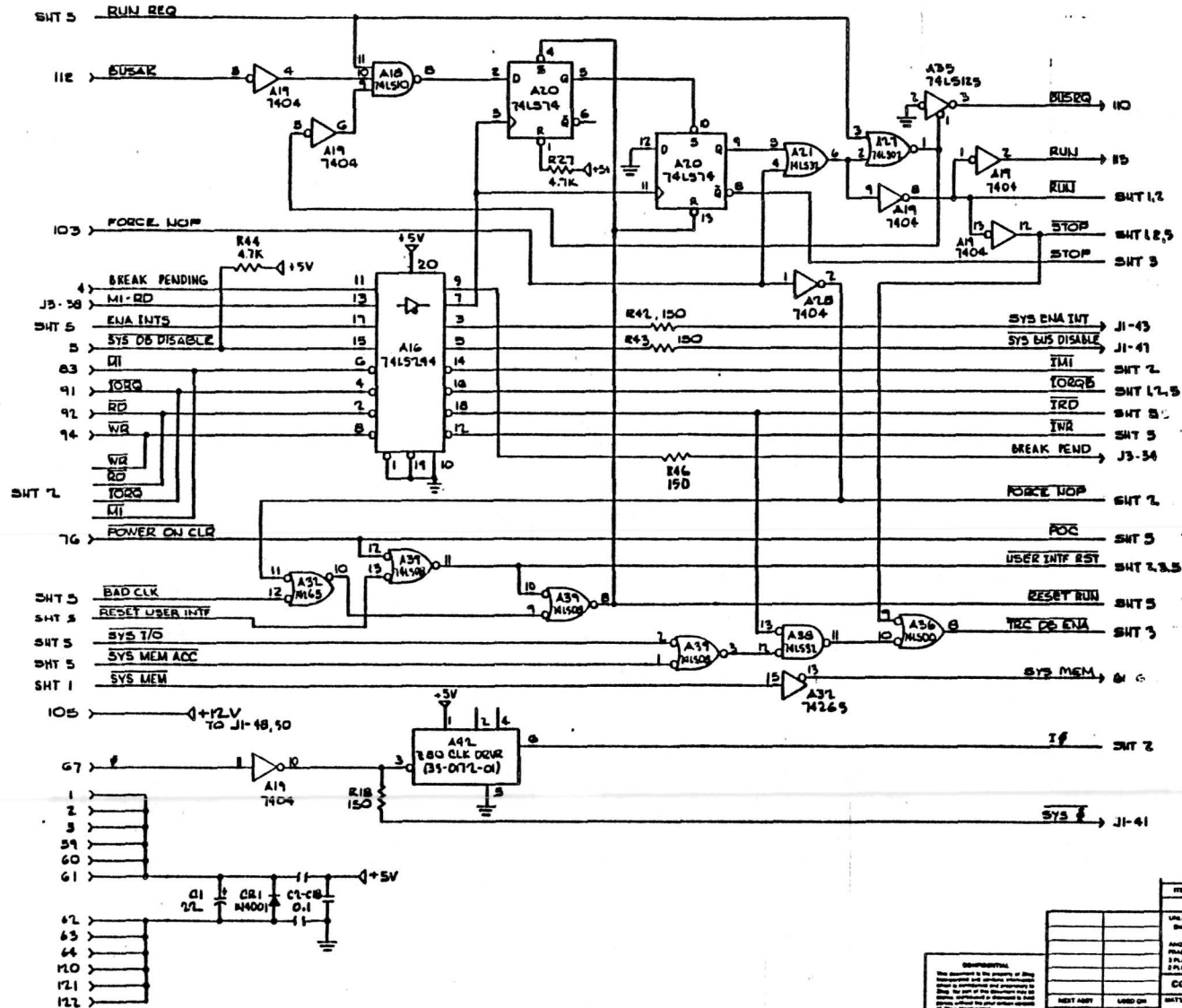


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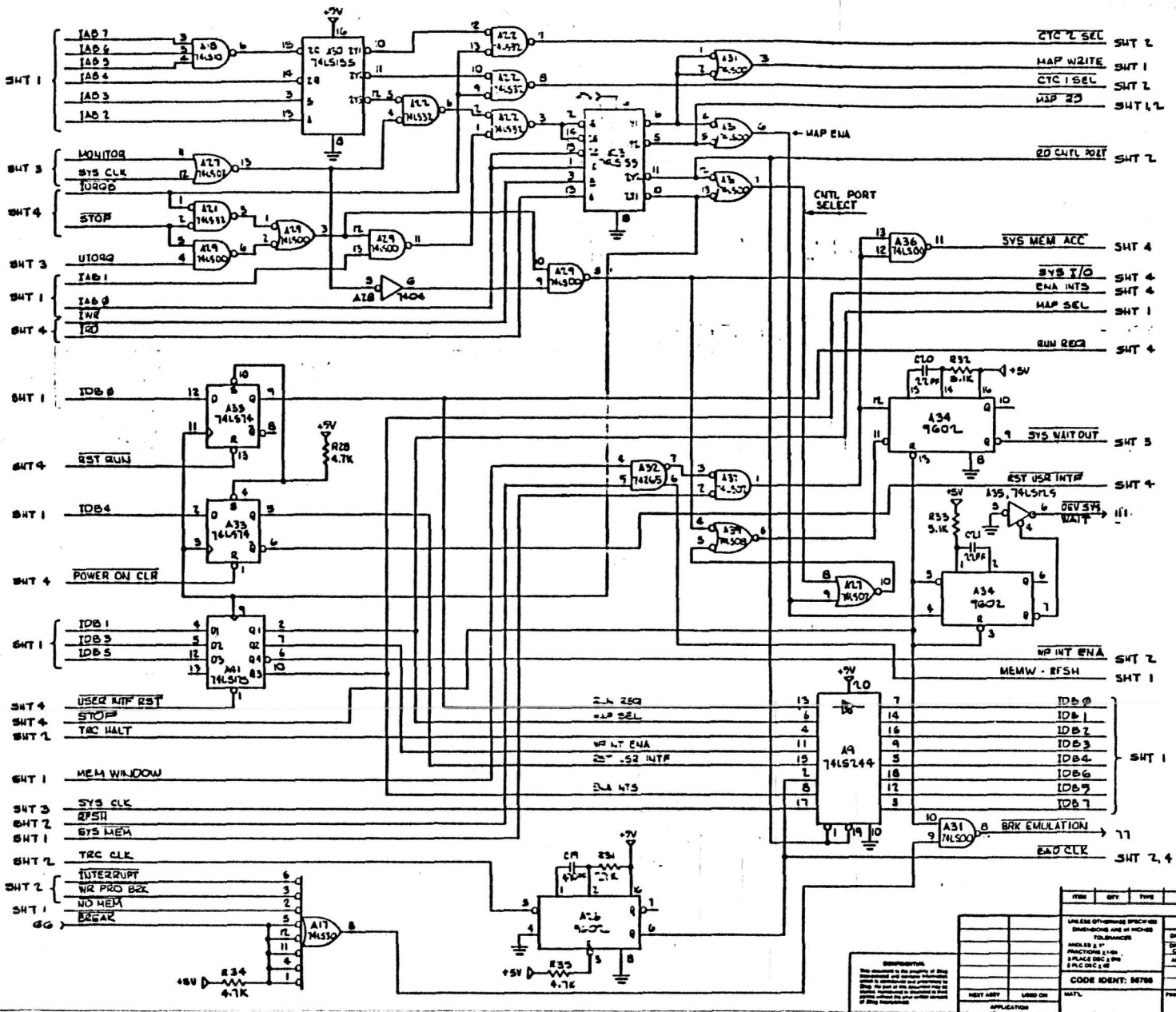
ITEM	QTY	TYPE	BLDG PART NO	DESCRIPTION	REV
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES			SHOW DATE AND DATE		
ANGLES 1:1			DATE 5-1-73		
FRACTIONS 1/16			BY [Signature]		
3 PLACE DECIMALS			CHECKED [Signature]		
PLC DEC 1/16			APPD [Signature]		
CODE IDENT: 86788			TITLE		
SIZE			DRAWING NO		
MATERIAL			D 02-0055-02		
APPLICATION			SCALE		
			SHEET 3 OF 5		

ZILOG INC.  
 3851 BARR ROAD CLAYTON, CALIFORNIA 94516  
 LOGIC DIAGRAM  
 USER POD CONTROLLER

REV	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	6-4-74	[Signature]



ITEM	QTY	TYPE	DIAG PART NO.	DESCRIPTION	REF DES.
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES				SIGNATURE AND DATE	<b>ZILOG INC.</b> 1011 SAGE ROAD CLIPPING, CALIFORNIA 95040 TITLE
ANGLES 1:16 FRACTIONS 1/16 DECIMALS 0.001 DIMENSIONS IN INCHES DIMENSIONS IN MILLIMETERS					
CODE IDENT: 04708 PART NO. USED ON APPLICATION				DATE: [Signature] 11/10/74 DESIGNED BY: [Signature] DRAWN BY: [Signature]	TITLE <b>LOGIC DIAGRAM,          USER POD CONTROLLER</b>
PART NO. USED ON APPLICATION				CONTROLLING NO. [Signature] PART NO. [Signature]	PROJECT NO. <b>DE-0059-02</b> SHEET 4 OF 9



REV	DESCRIPTION	DATE	APPROVED
A	SEE SHT. 1	6-4-79	[Signature]

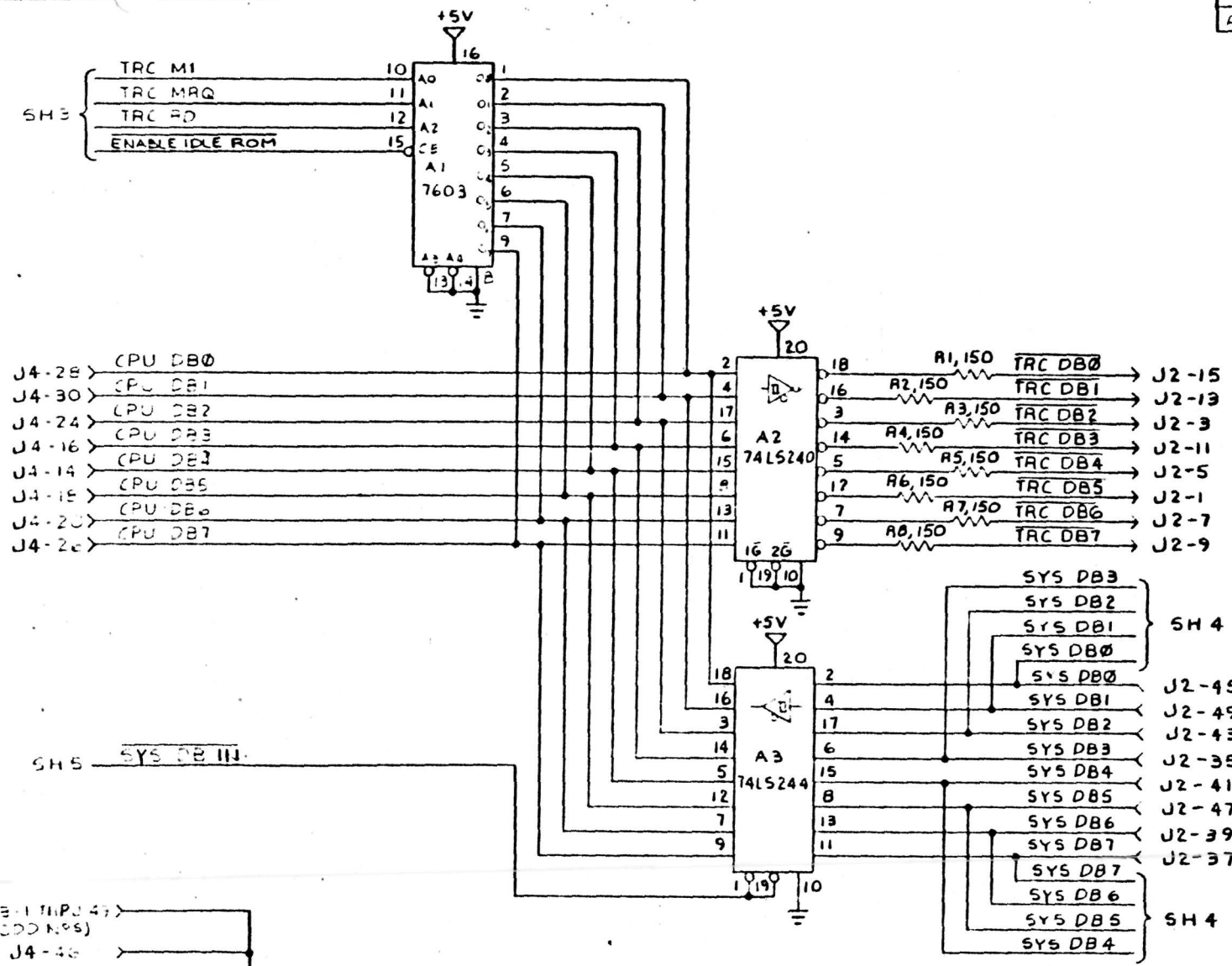
ITEM	QTY	TYPE	SOLE PART NO.	DESCRIPTION	REP DES.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES					
DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED					
FRANCE DRG 2-90					
FRANCE DRG 2-90					
FRANCE DRG 2-90					
CODE IDENT: 86788					
PARTS LIST					
SIGNATURE AND DATE					
DATE					
DRAWN BY					
CHECKED BY					
APPROVED BY					
TITLE					
ZILLOG INC.					
1811 BLAIR ROAD CLIPPING CALIFORNIA 92504					
DZ-0055-02 .A					
SHEET 5 OF 5					



LOGIC DIAGRAMS, USER POD

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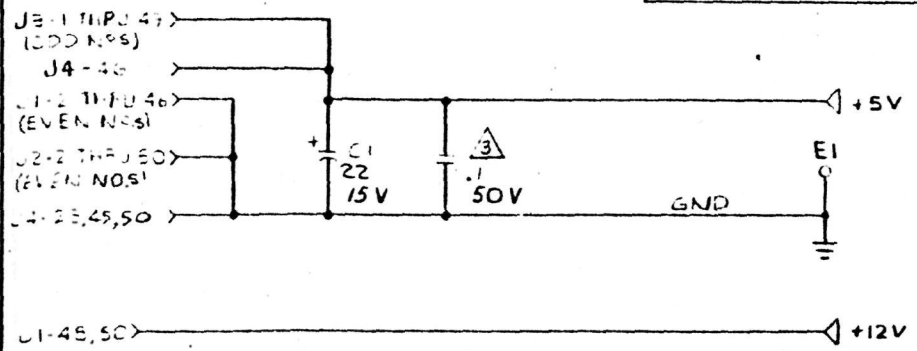
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
1	EAR 410, 480, 508, 509, 573, 623, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000	1-25-79	REK
A	RELEASE PER ECM 01010	4-23-79	REK



- NOTES - UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.
  2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
  3. -02 USES C2-C6 ; -05 USES C2-C17.

PEF DESC	
LAST USED	UNUSED
A28	
R74	R-0 44,62,65,69
TP1	

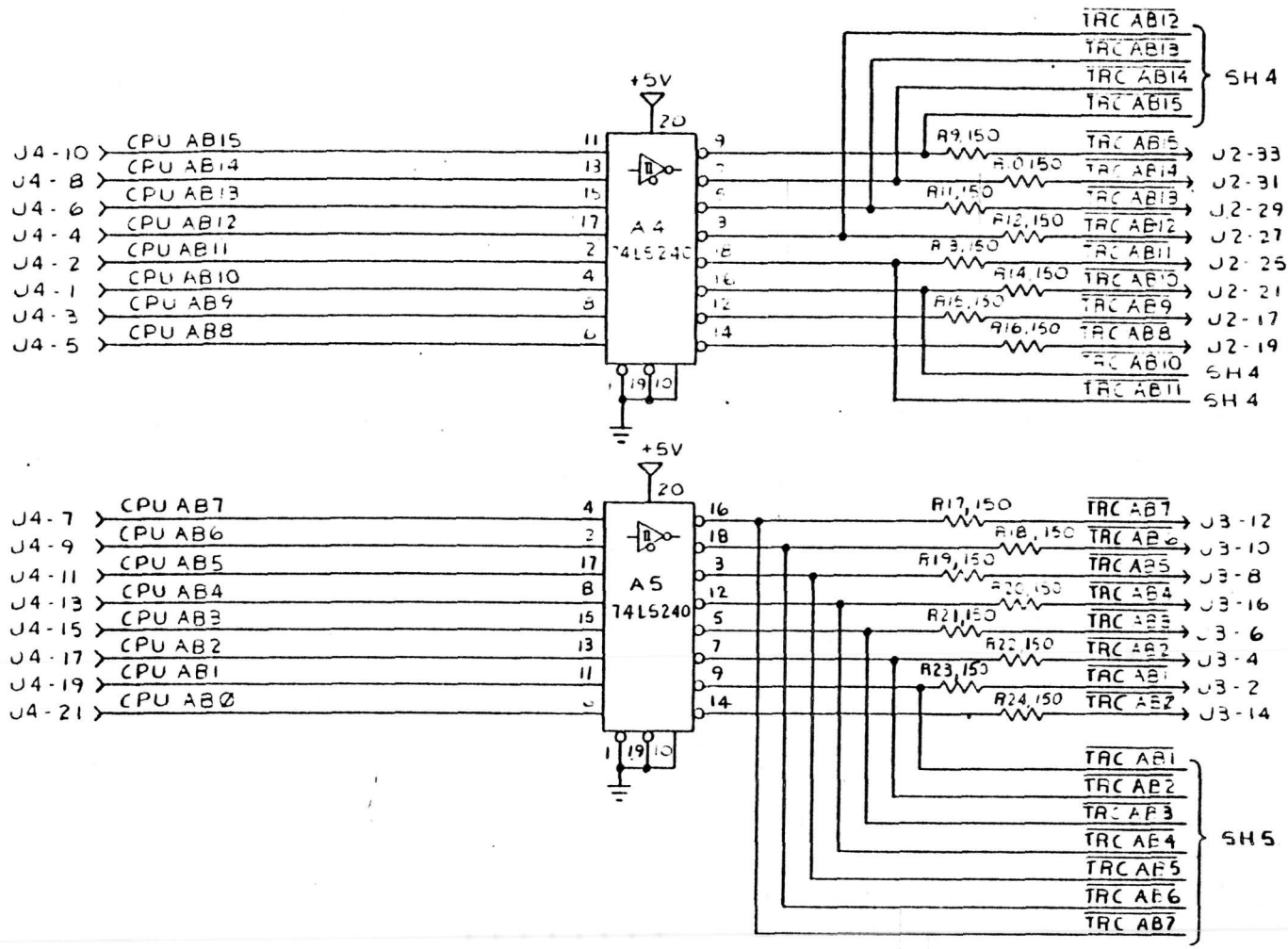
INTEGRATED CIRCUITS	
TYPE	SPARES
74LS08	2
7406	1
74LS32	2
74LS02	3



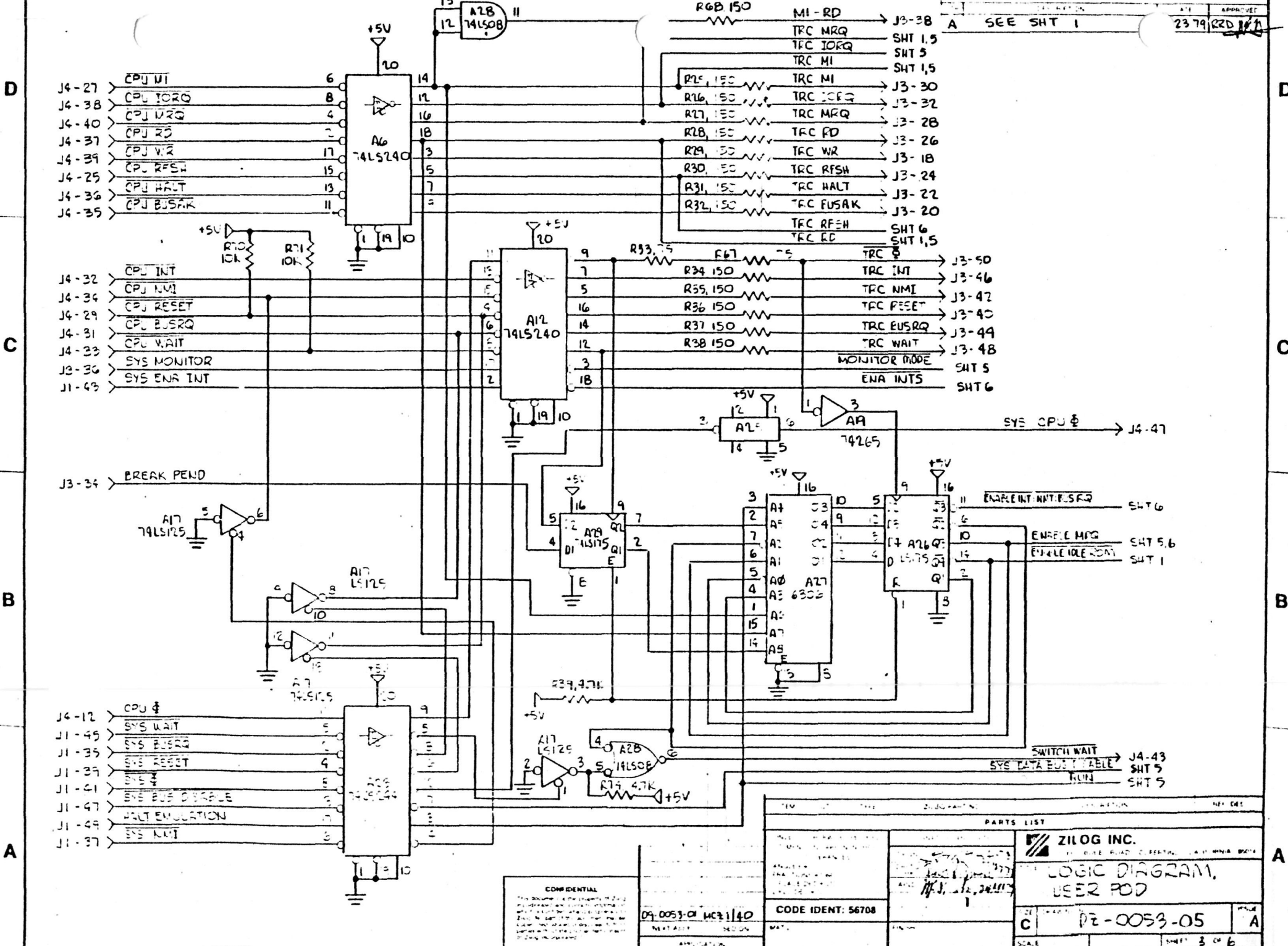
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED. ANGLE: 45° FRACTIONAL PART: PLACE DECIMAL POINT IN FRONT OF FRACTION. DIM: 0053-04-705-140 09-0053-03-705-14 NEXT ASSY: USED ON: MAT: FINISH: APPLICATION:	QUANTITIES INDICATED: DRAWN: P. J. L. R. 2/77 CHECKED: M. J. L. 2/77 DATE: 2/77 1	<b>ZILOG INC.</b> 3801 BIRCH AVE. CUPERTINO, CALIFORNIA 95014 <b>LOGIC DIAGRAM</b> <b>USER POD</b> SIZE: DRAWING: C DZ-0053-05 ISSUE: 1.4 SCALE: 100% SHEET: 1 OF 6
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REV	DESCRIPTION	DATE	APPROVED
A	SEE SH. 1	4-27-79 RRD	



SEE SH. 1	PLATE NUMBER SPECIFIED	DATE	<b>ZILOG INC.</b> 1400 BISHOP ROAD GUNTERVILLE, CALIFORNIA 95014
	USED ON	TITLE	
APPLICATION	MATERIAL	FINISH	SIZE: DRAWING NO. <b>DZ-0073-05</b> ISSUE <b>A</b> SCALE: <b>1:1</b> SHEET 2 OF 6



SEE SHT 1

<p>J4-27 CPU INT</p> <p>J4-38 CPU IORQ</p> <p>J4-40 CPU MRQ</p> <p>J4-37 CPU RD</p> <p>J4-39 CPU V.R</p> <p>J4-25 CPU RFSH</p> <p>J4-36 CPU WAIT</p> <p>J4-35 CPU BUSRQ</p>	<p>J4-32 CPU INT</p> <p>J4-34 CPU NMI</p> <p>J4-29 CPU RESET</p> <p>J4-31 CPU BUSRQ</p> <p>J4-23 CPU WAIT</p> <p>J3-36 SYS MONITOR</p> <p>J1-45 SYS ENR INT</p>	<p>J3-34 BREAK PEND</p>	<p>J4-12 CPU <math>\Phi</math></p> <p>J1-45 SYS WAIT</p> <p>J1-35 SYS BUSRQ</p> <p>J1-39 SYS RESET</p> <p>J1-41 SYS <math>\Phi</math></p> <p>J1-47 HLT EMULATION</p> <p>J1-49 SYS NMI</p> <p>J1-37</p>	<p>J3-38 MI-RD</p> <p>J3-30 TRC MRQ</p> <p>J3-32 TRC IORQ</p> <p>J3-28 TRC MRQ</p> <p>J3-26 TRC RD</p> <p>J3-18 TRC WR</p> <p>J3-24 TRC RFSH</p> <p>J3-22 TRC WAIT</p> <p>J3-20 TRC FUSAK</p> <p>SHT 6 TRC RFEH</p> <p>SHT 1,5 TRC EE</p> <p>J3-50 TRC <math>\Phi</math></p> <p>J3-46 TRC INT</p> <p>J3-47 TRC NMI</p> <p>J3-40 TRC RESET</p> <p>J3-44 TRC BUSRQ</p> <p>J3-48 TRC WAIT</p> <p>SHT 5 MONITOR MODE</p> <p>SHT 6 ENR INTS</p> <p>J4-47 SYS CPU <math>\Phi</math></p> <p>SHT 6 ENABLE INT NMI BUSRQ</p> <p>SHT 5,6 ENABLE MRQ</p> <p>SHT 1 ENABLE IORQ</p> <p>J4-43 SWITCH WAIT</p> <p>SHT 5 SYS DATA BUS ENABLE</p> <p>SHT 5 RUN</p>
---	---	-------------------------	--	---

REV	DATE	DESCRIPTION	BY	CHK
1.0				

<b>PARTS LIST</b>	
<i>(Empty)</i>	<i>(Empty)</i>
<b>ZILOG INC.</b>	
10000 BAYVIEW AVENUE, SAN JOSE, CALIF. 95131	
<b>LOGIC DIAGRAM,</b>	
<b>USER POD</b>	
CODE IDENT: 56708	
PARTS	
SCALE	
C	A
PE-0053-05	SHEET 3 OF 6

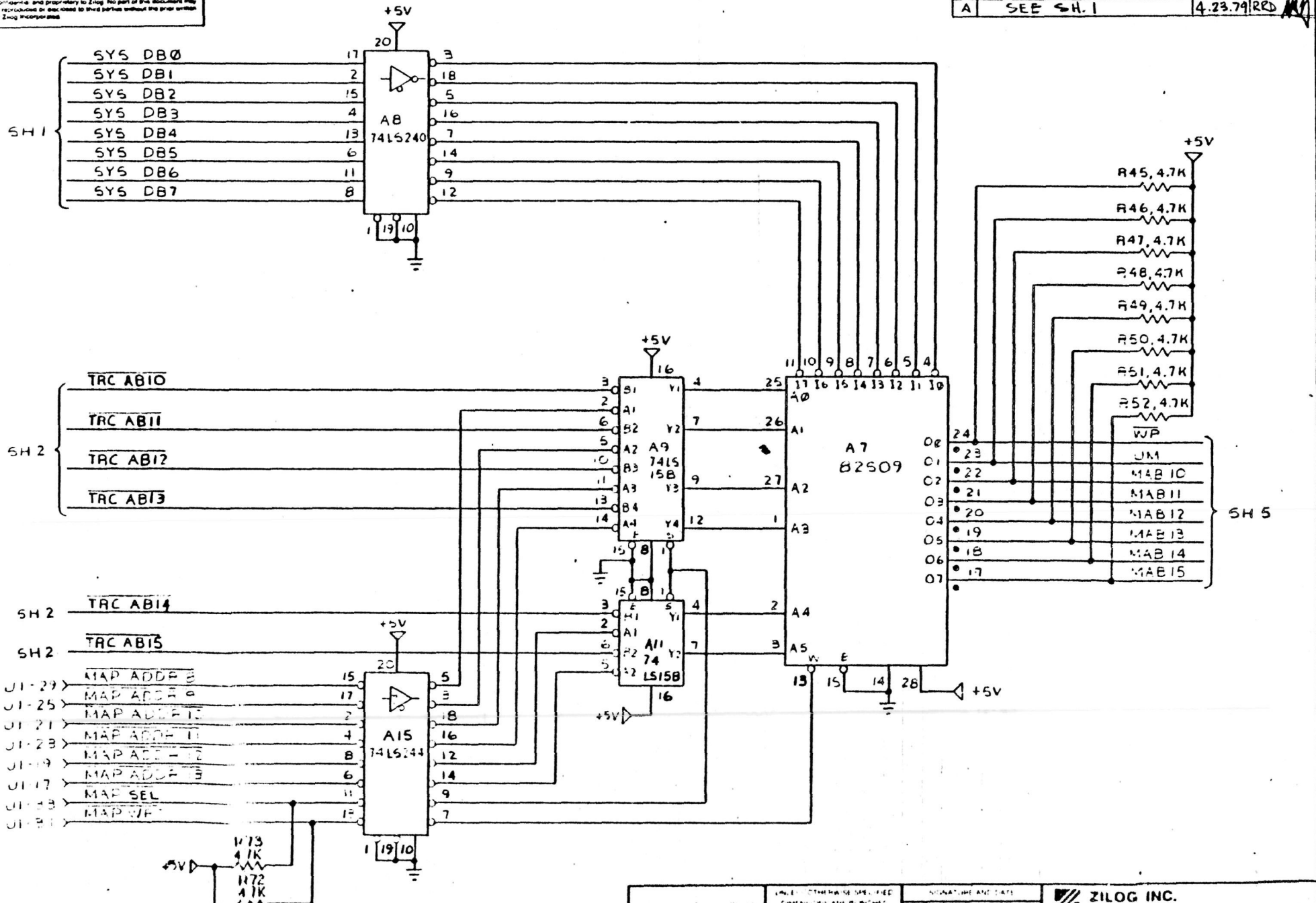
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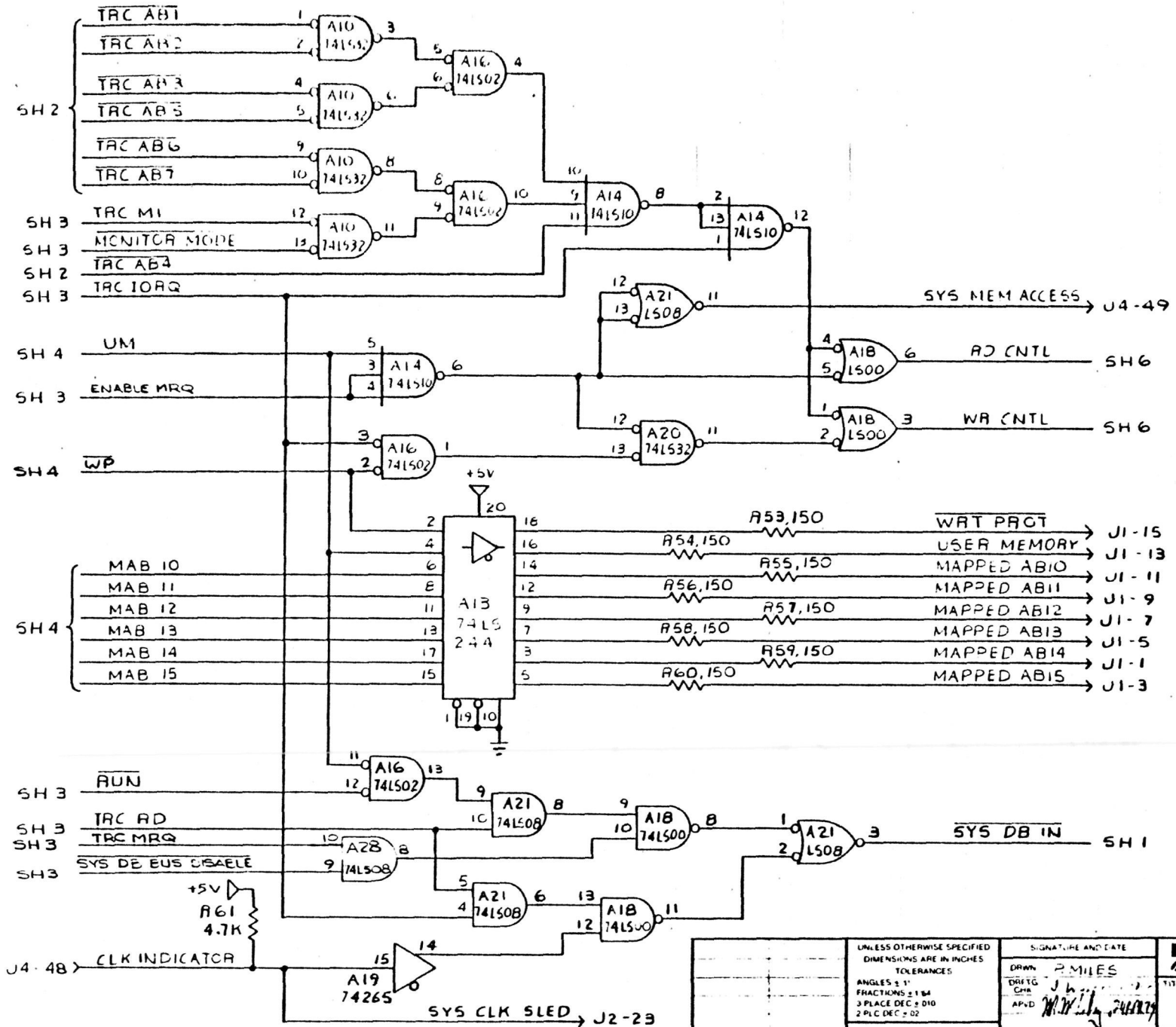
09-0053-01 MC21140

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REVISIONS		DATE	APPROVED
LTR	DESCRIPTION		
A	SEE SH.1	4.23.79	RED



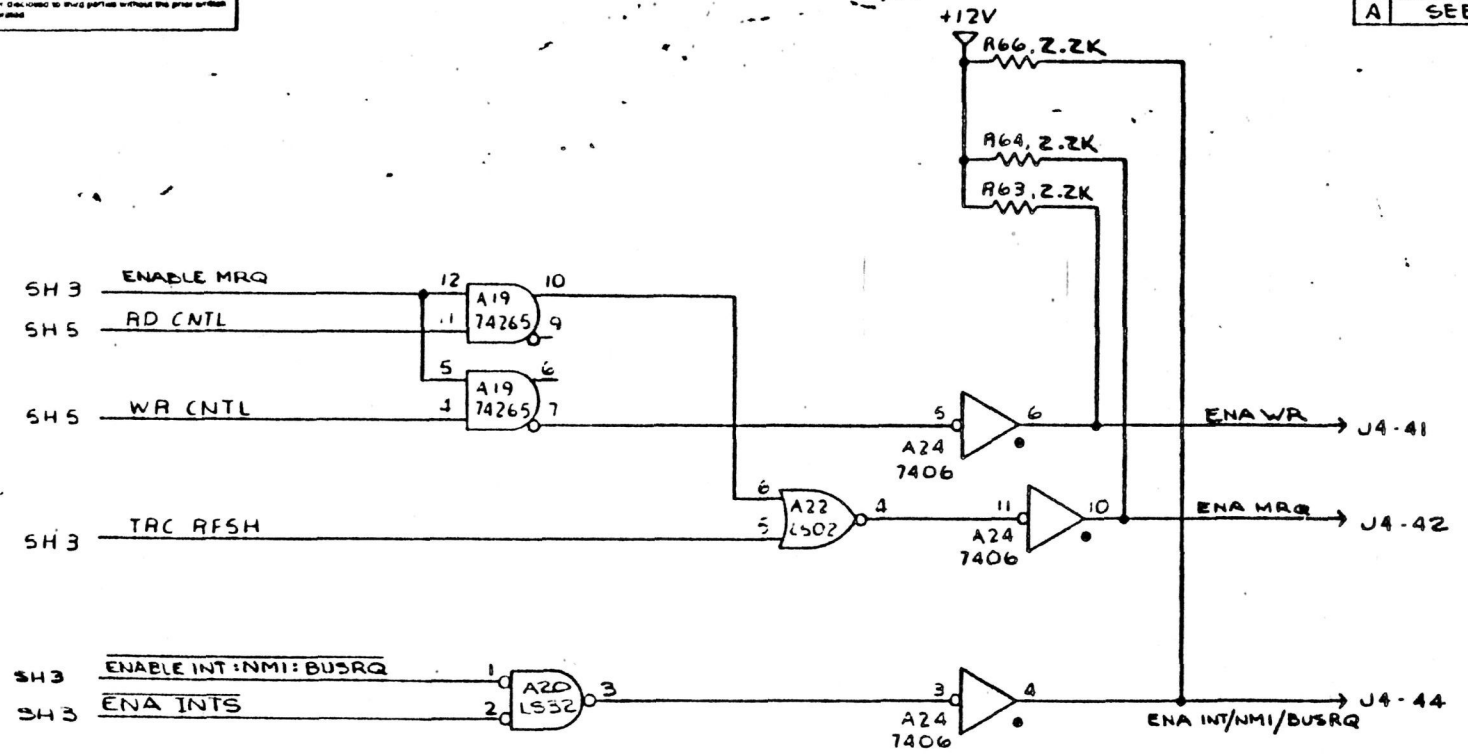
SEE SH.1	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES	SIGNATURE AND DATE	<b>ZILOG INC.</b> 1000 AVENUE 86, CUPERTINO, CALIFORNIA 95014
	ANGLE ± 1°	DRAWN: F. J. FEL CHECKED: CHA DATE: 11/17/79	
SS: _____	MATL: _____	FINISH: _____	SIZE: C PART: DZ-0053 SCALE: 1:1 SHEET: 5 OF 6



SEE SH.1	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES:	SIGNATURE AND DATE	<b>ZILOG INC.</b> 1046C BUBB ROAD CUPERTINO CALIFORNIA 95014
	ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± 0.10 2 PLACE DEC ± 0.2	DRAWN: PMILES CHECKED: [Signature] APVD: [Signature]	
NEXT ASSY	USE: ON	FINISH	SIZE: C DRAWING NO: <b>DZ-0053-05</b> SCALE: _____
APPLICATION	MATL		ISSUE: A SHEET 5 OF 6

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	SEE SH.1	4.23.79	RRD



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 1° FINISHES AS SHOWN UNLESS OTHERWISE SPECIFIED	SIGNATURE AND DATE DRAWN: P.MILES DATE: 4/23/79 APP: M. DIAL, 24817	<b>ZILOG INC.</b> 1440 BUREAU ROAD CUPERTINO CALIFORNIA 95010
	SEE SH.1 ASSY USED ON: APPLICATION:	FINISH:
MATERIAL:		PAGES: 6 OF 6

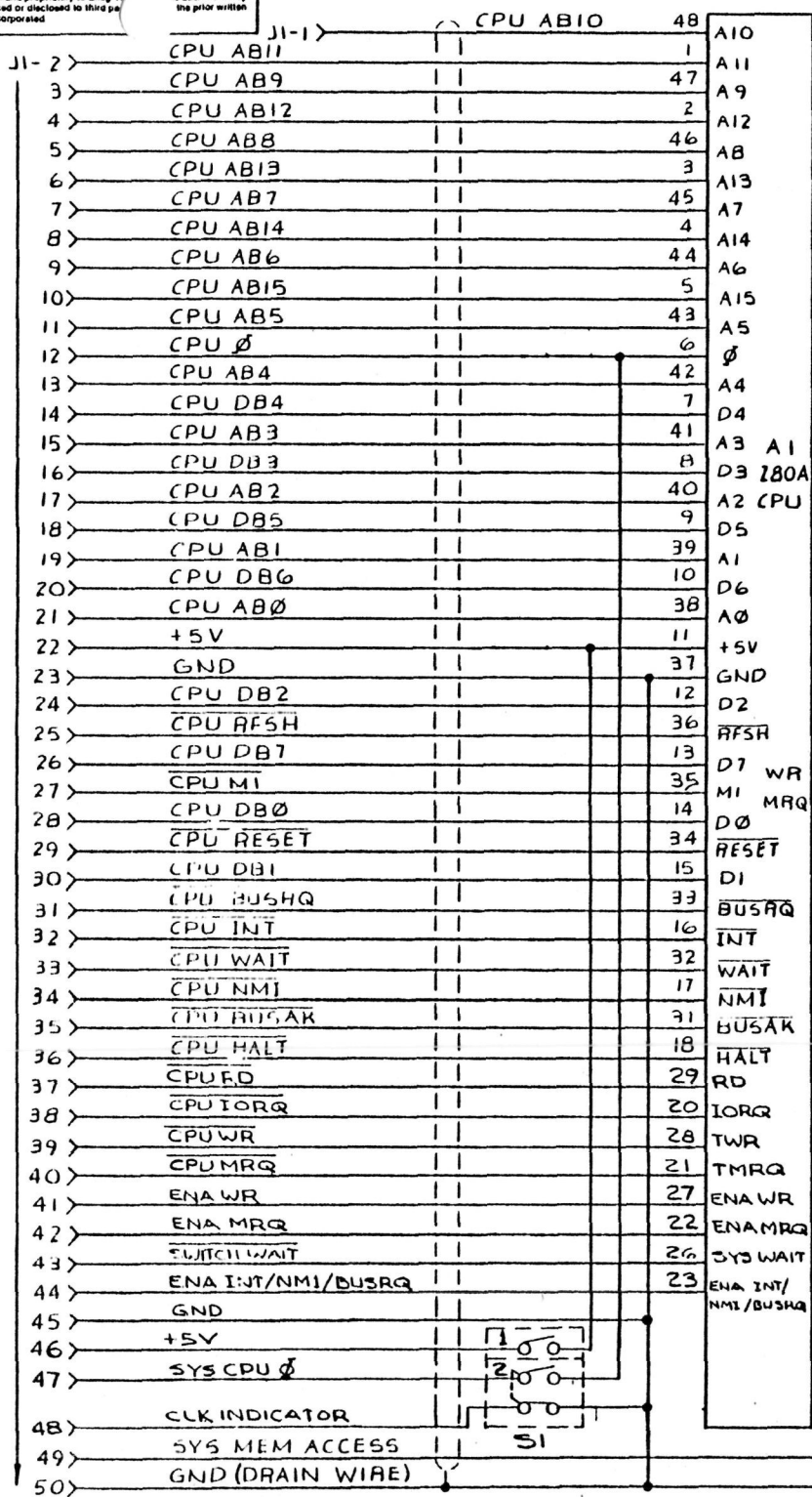
LOGIC DIAGRAMS, EMULATOR



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Outgoing information is information in this document may be the prior written

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE ECN 00385	3-78	RLF
B	ECN 00527	10-27-78	RKD
C	ECN 00634	11-20-78	A2
D	ECN 00786	1-3-79	RKD



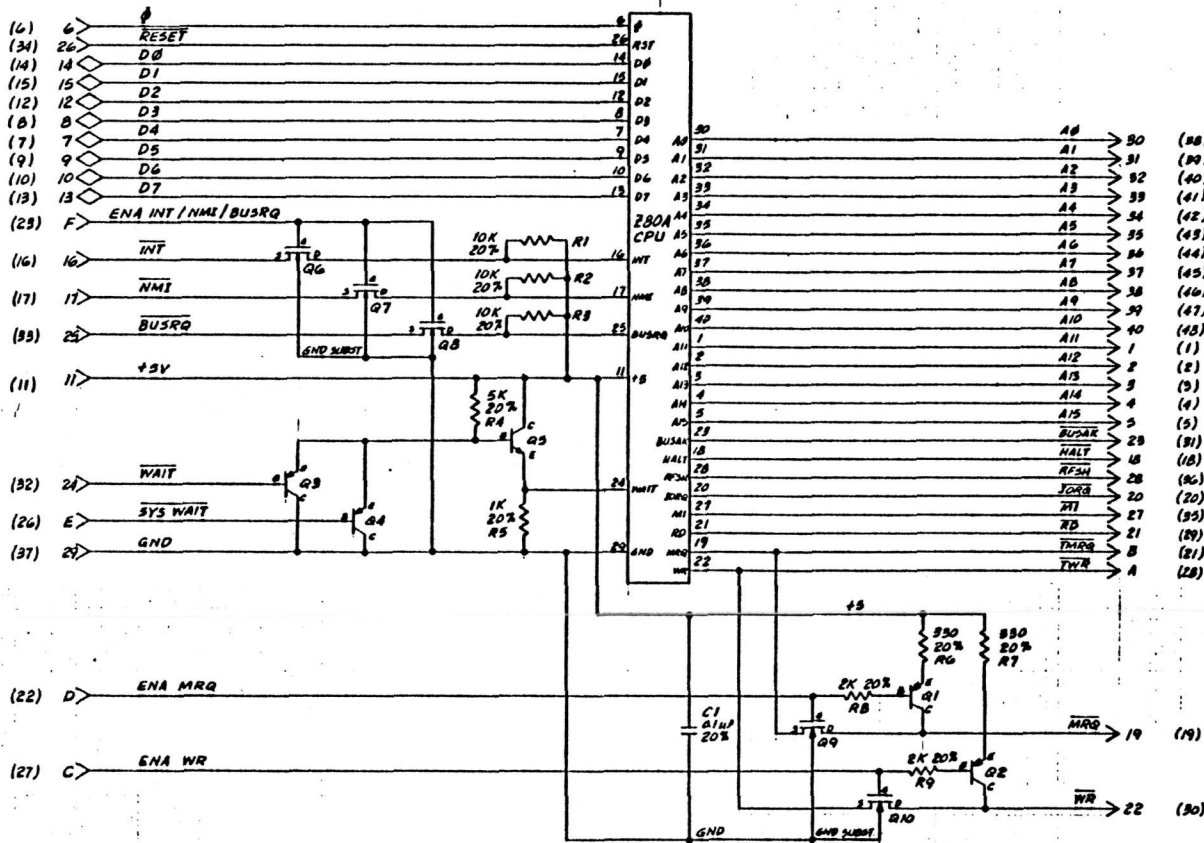
- 30 USER WR
- 19 USER MRQ
- 24
- 25

⊙ SYS MEM  
⊙ GND

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES		SIGNATURE AND DATE		<b>ZILOG INC.</b> 10400 BUBB ROAD, CUPERTINO, CALIFORNIA 95014	
ANGLES ± 1°	FRACTIONS ± 1/64	DRWN	P. MILES 10-1477	TITLE	
3 PLACE DEC ± 0.10	2 PLC DEC ± 0.2	DRAFTG		LOGIC DIAGRAM	
		CHK		EMULATOR	
		APVD	<i>[Signature]</i>	SIZE	DRAWING NO.
				C	DZ-0056-02
				SCALE	NONE
NEXT ASSY	USED ON	MATL:	FINISH	ISSUE	D
APPLICATION				SHEET	1 OF 1

LOGIC DIAGRAMS, Z-80A CPU EMULATOR (HYBRID)

REV	DESCRIPTION	DATE	APPROVED
D1	ECN 00315	12-7-78	912



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTS LIST

RESISTORS

CAPACITORS

ALL PINS PREASSIGNED TO STANDARD 48 PIN DIP AS INDICATED. PACKAGE PIN # IN ( ). PIN SPACING: 0.100 X 0.600 MM. NOM. PIN LENGTH: 0.330 IN. NOM.

2. MARK:

ZILOG Z80A CPU EMULATOR 33-0171-01

MARK WITH LOT NUMBER  
REV. A NO LOT, LOT 01 AND LOT 02  
REV. B NONE MADE  
REV. C NONE BUILT  
REV. D LOT 3 AND UP

3. Q1 AND Q2 2N3546

Q3 AND Q4 2N2907, 2N2907A, 2N2944, 2N2944A, 2N2945, 2N2945A, 2N2946, 2N2946A

Q5 2N2222, 2N2222A

Q6 THROUGH Q10 SIGNETICS SDS800B MOS FET SWITCH ARRAY

4. PINS H AND G NOT USED (24) AND (25)

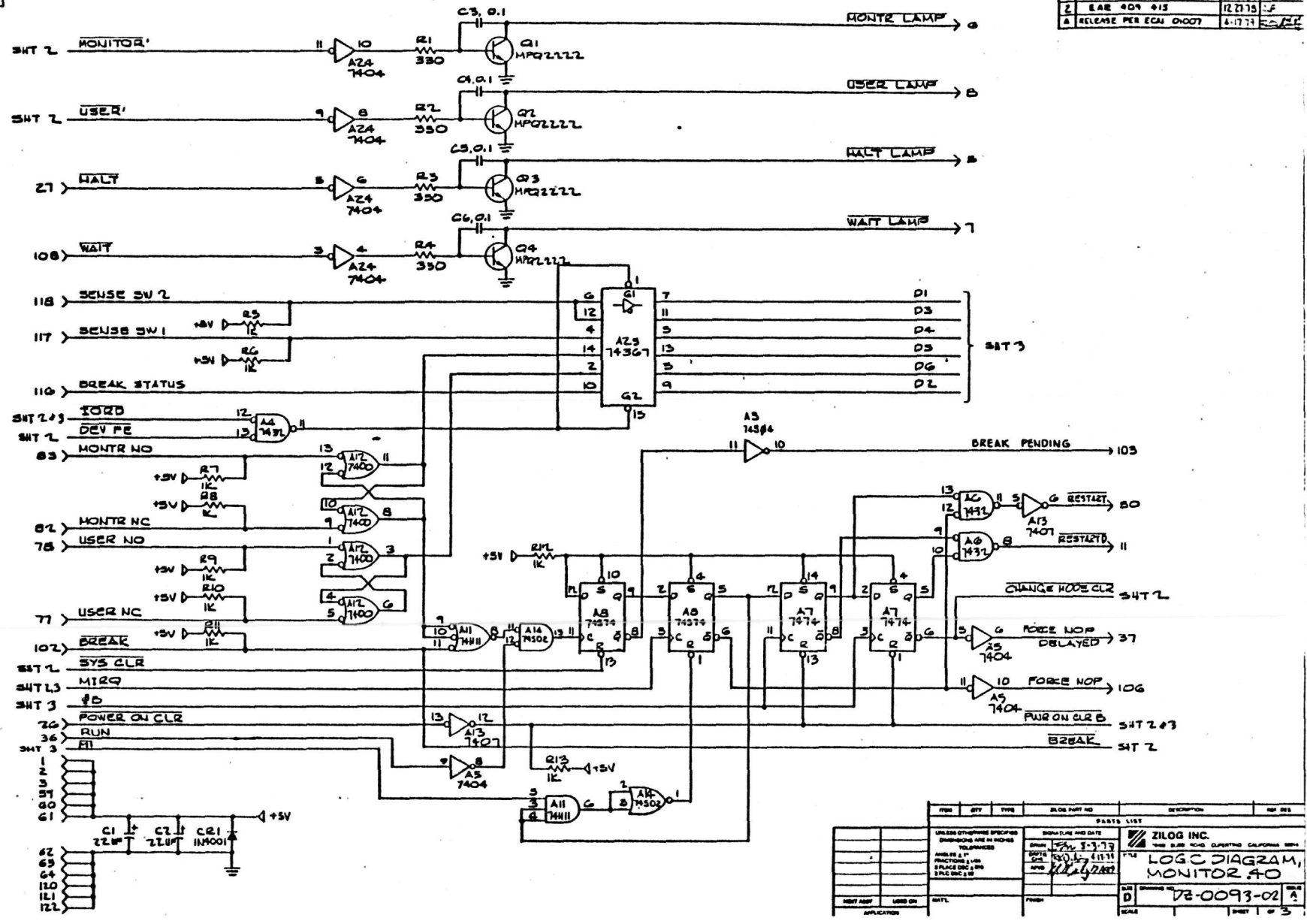
ITEM	QTY	TYPE	ZILOG PART NO.	DESCRIPTION	REV. USE
PARTS LIST					
UNLESS OTHERWISE SPECIFIED			SIGNATURE AND DATE		
DIMENSIONS ARE IN INCHES			TOLERANCES		
ANGLES ± 1°			DATE: 12/7/78		
FRACTIONS 2/16			DRAWN BY: [Signature]		
SPACE DEC. 1/16			CHECKED BY: [Signature]		
PLC DEC. 1/16			DATE: 12/7/78		
CODE IDENT: 88708			TITLE: Z80A CPU EMULATOR		
NEXT ASSY			SIZE: D		
LIND ON			DRAWING NO: 33-0171-01		
DATE:			SCALE: NONE		
APPLICATION:			SHEET 1 OF 1		

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LOGIC DIAGRAMS, MONITOR.40

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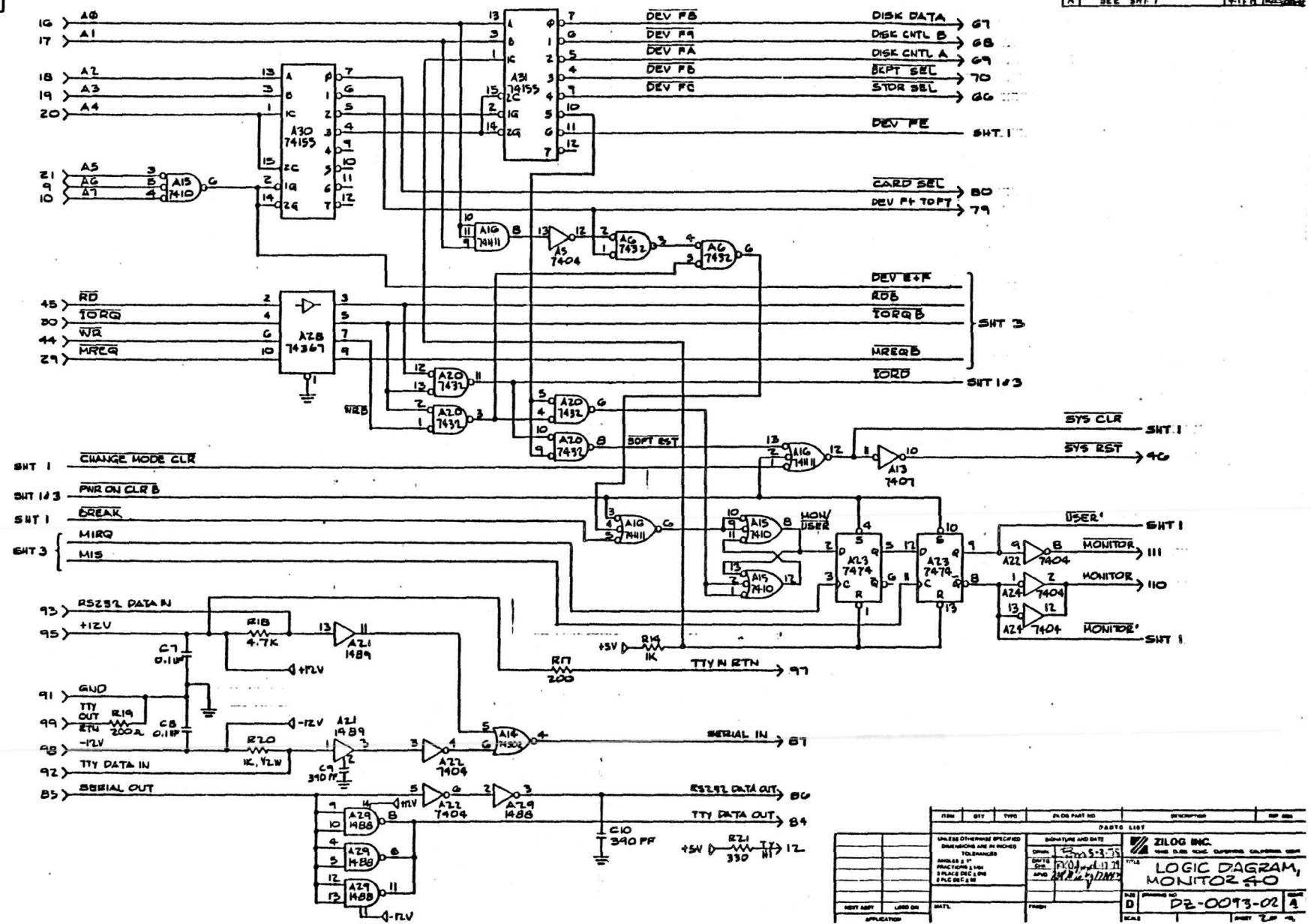
REV	DESCRIPTION	DATE	APPROVED
1	EAR 283 319	11-9-73	RO
2	EAR 409 #13	12-27-75	JF
A	RELEASE PER ECM 0007	4-17-77	CC/BJ



ITEM	QTY	TYPE	ZILOG PART NO.	DESCRIPTION	REV. DES.
<small>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES</small>					
			<small>DATE: 1-3-73 DRAWN: J. J. J.</small>		
			<small>APPROVED: J. J. J.</small>		
			<small>PLATE NO. 100</small>		
			<small>FILE NO. 100</small>		
<b>ZILOG INC.</b> <small>THE MICRO COMPUTER COMPANY</small> 2001 CENTRAL EXPRESSWAY, FOLSOM, CALIF. 95630					
<b>LOGIC DIAGRAM, MONITOR 40</b>					
DATE: 12-27-75					
DRAWN BY: J. J. J.					
CHECKED BY: J. J. J.					
PART NO. 78-0093-02					
SHEET 1 OF 3					

For a complete list of the components of this circuit, refer to the component list on page 2. Components are shown in this diagram as they are to be purchased. The manufacturer's name and part number are given in parentheses.

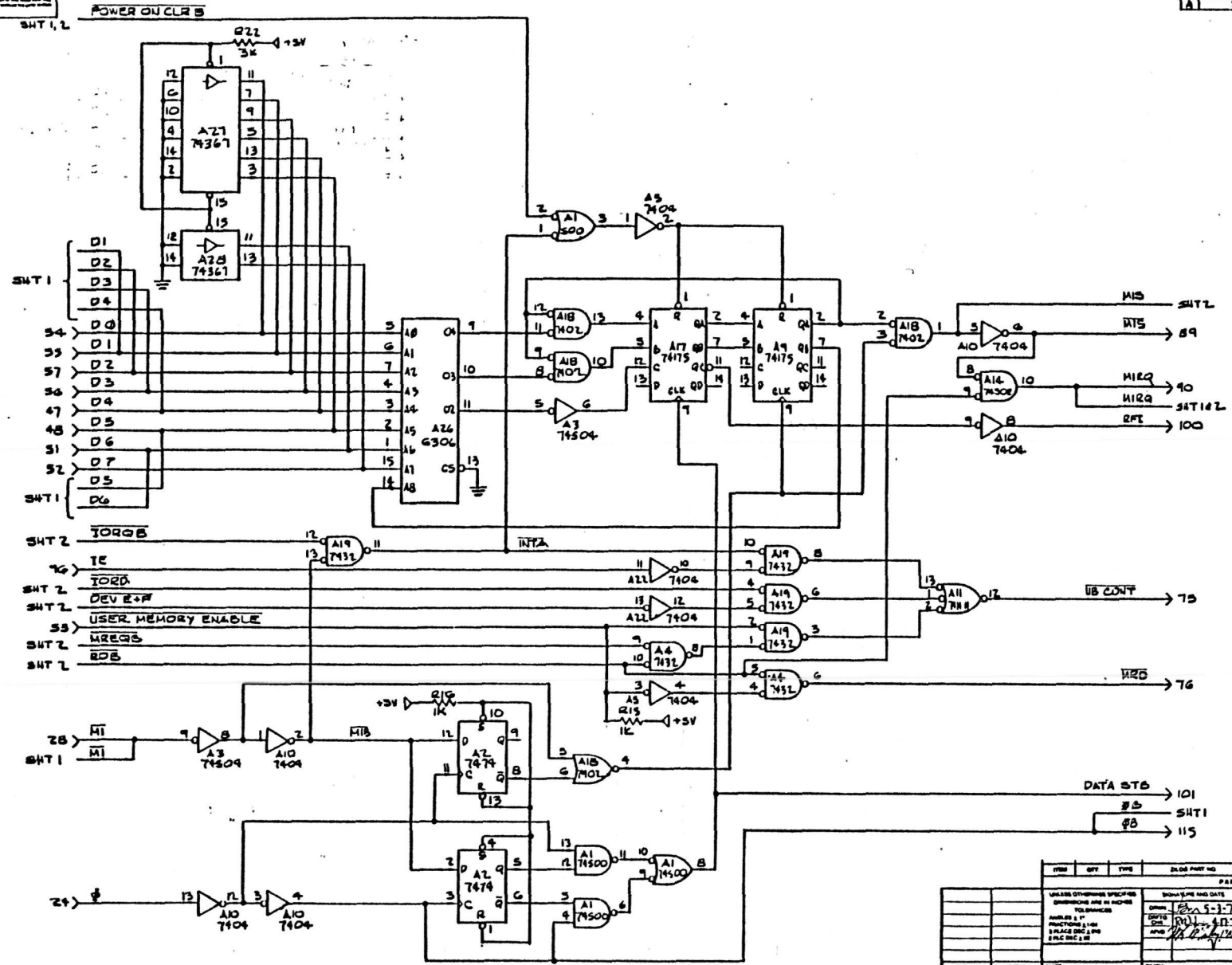
REV	DESCRIPTION	DATE	APPROVED
A	SEE SHT 1	4-17-74	RE-468



ITEM	QTY	TYPE	PN OR PART NO	DESCRIPTION	REF DES
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES					
DRAWN BY: <i>CS-3-75</i>					
CHECKED BY: <i>RD</i>					
DATE: <i>4-11-74</i>					
APPROVED BY: <i>DM</i>					
TITLE: <b>LOGIC DIAGRAM, MONITOR 40</b>					
PROJECT NO: <b>DE-0073-02</b>					
PAGE: <b>2</b>					

UNCLASSIFIED  
 AUTHORITY: NND 645014  
 DATE: 08-22-2014  
 BY: [Redacted]

REV	DESCRIPTION	DATE	BY
A	SEE SMT 1	4-7-78	[Redacted]



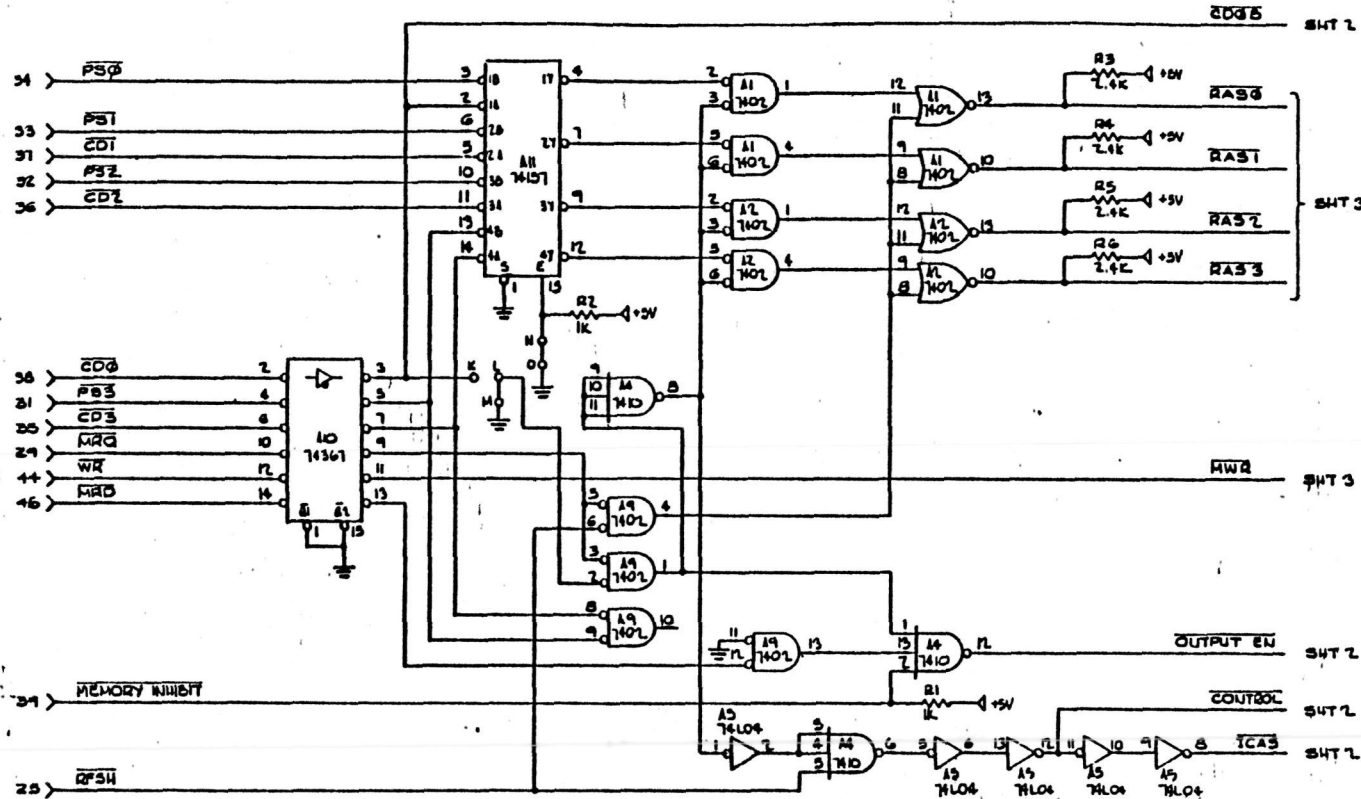
ITEM	QTY	TYPE	ZILOG PART NO.	PARTS LIST	DESCRIPTION	REV DES
VALUES OTHER THAN SPECIFIED INDICATED ARE IN PARENTHOSES						
TOLERANCES						
DIMENSIONS IN INCHES						
DIMENSIONS IN MILLIMETERS						
FUNCTIONS IN PARENTHOSES						
PLACE DIMENSIONS IN PARENTHOSES						
ELECTRICAL SYMBOLS						
DATE: 5-1-76						
DRAWN: [Redacted]						
CHECKED: [Redacted]						
APPROVED: [Redacted]						
TITLE: LOGIC DIAGRAM, MONITOR #0						
PART NO: DZ-C093-02 1						
PAGE: 3 OF 3						

LOGIC DIAGRAMS, MEMORY 25



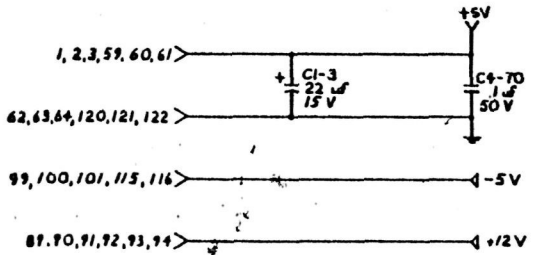
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECN 00320	7-1-78	W.E. [Signature]
B	ECN 00462	4-16-79	ROB [Signature]



NOTES: UNLESS OTHERWISE SPECIFIED  
 1. ALL RESISTOR VALUES ARE IN OHMS. 1/4W, 5%  
 2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

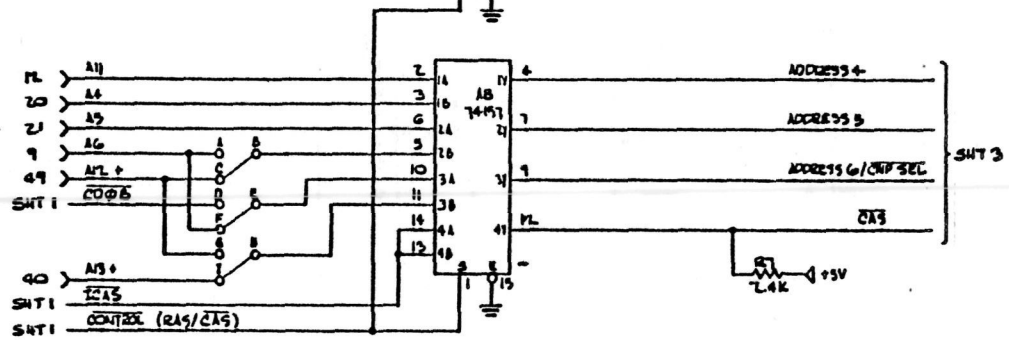
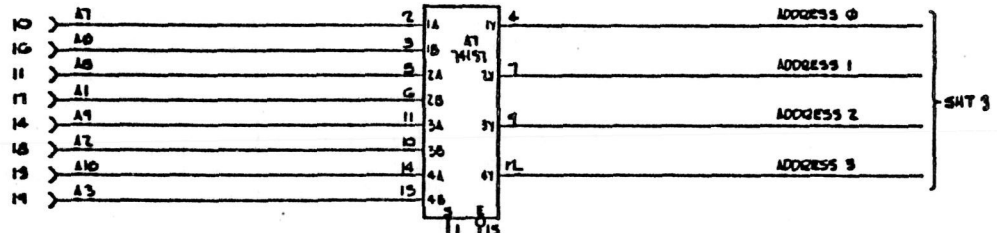
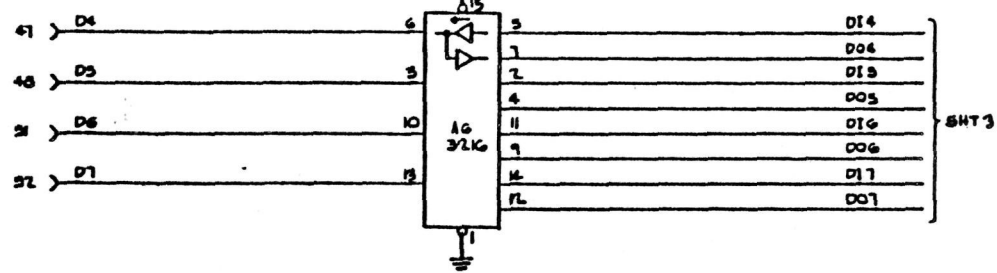
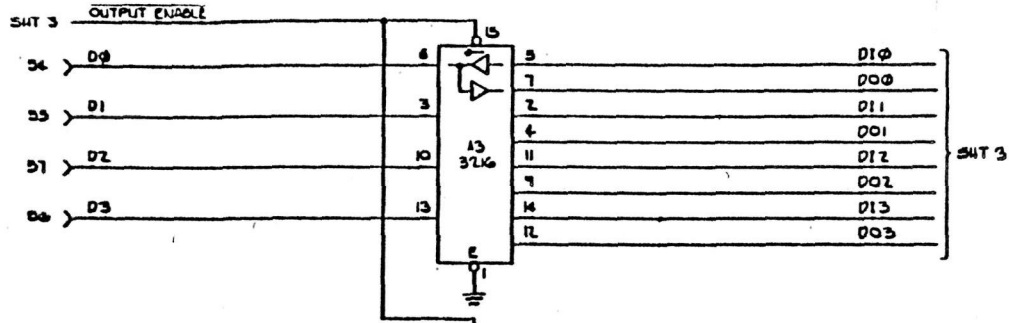
REF. DESIG.	
LAST USED	UNUSED
A43	
C70	
A7	



ITEM	QTY	TYPE	SILOS PART NO.	DESCRIPTION	REF. DESIG.
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES					
SIGNATURE AND DATE: [Signature] 6-23-78 TITLE: LOGIC DIAGRAM, MEMORY 25 DRAWN BY: [Signature] CHECKED BY: [Signature] DATE: 8-95-1/80 PART NO.: 07-000-0-805-1155 SCALE: 1:1 SHEET: 1 OF 3					

REVISIONS

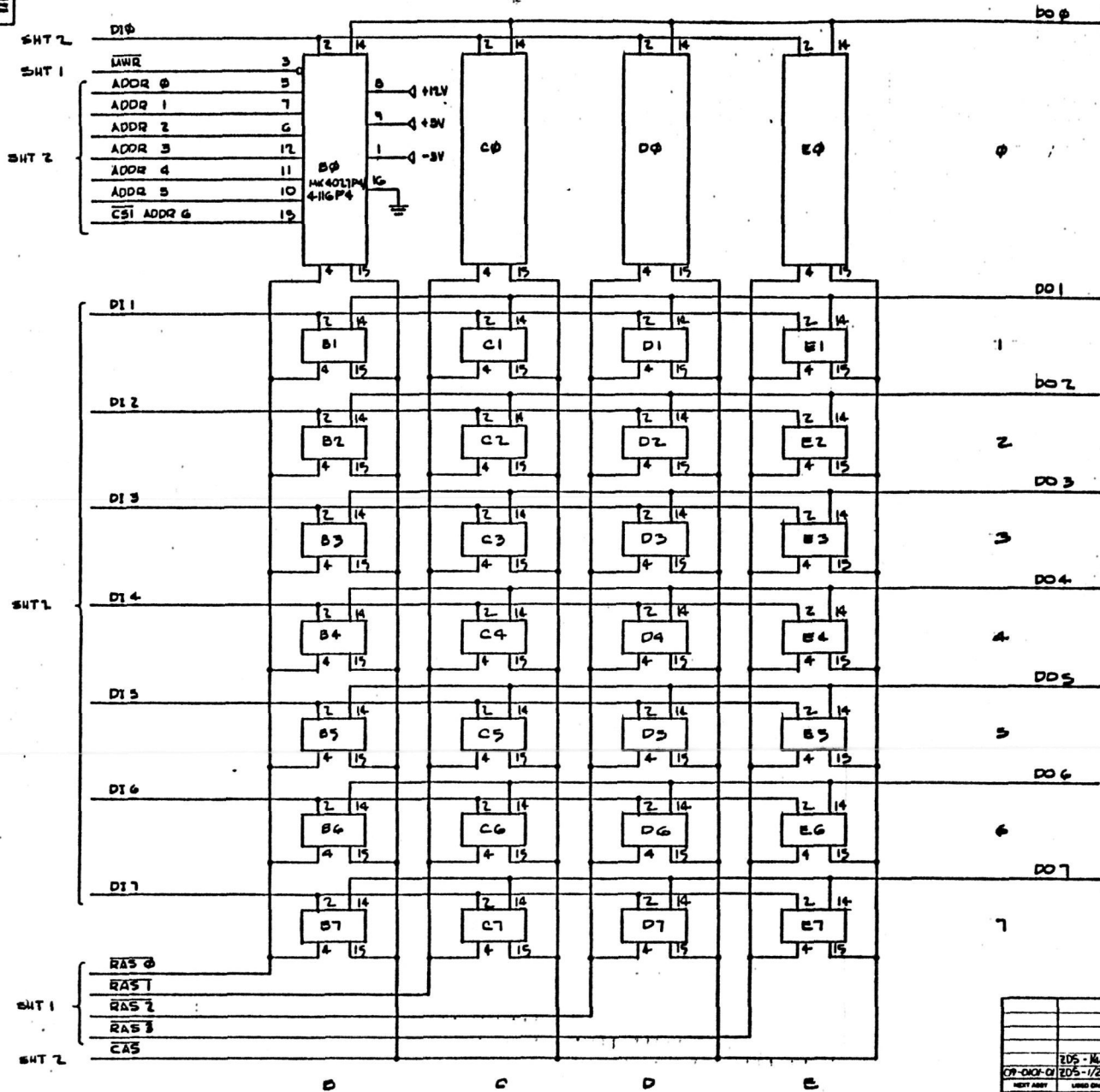
REV	DESCRIPTION	DATE	BY
B	SEE SH1 1	4-4-79	DT/25



ITEM	QTY	TYPE	BLDG PART NO.	DESCRIPTION	REF DES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TO FRACTIONS					
DRAWING AND DATE					
SIGNED: 6-19-79					
DATE: 4-4-79					
BY: DT/25					
TITLE: LOGIC DIAGRAM, MEMORY 25					
PARTS LIST					
ZILOG INC. 1045 BLUE ROAD CLAYTON, CALIFORNIA 94520					
DRAWING NO: 02-0101-01					
SCALE: SHEET 2 OF 3					

Not to be used in any program of integrated circuits unless specifically approved by the manufacturer. The user is responsible for the proper use of any integrated circuit.

REV	DESCRIPTION	DATE	APPROVED
1	SEE SHT 1	4.16.71	REB/BJT



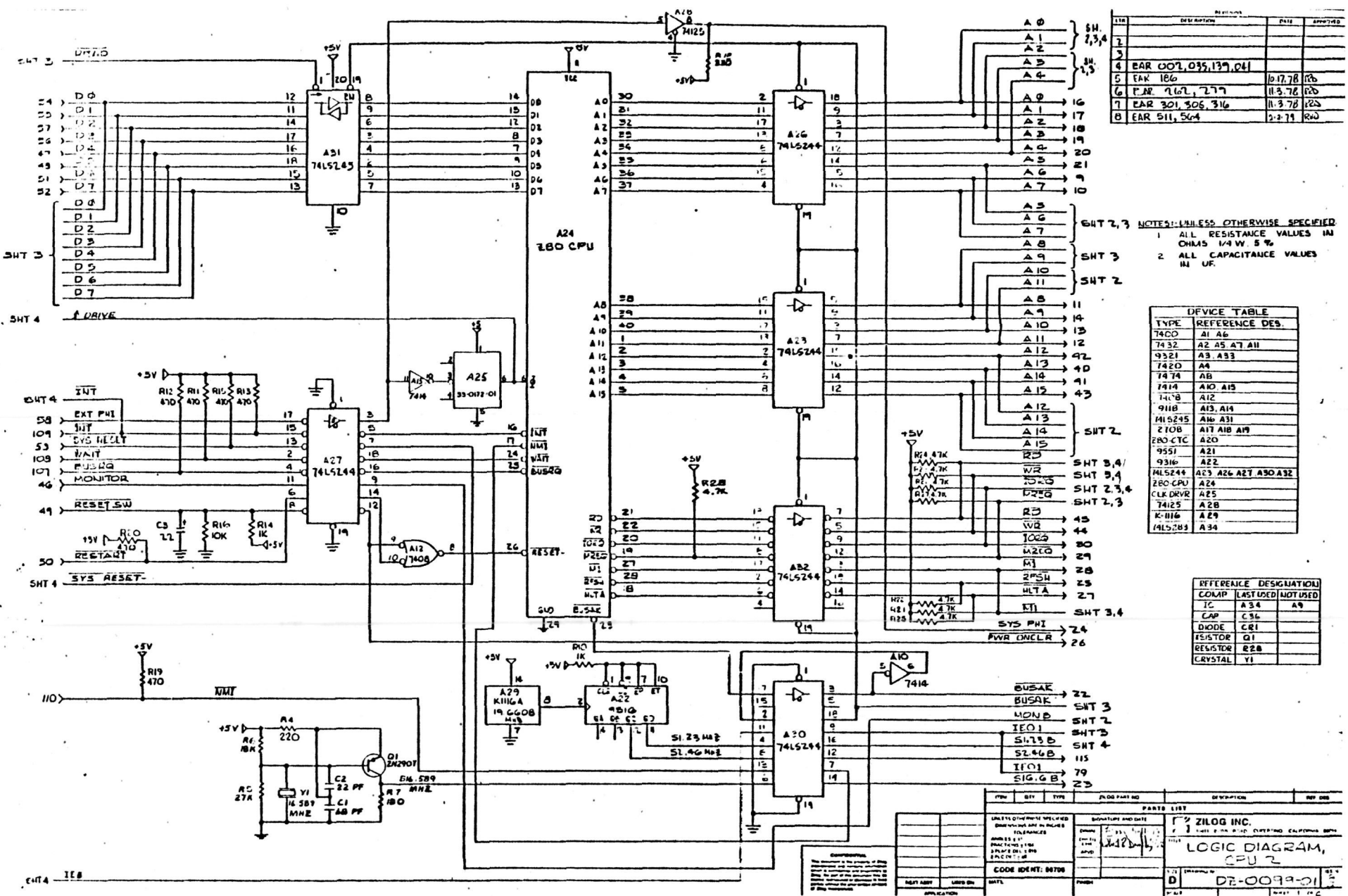
SHT 2

ALL DEVICES ARE MRE 15  
SHOWN ON DEVICE NO B0  
FOR 16K x 8 666 MK4017P-4  
FOR 60K x 8 USE MK4116P-4

REV	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES
			PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			ZILOG INC.		
TOLERANCES			THIS DRAWING IS UNLESS OTHERWISE SPECIFIED		
ANGLES 1/2°			DATE 2-2-71		
FRACTIONS 1/32			DRAWN BY J. J. J.		
DECIMALS .0005			CHECKED BY J. J. J.		
NEUTRAL			DATE 2-2-71		
APPROVED BY			TITLE		
205-M0			LOGIC DIAGRAM,		
CP-0101-01			MEMORY 25		
NEXT ASSY USED ON			REV		
SHT 1			D		
APPLICATION			PART 3 OF 3		

LOGIC DIAGRAMS, CPU

(09-0099-01)



REV	DESCRIPTION	DATE	APPROVED
1			
2			
3			
4	BAR 007, 035, 139, 041		
5	EAK 186	10.17.78	RB
6	P.A.R 767, 777	11.3.78	RB
7	E.A.R 301, 306, 316	11.3.78	RB
8	E.A.R 511, 564	2.2.79	RB

NOTES: UNLESS OTHERWISE SPECIFIED  
 1 ALL RESISTANCE VALUES IN OHMS 1/4 W 5 %  
 2 ALL CAPACITANCE VALUES IN UF.

DEVICE TABLE	
TYPE	REFERENCE DES.
7400	A1 A6
7432	A2 A5 A7 A11
9321	A3 A33
7420	A4
7474	AB
7414	A10 A15
7408	A12
9118	A13 A14
M5245	A16 A31
Z108	A17 A18 A19
Z80 CTC	A20
9551	A21
9316	A22
M5244	A23 A26 A27 A30 A32
Z80 CPU	A24
CLK DRIVER	A25
74125	A28
K-1116	A29
74LS283	A34

REFERENCE DESIGNATION		
COMP	LAST USED	NOT USED
IC	A 34	A 9
CAP	C 36	
DIODE	C 81	
RESISTOR	Q 1	
RESISTOR	R 28	
CRYSTAL	Y 1	

REV	DATE	TYPE	FILE NO	DESCRIPTION	REV DES

UNLESS OTHERWISE SPECIFIED  
 DIMENSIONS ARE IN INCHES  
 TOLERANCES  
 FRACTIONS 1/16  
 DECIMALS 0.05  
 HOLE POSITION 0.10  
 HOLE DIA 0.015

CODE IDENT: 00700

DATE: 11.3.78

DESIGNED BY: RB

CHECKED BY: RB

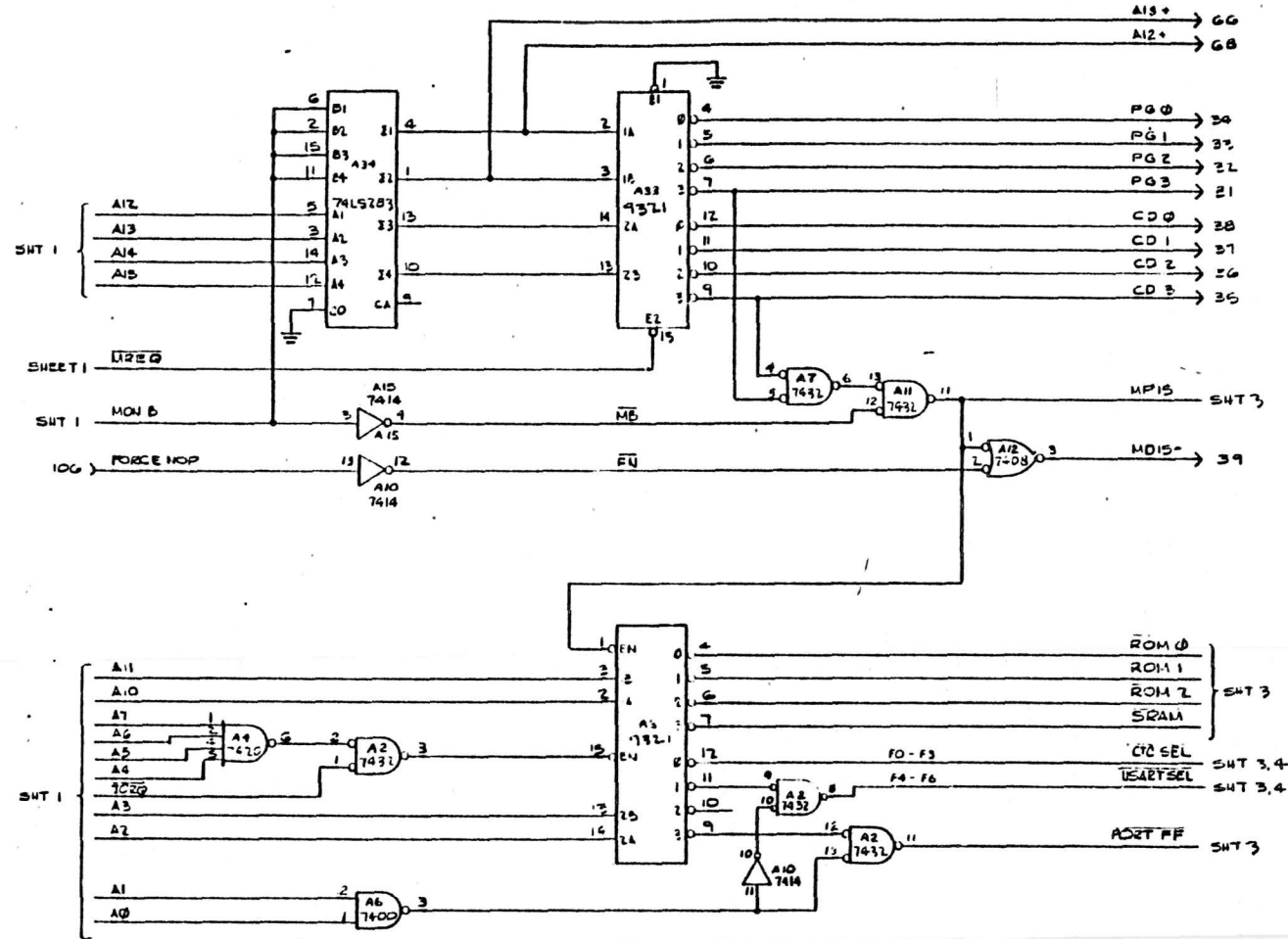
APPROVED BY: RB

LOGIC DIAGRAM, CPU 2

REV: 8

DATE: 11.3.78

REV	DESCRIPTION	DATE	APPROVED
7	SEE SHT. 1	11-8-78	RB



REV	QTY	TYPE	PCB PART NO.	QTY PER PCB	REV

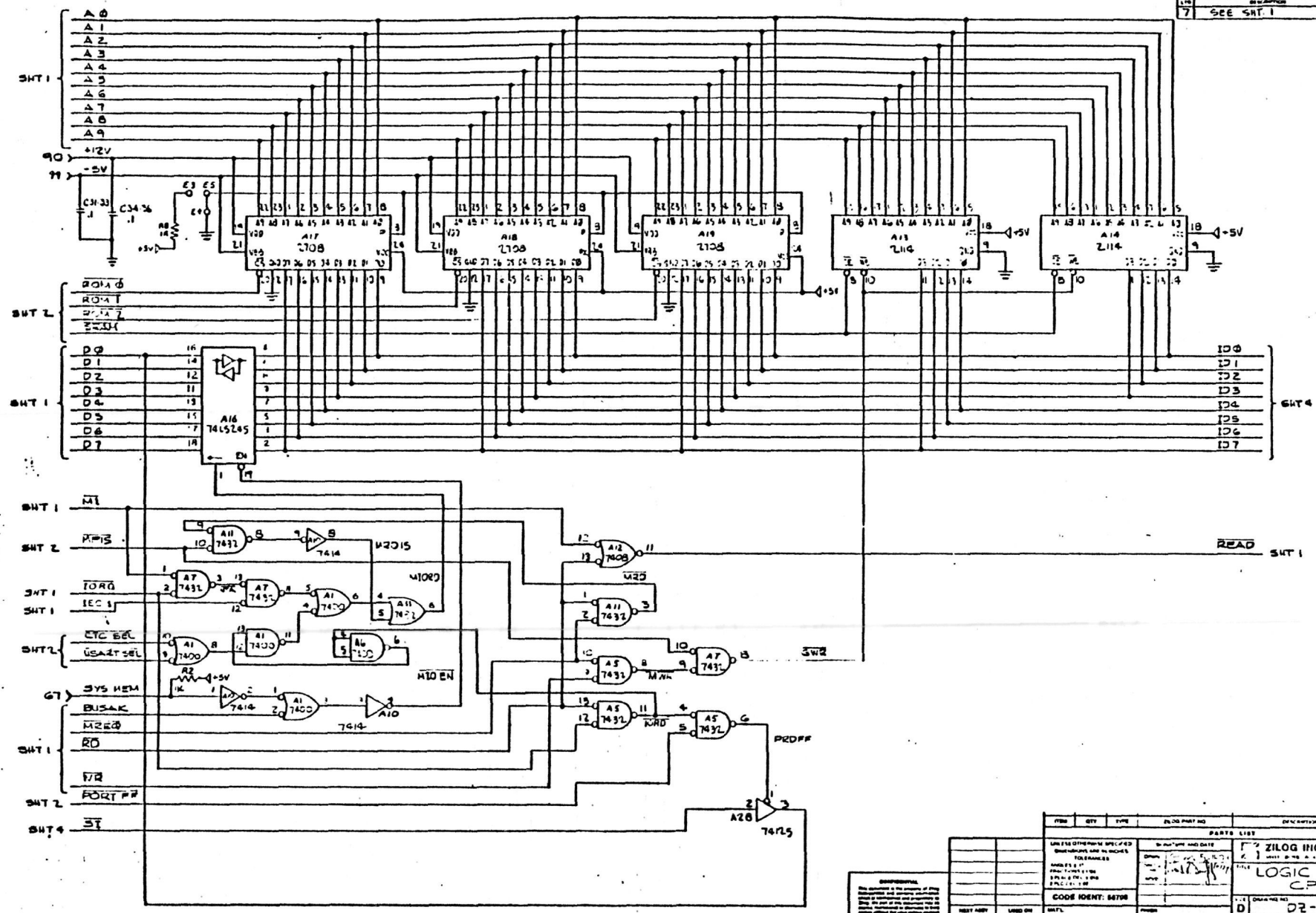
  

DATE	BY	DESCRIPTION

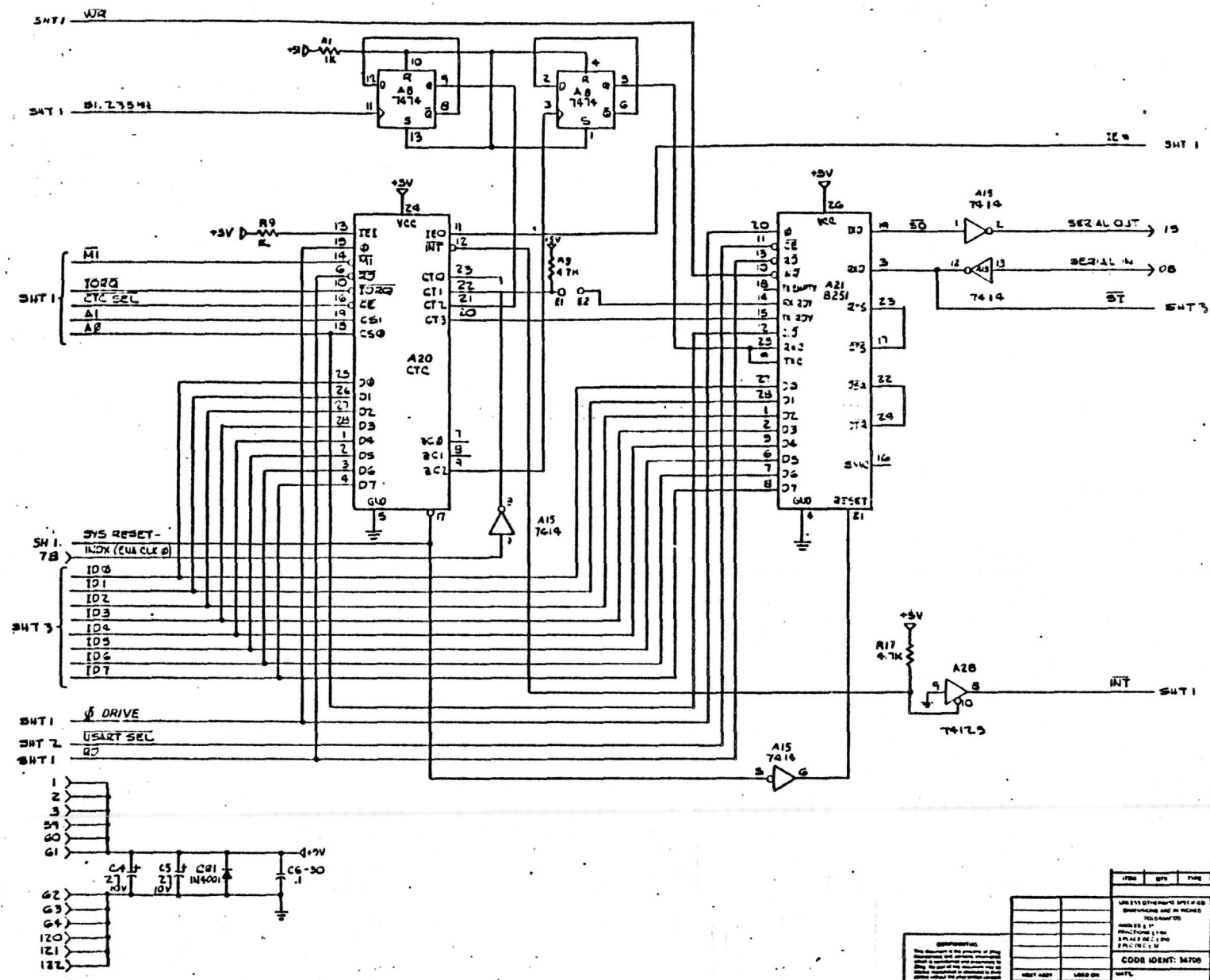
<p><b>CONFIDENTIAL</b></p> <p>This document is the property of Zilog Inc. It contains information that is confidential and may be subject to patent or other legal protection. It is not to be distributed outside of Zilog Inc. without the express written consent of Zilog Inc.</p>	<p>DATE: 11-8-78</p> <p>BY: RB</p> <p>DESCRIPTION: LOGIC DIAGRAM, CPU 2</p> <p>CODE IDENT: 00706</p>	<p>ZILOG INC.</p> <p>1011 N. 17TH ST. SUITE 200, CULVER CITY, CALIFORNIA 90230</p> <p>LOGIC DIAGRAM, CPU 2</p> <p>REV: D</p> <p>DATE: 02-0099-01</p> <p>SHEET: 2 OF 4</p>
--	--	---

REV	DESCRIPTION	DATE	APPROVED
7	See SHT 1	11.3.78:ab	



ITEM	QTY	TYPE	ZILOG PART NO.	DATE	REV
PARTS LIST					
ZILOG INC.					
LOGIC DIAGRAM, CPU 2					
CODE IDENT: 84798					
D 02-C091-01 8					

REV	DESCRIPTION	DATE	APPROVED
7	SEE SHT 1	11/2/80	

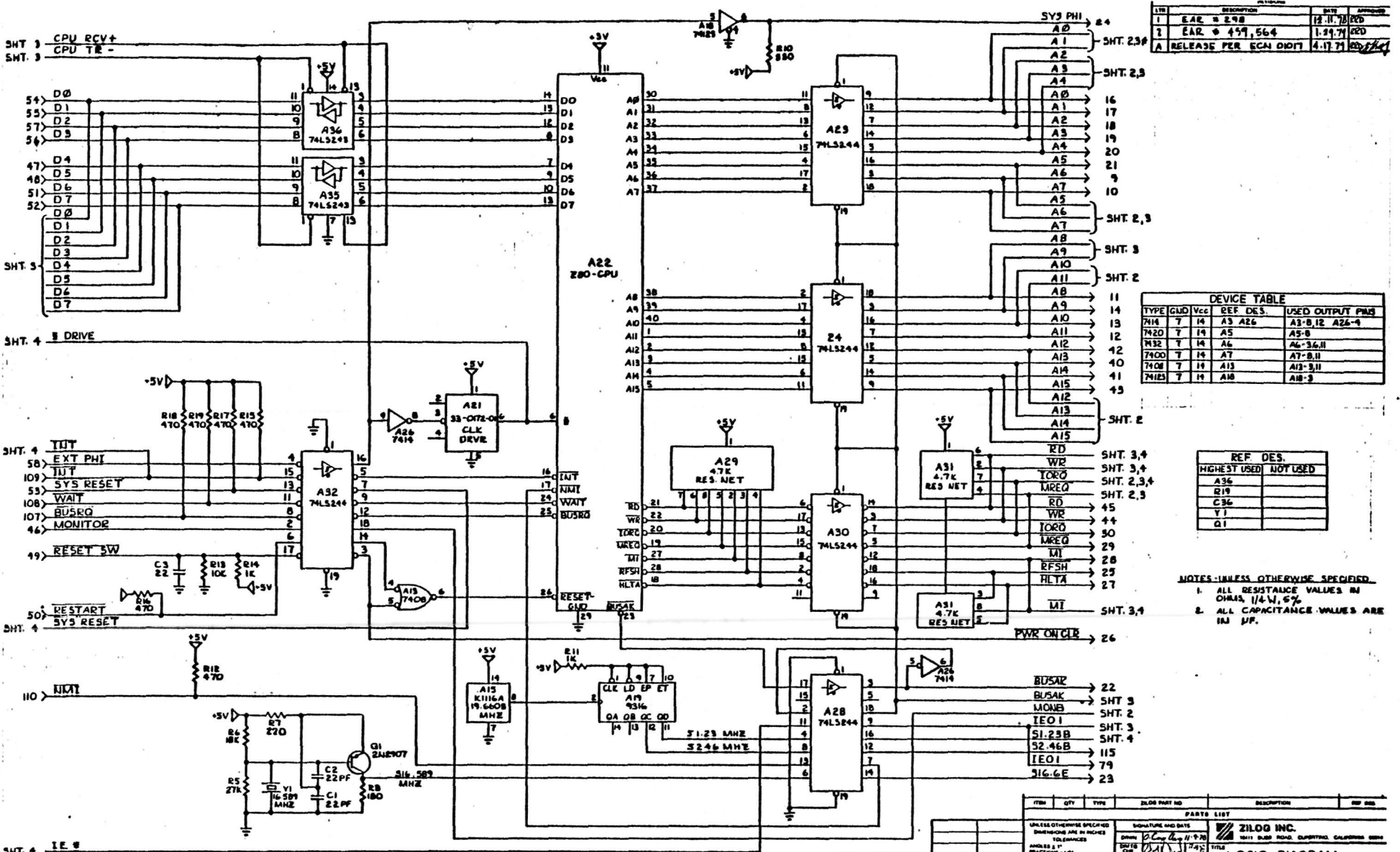


ITEM	QTY	TYPE	QLOS PART NO	DESCRIPTION	AMP DESG
PARTS LIST					
UNLESS OTHERWISE SPECIFIED			SIGNATURE AND DATE		
DIMENSIONS ARE AS SHOWN			DATE: 11/2/80		
MATERIALS ARE TO BE USED			DRAWN BY: [Signature]		
FINISHES ARE TO BE USED			CHECKED BY: [Signature]		
TOLERANCES ARE TO BE USED			DATE: 11/2/80		
UNLESS OTHERWISE SPECIFIED			DATE: 11/2/80		
CODE IDENT: M706			TITLE: LOGIC DIAGRAM, CPU 2		
REV	APPY	LDG ON	DATE	POWER	SCALE
APPLICATION				D	02-0099-01 8
				SCALE	SHEET 6 OF 6



LOGIC DIAGRAMS, CPU-3

(09-0099-03)



ITEM	DESCRIPTION	DATE	APPROVED
1	EAR # 248	12.11.70	ROD
2	EAR # 459, 564	1.29.71	ROD
A	RELEASE PER ECN 01071	4.17.71	ROD

TYPE	QTY	V <sub>CC</sub>	REF. DES.	USED OUTPUT PINS
7414	7	14	A3, A26	A3-B, 12, A26-4
7420	7	14	A5	A5-B
7432	7	14	A6	A6-3&11
7400	7	14	A7	A7-B, 11
7408	7	14	A13	A13-3, 11
7415	7	14	A10	A10-3

HIGHEST USED	NOT USED
A36	
R19	
C36	
Y1	
Q1	

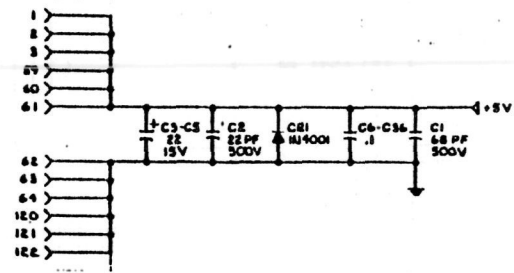
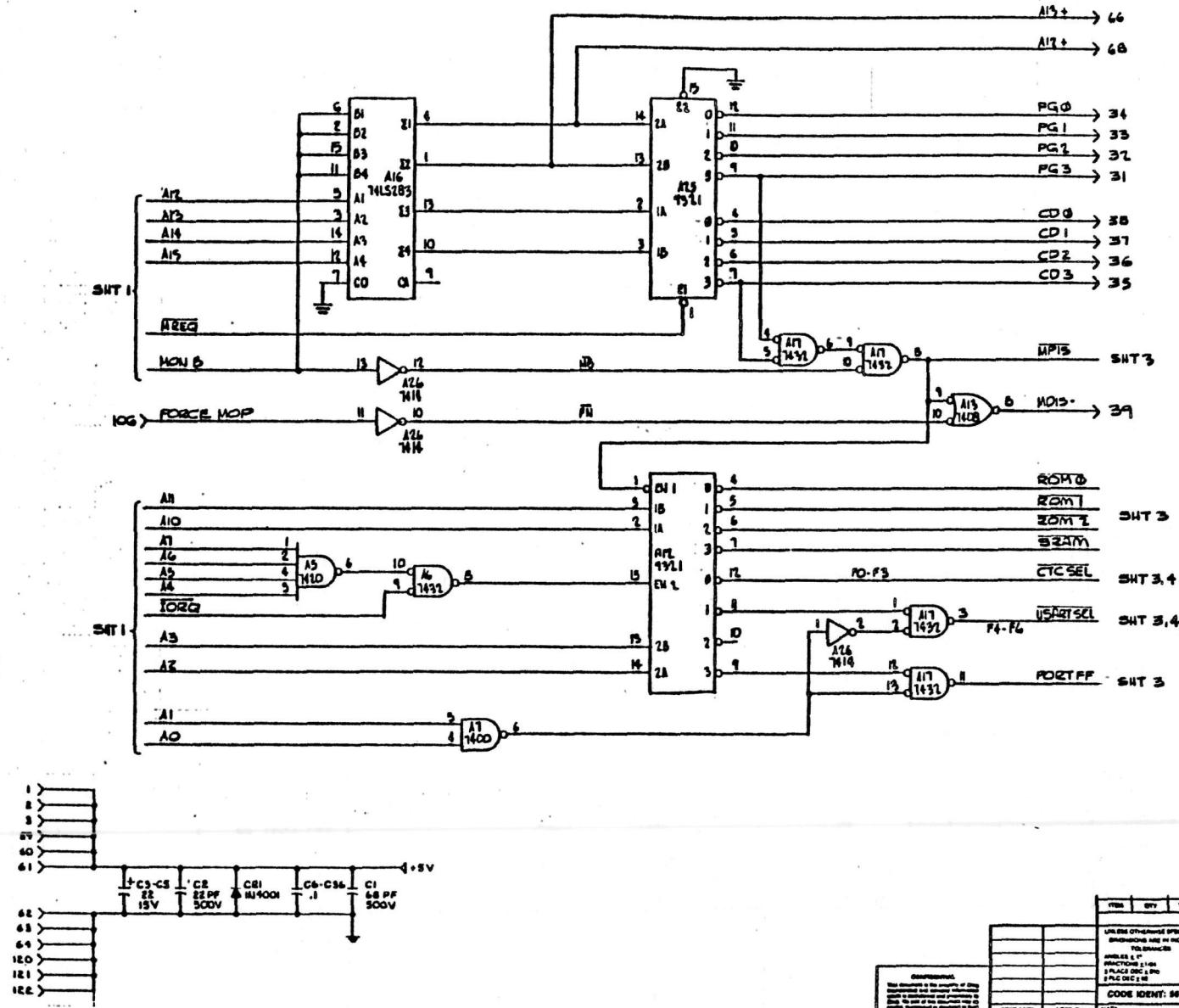
NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. ALL RESISTANCE VALUES IN OHMS, 1/4 W, 5%  
 2. ALL CAPACITANCE VALUES ARE IN μF.

ITEM	QTY	TYPE	SILOC PART NO.	DESCRIPTION	REF. DES.
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE IN INCHES					
DIMENSIONS ARE IN INCHES TOLERANCES					
ANGLES ± 1°					
FRACTIONS 1/16"					
3 PLACE DECIMALS					
5 PLACE DECIMALS					
E PLACES DECIMALS					
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES TOLERANCES					
ANGLES ± 1°					
FRACTIONS 1/16"					
3 PLACE DECIMALS					
5 PLACE DECIMALS					
E PLACES DECIMALS					
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES TOLERANCES					
ANGLES ± 1°					
FRACTIONS 1/16"					
3 PLACE DECIMALS					
5 PLACE DECIMALS					
E PLACES DECIMALS					

10-0018-3 Ep6-140  
 NIGHT ARMY  
 USED ON

SHT. 4 IE #

REV	DESCRIPTION	DATE	BY
4	SEE SHEET 1	4.17.71	RV

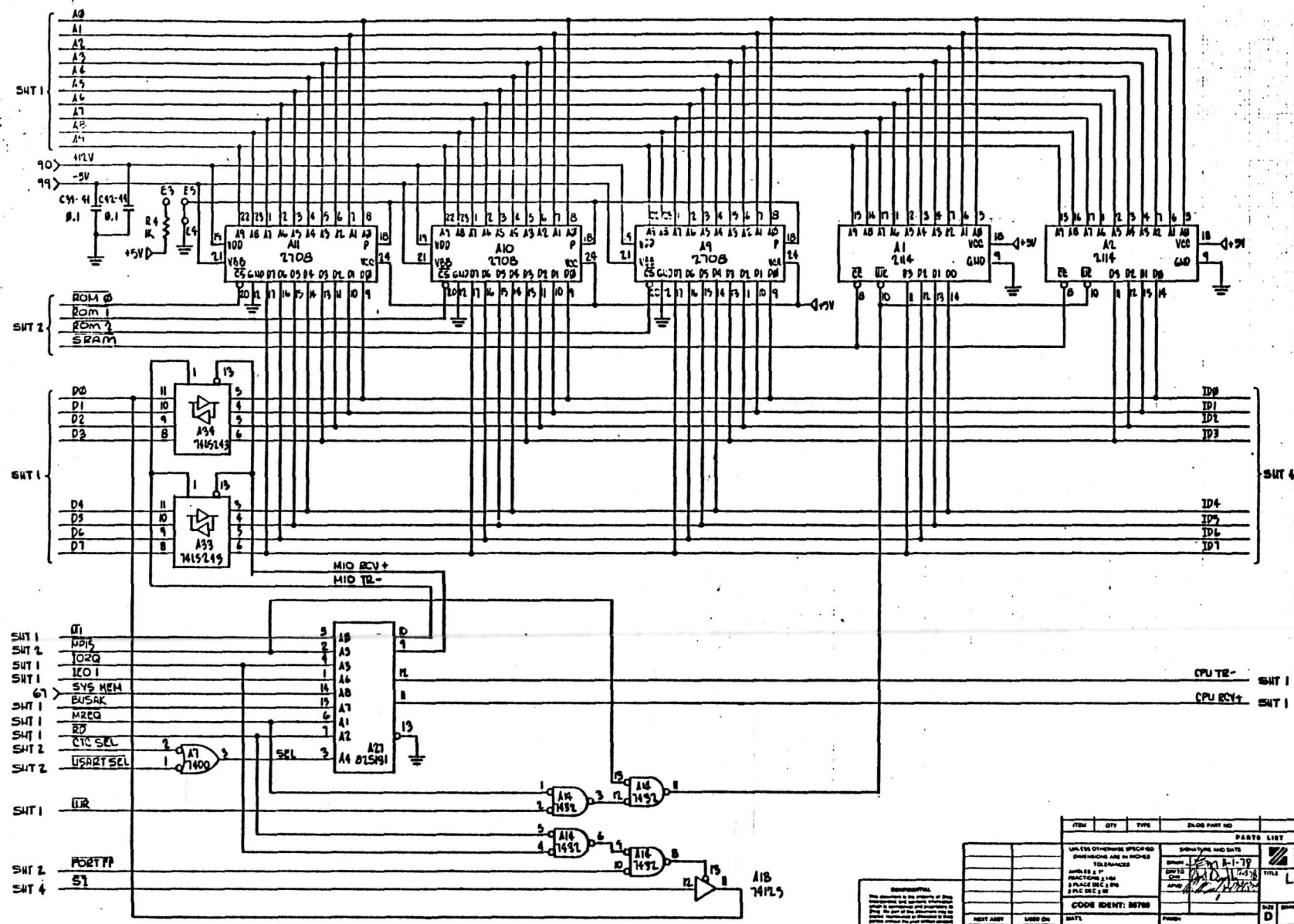


CONVENTIONS:  
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ITEM	QTY	TYPE	SOLE PART NO.	DESCRIPTION	REV. DES.
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			SCHEDULE AND DATE		
TOLERANCES			DATE: 11.1.71		
ANGLES & R			DATE: 11.1.71		
FRACTIONS 1/64			DATE: 11.1.71		
PLACES DEC 2 1/2			DATE: 11.1.71		
PLACES DEC 2 1/8			DATE: 11.1.71		
CODE IDENT: 8778			DATE: 11.1.71		
REV. DES.	DATE	BY	APP'D.	SCALE	SHEET 2 OF 4
D	12-0099-03	A			

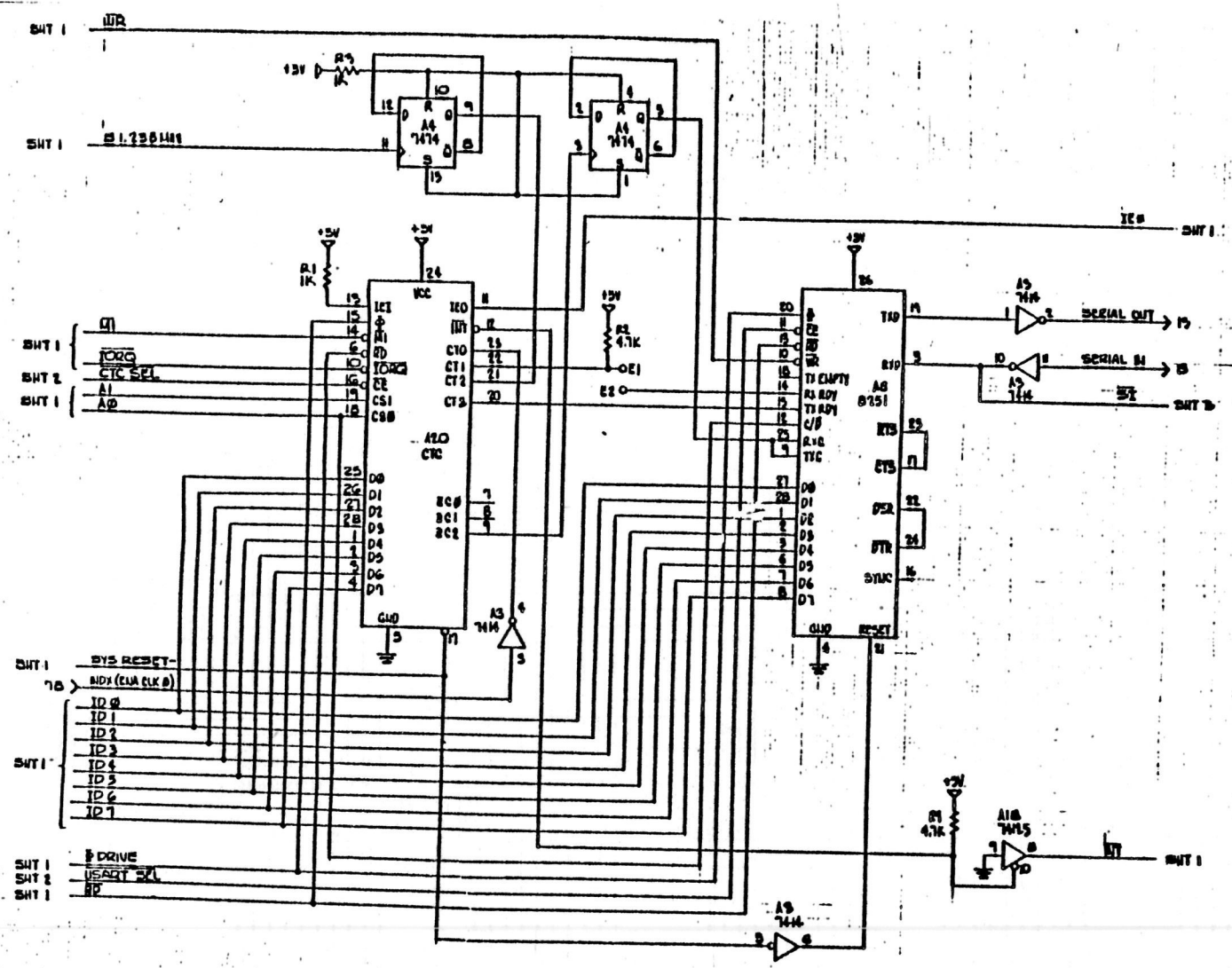
ZILOG INC.  
 1801 BLUE ROAD CUPERTINO CALIFORNIA 95014  
 LOGIC DIAGRAM,  
 CPU 3

REV	DESCRIPTION	DATE	APPROVED
A	SCS S-VCT 1	4.11.74	[Signature]



DISCLAIMER:  
The accuracy of the information of this drawing is the responsibility of the user. It is not to be used for any other purpose than that for which it was intended. No liability is assumed by the user for any damage or loss resulting from the use of this drawing.

ITEM	QTY	TYPE	ZILOG PART NO.	PARTS LIST	DESCRIPTION	REV. NO.
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES FINISHES PLACEMENT PLACEMENT PLACEMENT						
DRAWN BY: [Signature]			DATE: 1-1-79		TITLE: ZILOG INC. 1981 BLDG. SCHE. QUINCY, CALIFORNIA, USA	
CHECKED BY: [Signature]			DATE: 1-1-79		TITLE: LOGIC DIAGRAM, CPU 3	
CODE IDENT: 88788			PART NO: D2-0099-03		SCALE: 1/8"	
NEXT ASSY: [Blank]			LEADS ON: [Blank]		PART 3 OF 4	
APPLICATION: [Blank]			DATE: [Blank]		[Blank]	



REV	QTY	TYPE	3200 PART NO.	DESCRIPTION	REV

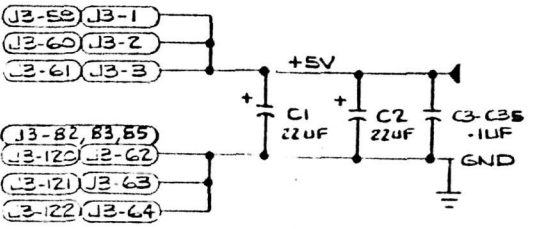
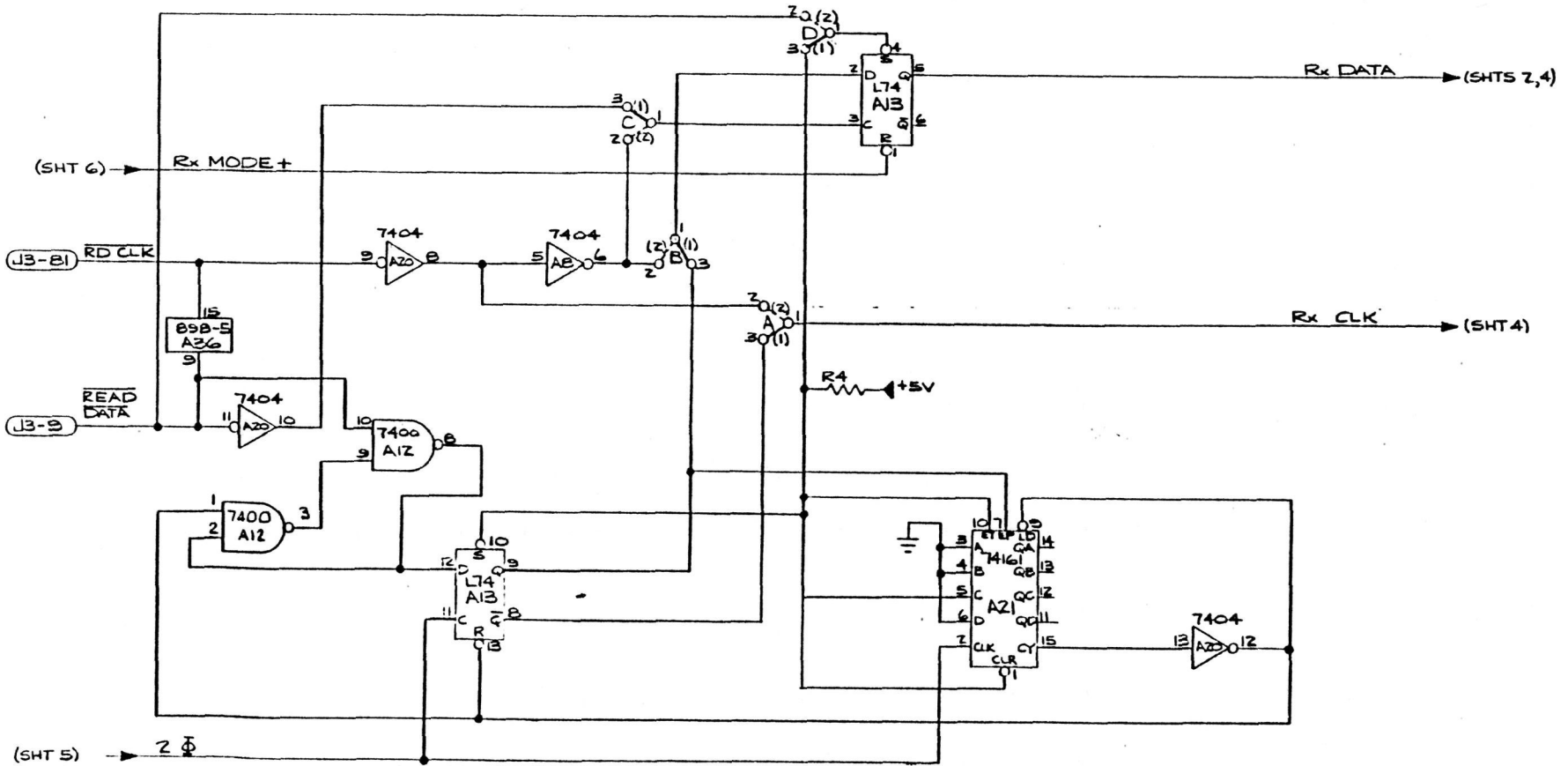
PARTS LIST		DESCRIPTION	REV
7414	2	HEX INVERTER	
7415	1	NAND GATE	
7451	1	DECODER	

ZILOG INC. 3001 S.W. 10TH AVENUE, GAITHERSBURG, MD 20878		DATE: 11-1-74 DRAWN: [Signature] CHECKED: [Signature]
LOGIC DIAGRAM, CPU 3		PART NO: 72-0099-03 REV: A

LOGIC DIAGRAMS, FLOPPY CONTROLLER

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	ECN 00202	1-26-8	A
D	ECN 00670	11-8-78	AL

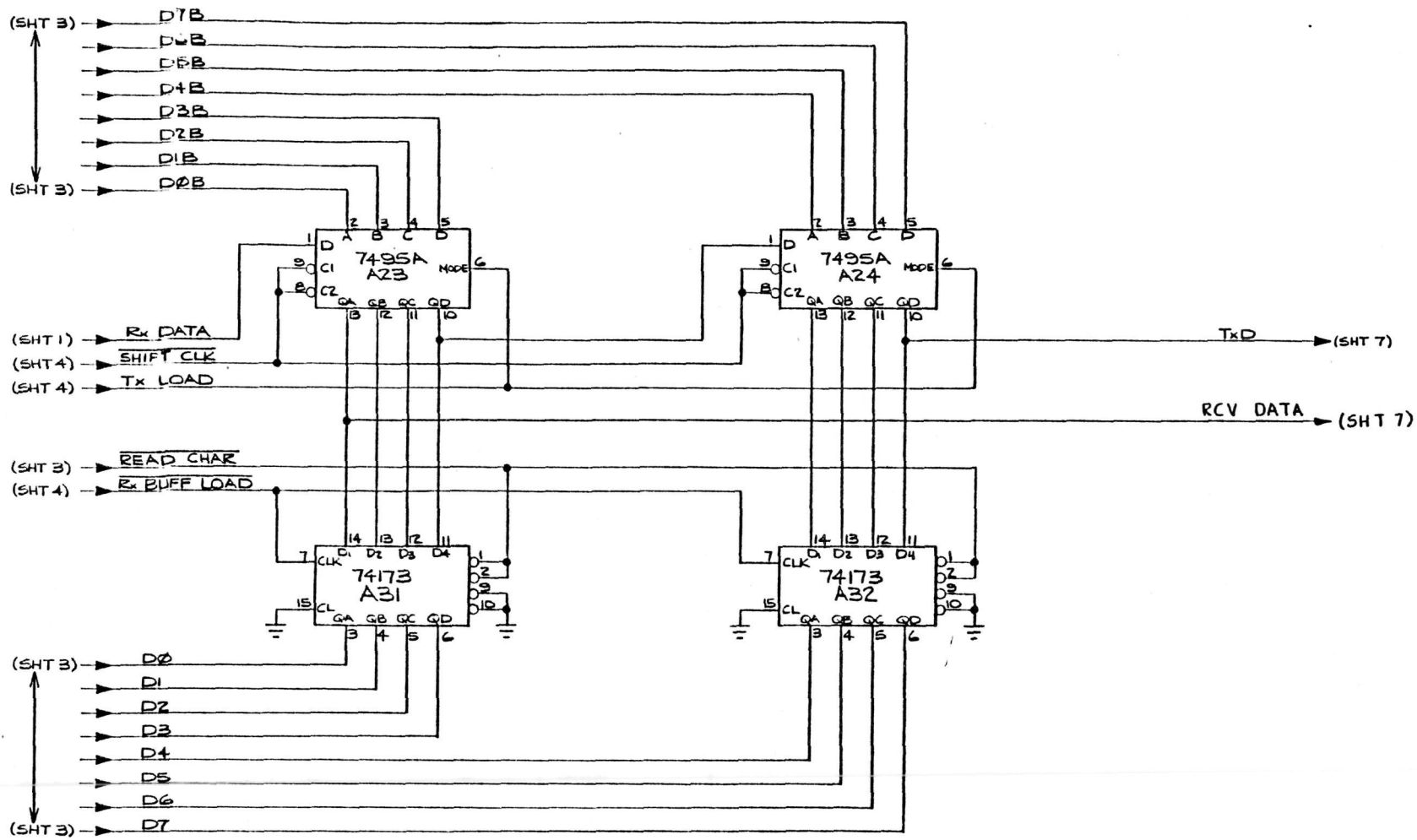


J-3

FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES			
±	°	±	°		
APPROVALS	DATE	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. The part of this document may be copied, reproduced or disclosed in any form without the prior written consent of Zilog Incorporated.			
DRAWN	1-18-76	SCALE	SIZE	DRAWING NO.	
CHECKED		NONE	C	DE-0004-01	
DO NOT SCALE DRAWING					SHEET 1 OF 7

REVISIONS		
LTR	DESCRIPTION	DATE
D		1-26-76

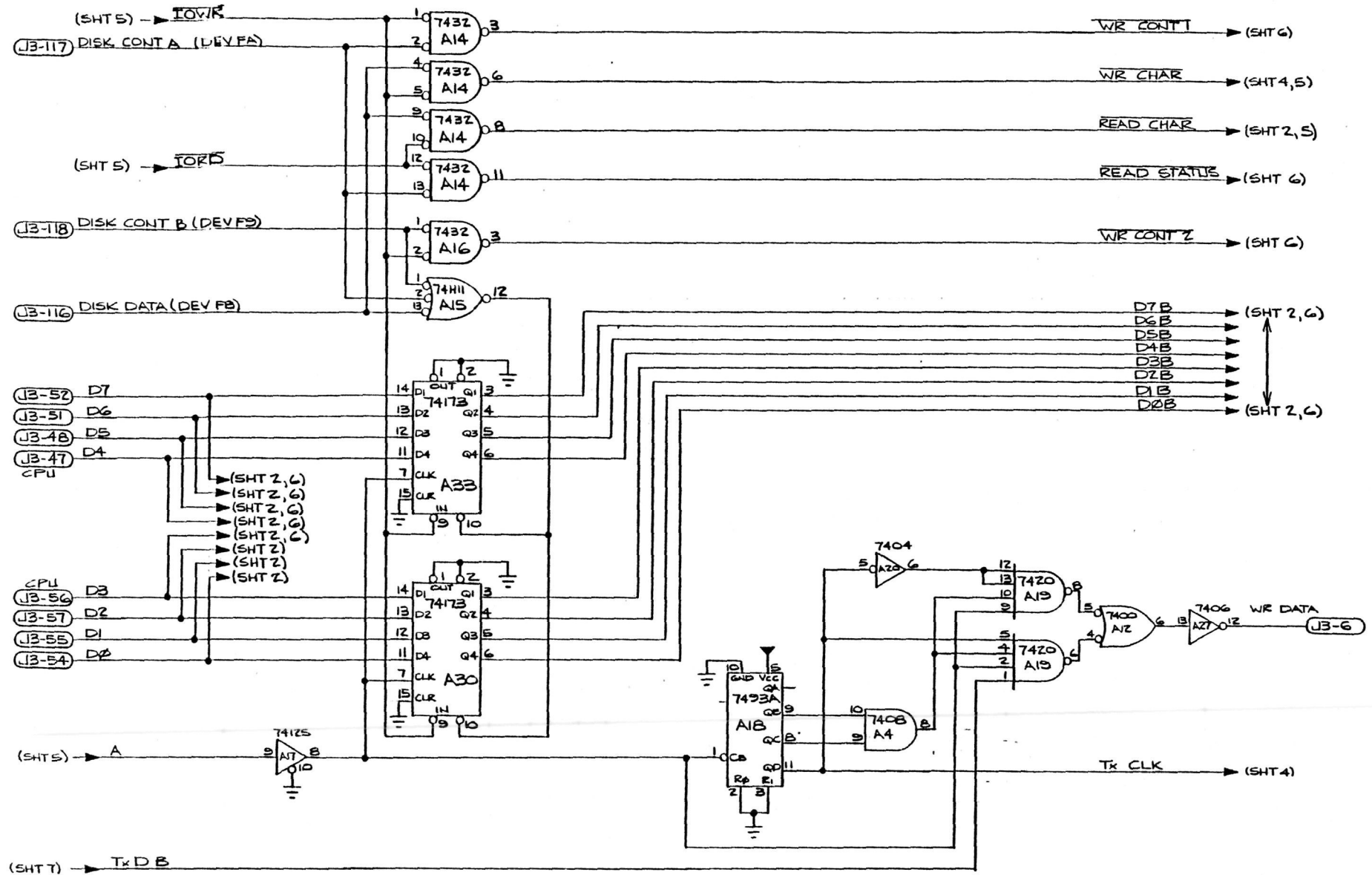


FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±			
CONFIDENTIAL			
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APPROVALS	DATE	SCALE	SIZE
DRW M.J.L.	4-13-76	NONE	C
CHECKED		DRAWING NO. DZ-0004-01	
DO NOT SCALE DRAWING			HEET 2 OF 7



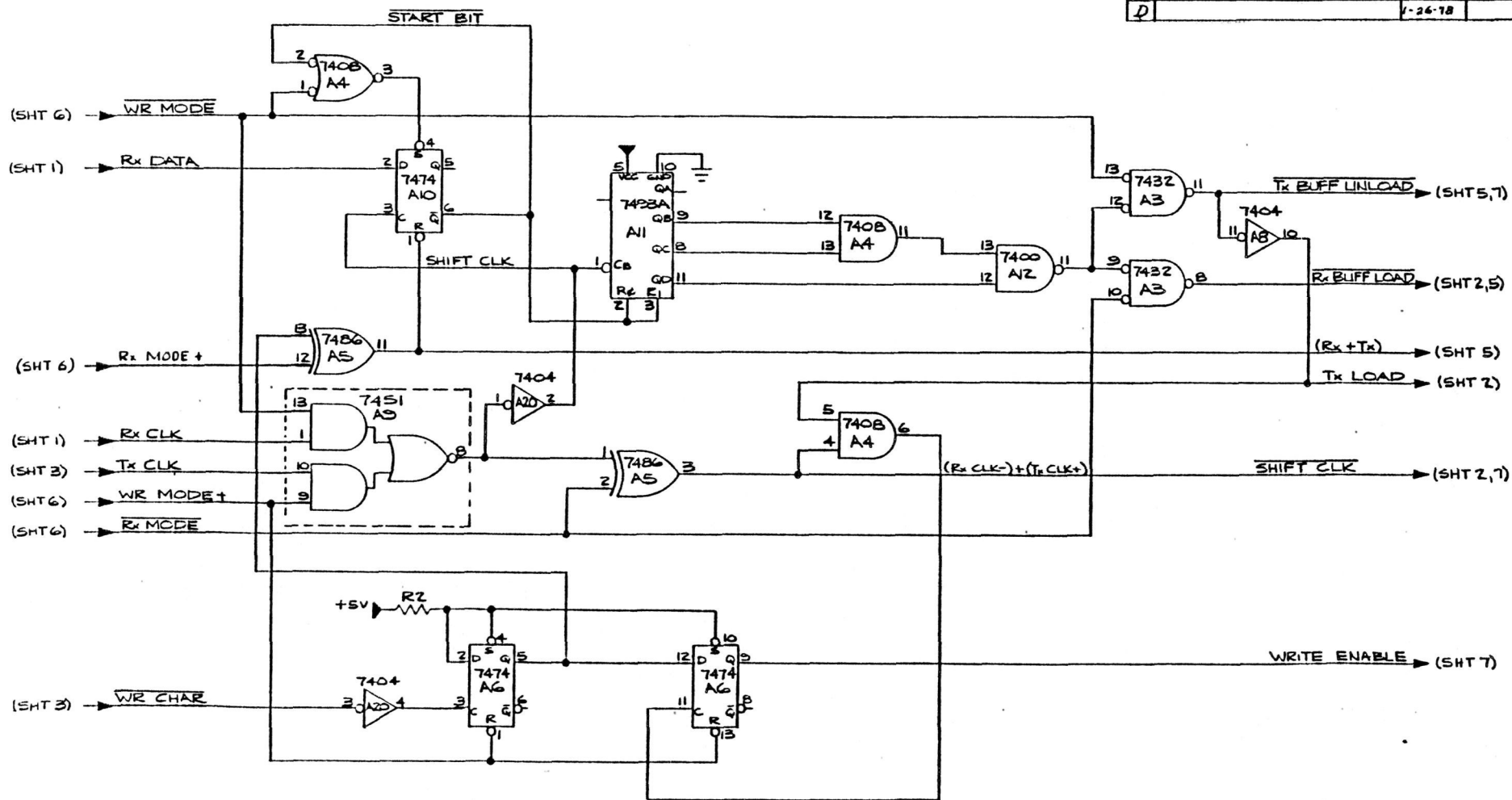
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES				<b>CONFIDENTIAL</b> This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated.	
APPROVALS	DATE				
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CHECKED		NONE	C	DO NOT SCALE DRAWING	
				SHEET 3 OF 7	

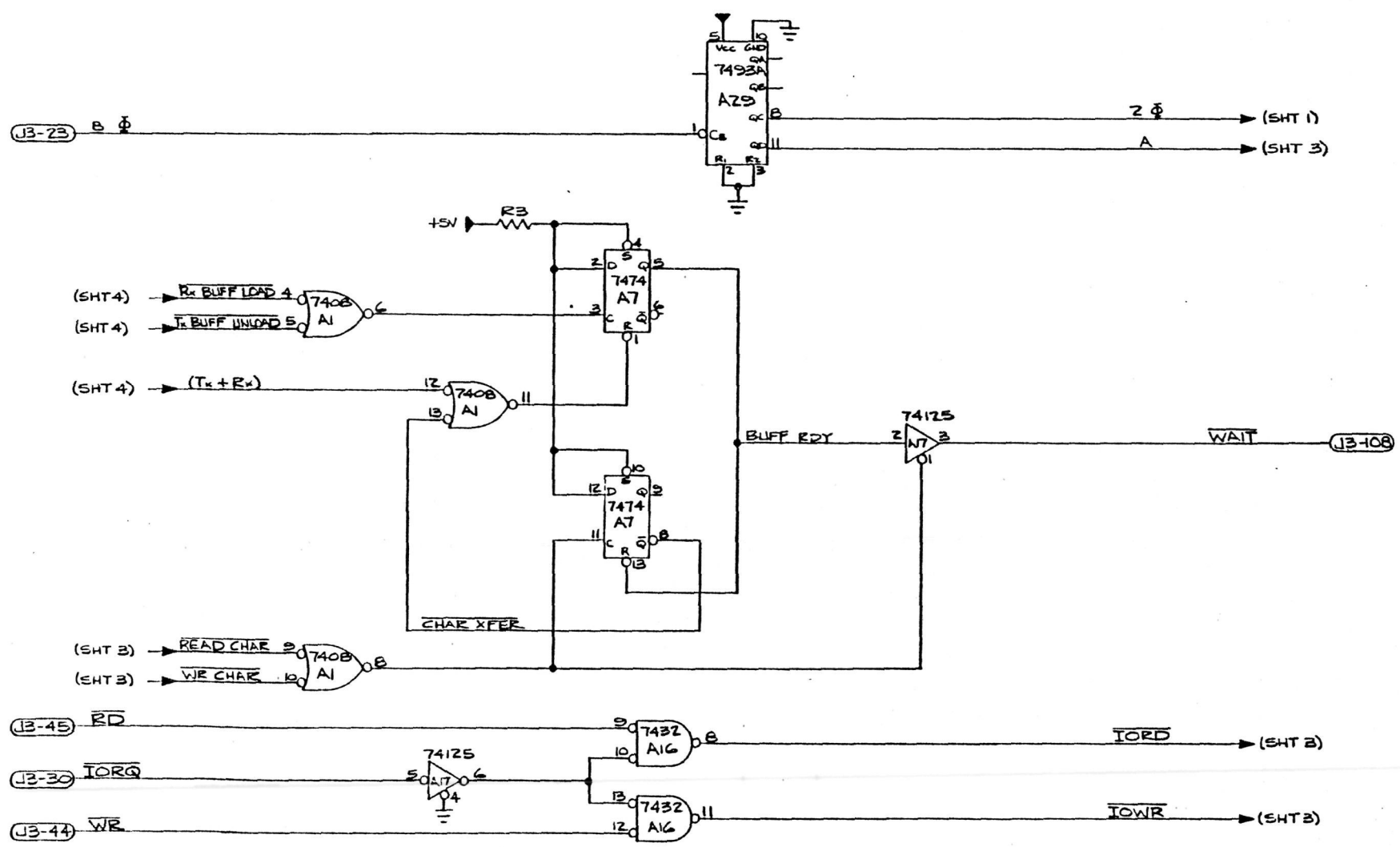
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



### FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC		
±	±	±	CONFIDENTIAL
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APPROVALS	DATE	SCALE	SIZE
DESIGN	4-5-78	NONE	C
CHECKED			DRAWING NO. DZ-000+01
DO NOT SCALE DRAWING			SHEET 4 OF 7

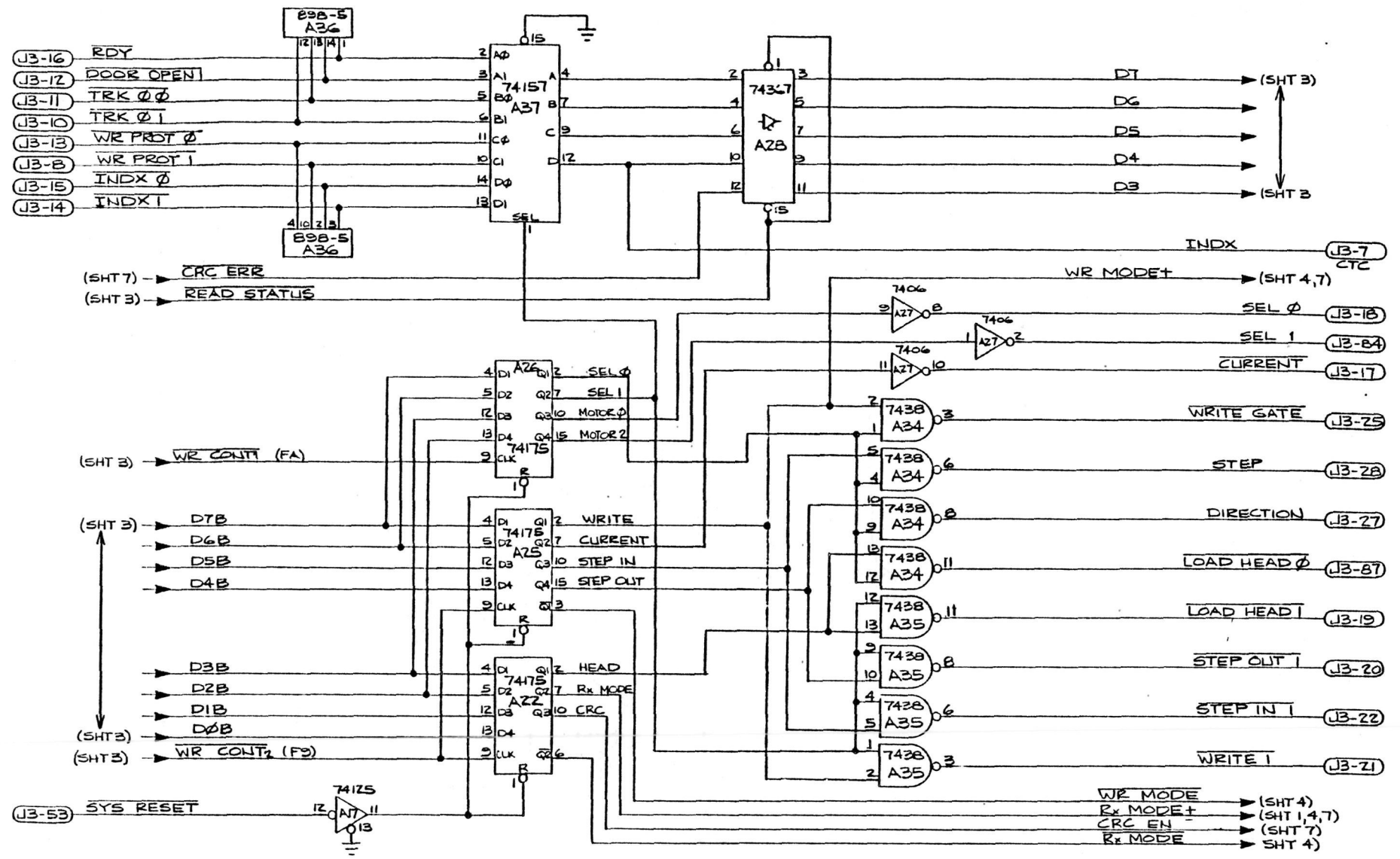
REVISIONS		
LTR	DESCRIPTION	DATE
D		1-26-78



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		Z Z Z			
CONFIDENTIAL		<small>This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. In part of this document may be copied, reproduced or disclosed in third parties and all the prior written consent of Zilog Incorporated.</small>			
APPROVALS	DATE	SCALE	SIZE	DRAWING NO.	
DRW: R. J. LILL	4-15-78	1/4" = 1"	C	DZ-0004-01	
CHECKED				SHEET 5 OF 7	
				D) NOT SCALE DRAWING	

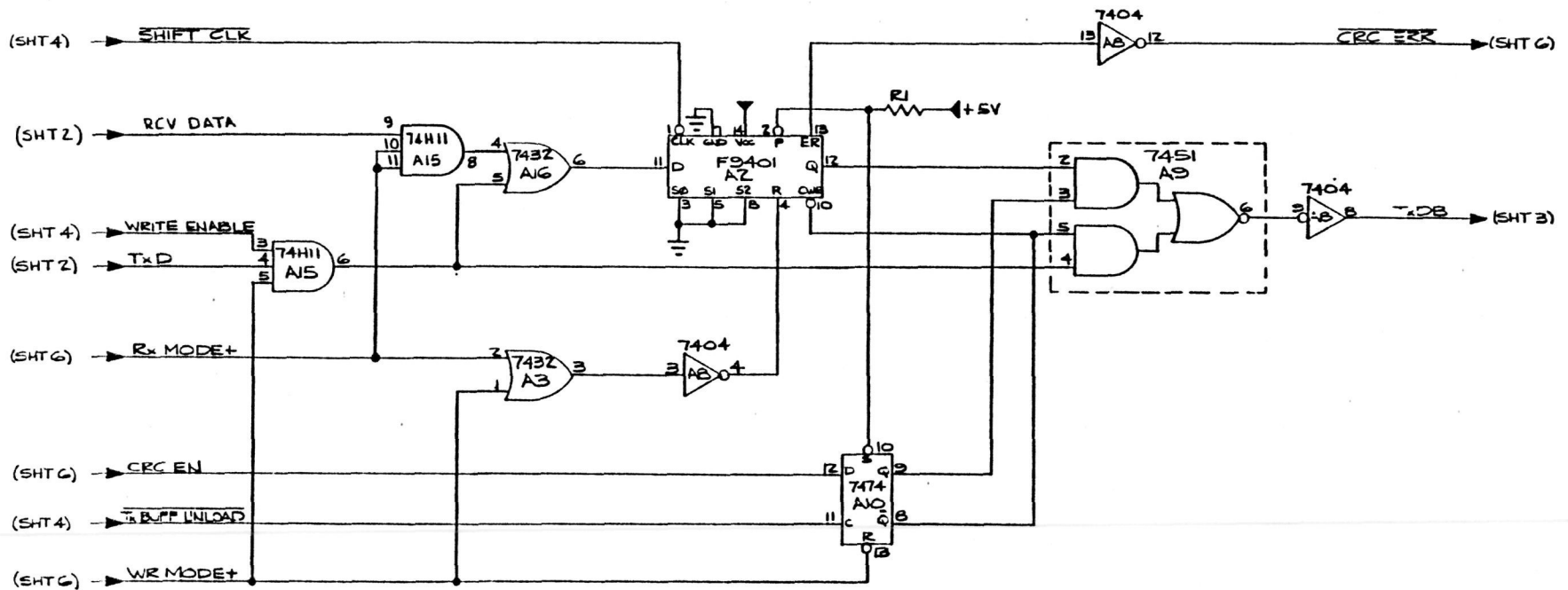
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	



FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±			
APPROVALS		DATE	
DRAWN 11.3.1c		4-15-76	
CHECKED		SCALE	SIZE
		NONE	C
		DRAWING NO. D2-0004-01	
		DO NOT SCALE DRAWING	
		SHEET 6 OF 7	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D		1-26-78	

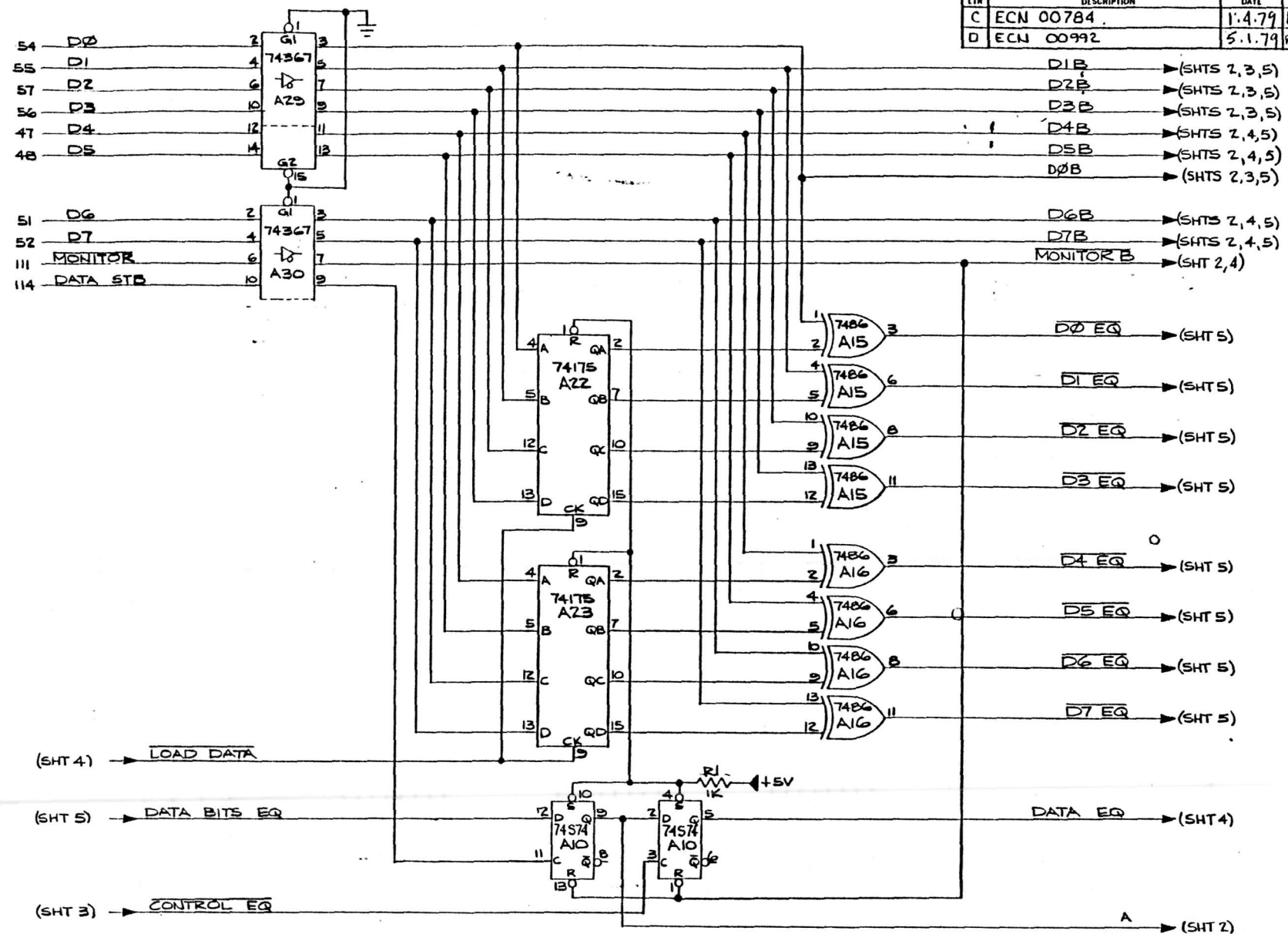


### FLOPPY CONTROLLER

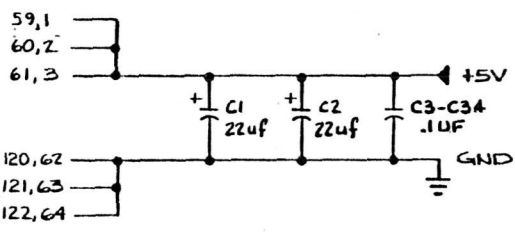
TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS DEC ANGLES			
2 2 2	CONFIDENTIAL		
APPROVALS	DATE	This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. The part of this document may be copied, reproduced or disclosed in any form without the prior written consent of Zilog Incorporated.	
DRAWN T.C.L.L.	4-15-76	SCALE	NONE
CHECKED		SIZE	C
		DRAWING NO.	DE-0004-01
		DO NOT SCALE DRAWING	SHEET 7 OF 7

LOGIC DIAGRAMS, BREAKPOINT

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
C	ECN 00784	1.4.79	RRS
D	ECN 00992	5.1.79	RRS



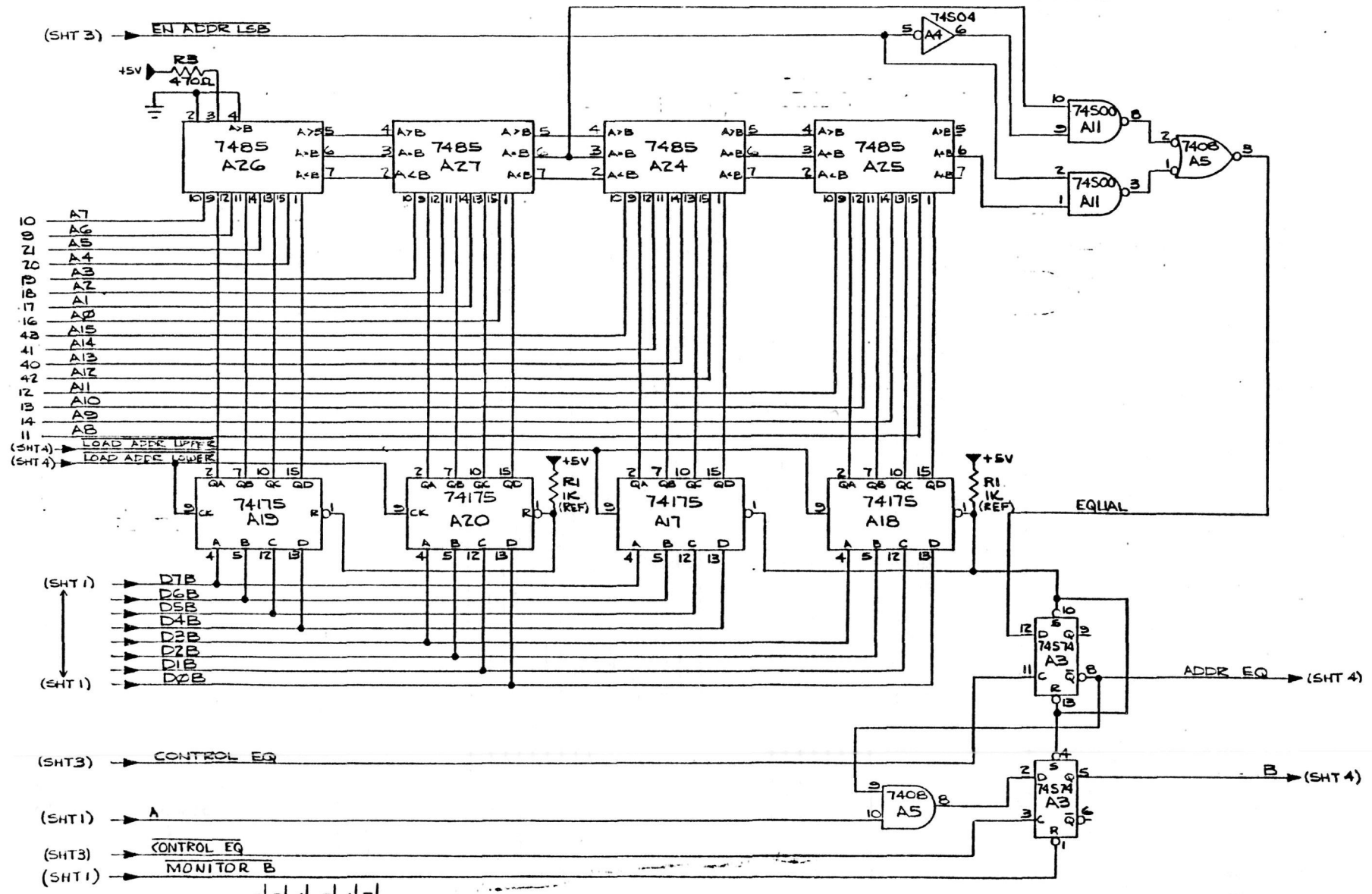
(MONITOR)  
(MONITOR)



BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES	
±	±	±	±
<b>Zilog</b>			
CONFIDENTIAL			
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APPROVALS	DATE	SCALE	SIZE
DRW: M.J.L.	4-12-76	NONE	C
CHECKED			DWING NO
J.C. Hager	4/19/78		DZ-0003-02
JCH	7/2/77	DO NOT SCALE DRAWING	SHEET 1 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5-1-79	RPD

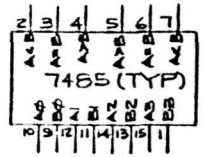


- 10 A7
- 10 AG
- 10 AS
- 21 A4
- 20 A3
- 19 AZ
- 18 AI
- 17 AD
- 16 A15
- 43 A14
- 41 A13
- 42 A12
- 12 A10
- 13 AS
- 14 AB

(SHT 4) LOAD ADDR UPPER  
 (SHT 4) LOAD ADDR LOWER

- (SHT 1) D7B
- (SHT 1) D6B
- (SHT 1) D5B
- (SHT 1) D4B
- (SHT 1) D3B
- (SHT 1) D2B
- (SHT 1) D1B
- (SHT 1) D0B

- (SHT 3) CONTROL EQ
- (SHT 1) A
- (SHT 3) CONTROL EQ
- (SHT 1) MONITOR B

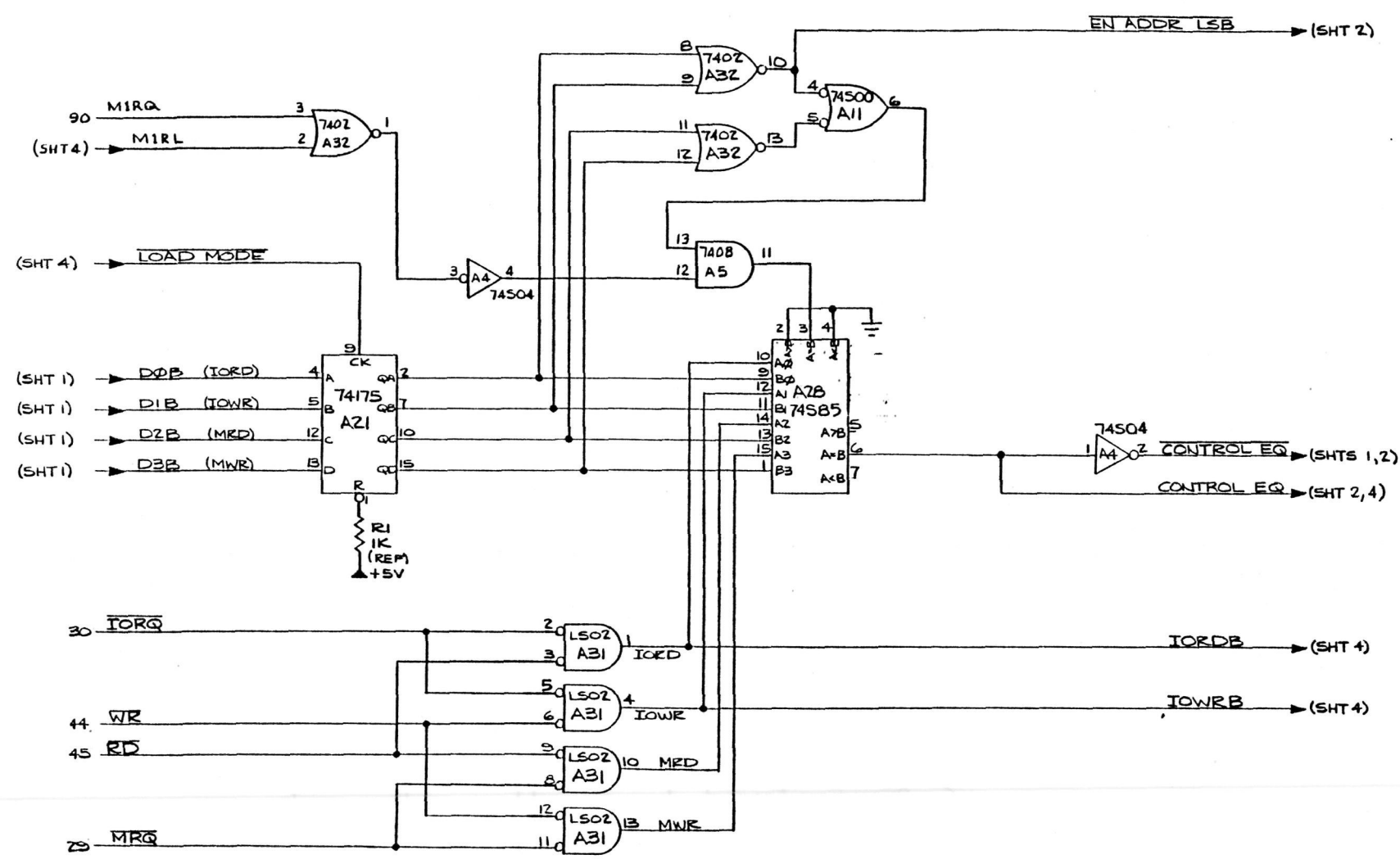


BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		<b>Zilog</b>	
APPROVALS		DATE	
DRAWN	4-12-76		
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DRAWING NO. DZ-0003-C2		DO NOT SCALE DRAWING	
		SHEET 2 OF 5	



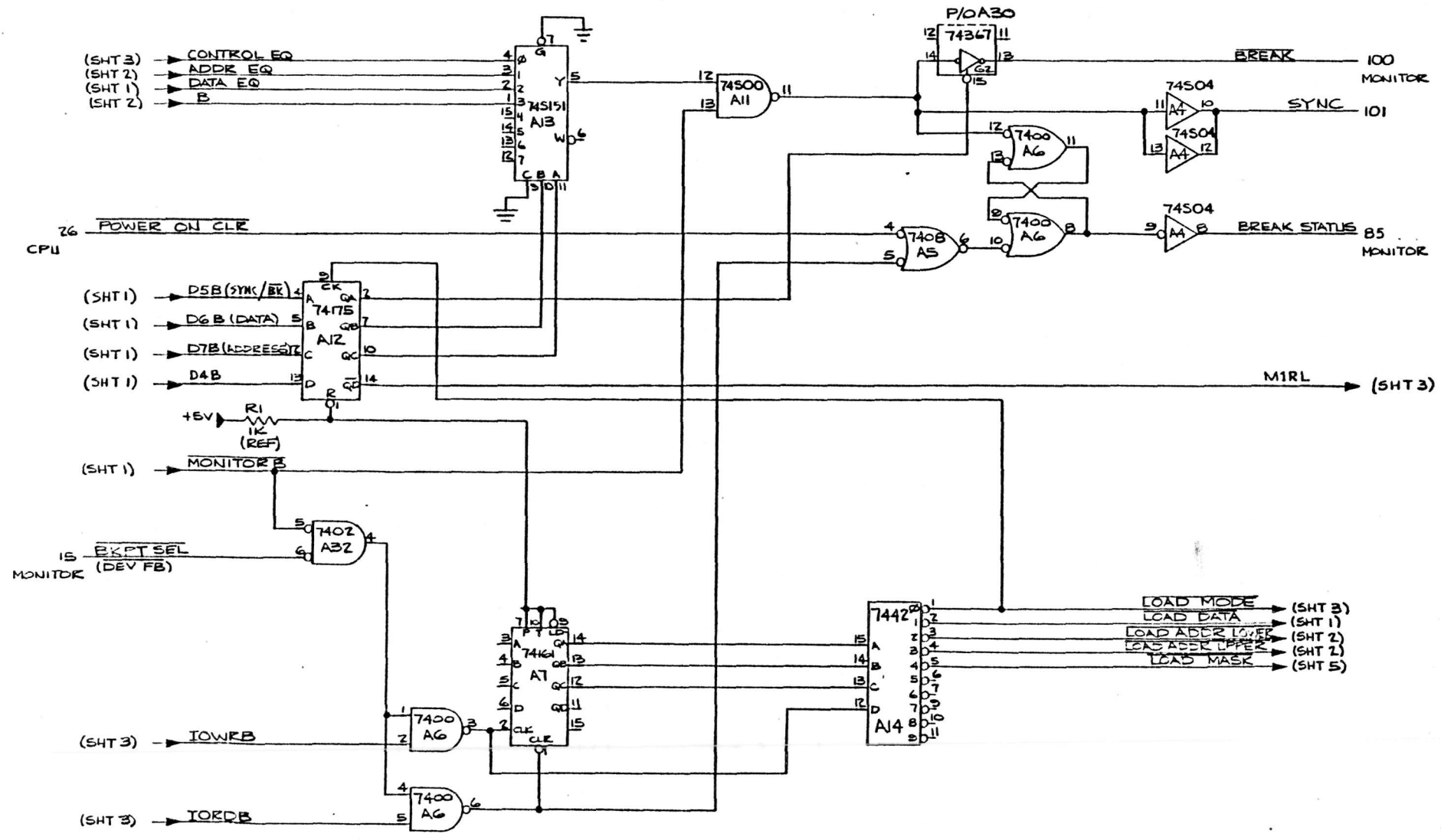
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5.1.79	RRD



BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES			
APPROVALS		DATE		<small>CONFIDENTIAL</small> This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog, Incorporated.	
DRAWN: M. S. L. CHECKED: J. C. H.	DATE: 4-12-76 DATE: 7/19/78	SCALE: NONE	SIZE: C	DRAWING NO. DZ-0003-02	
DO NOT SCALE DRAWING				SHEET 3 OF 5	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
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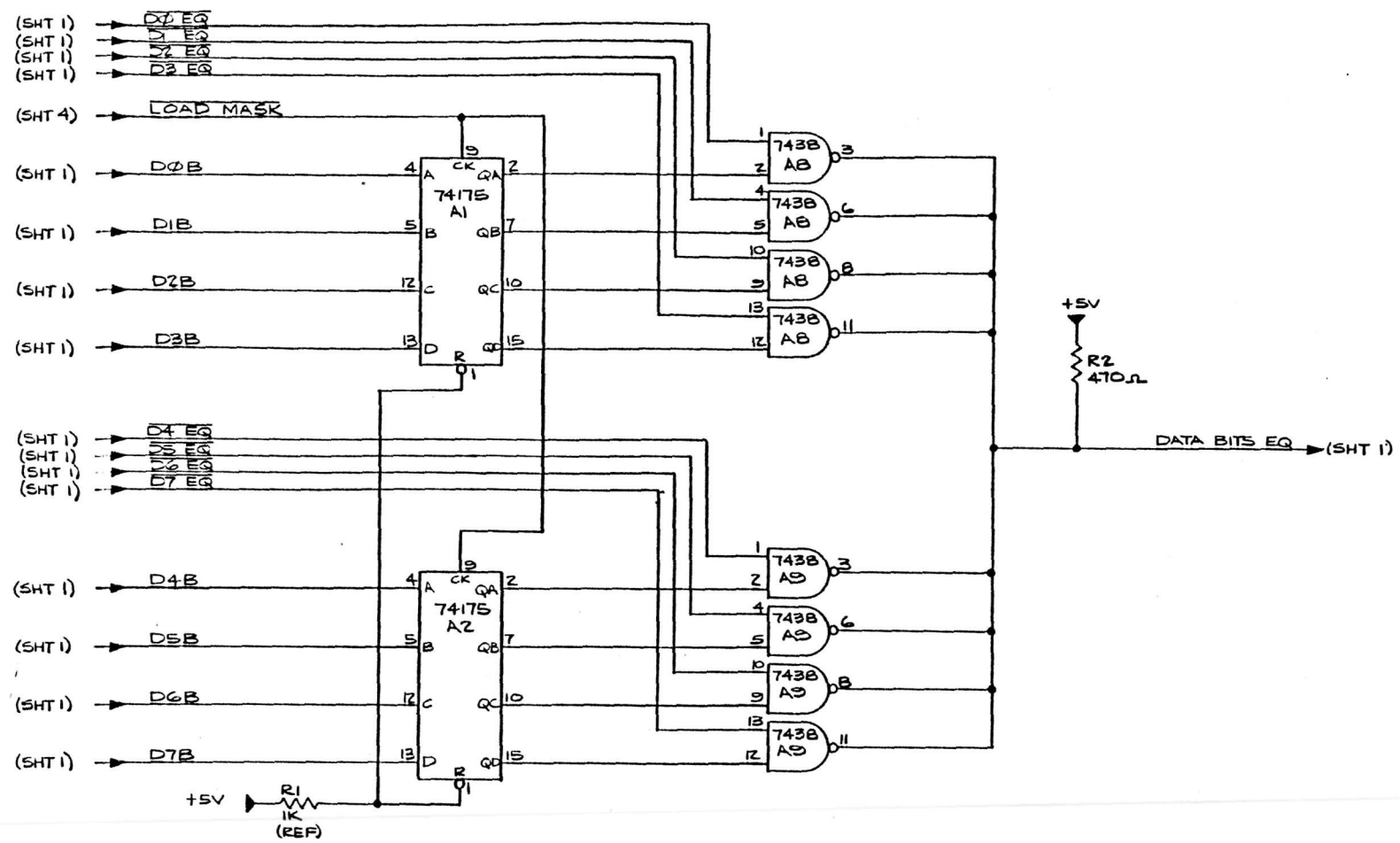


BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES	
3	2	2	2
CONFIDENTIAL			
This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. The part of this document may be copied, reprinted or disclosed to third parties without the prior written consent of Zilog Incorporated.			
APPROVALS	DATE		
DESIGN	7-2-76		
CHECKED		SCALE	SIZE
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		DRAWING NO.	DZ-0003-02
		[DO NOT SCALE DRAW]	
		SHEET 4 OF 5	

8. SHOP DRAWINGS ACCEPTED UNDER NO. 4478

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE SHT. 1	5.1.79	RED <i>[Signature]</i>

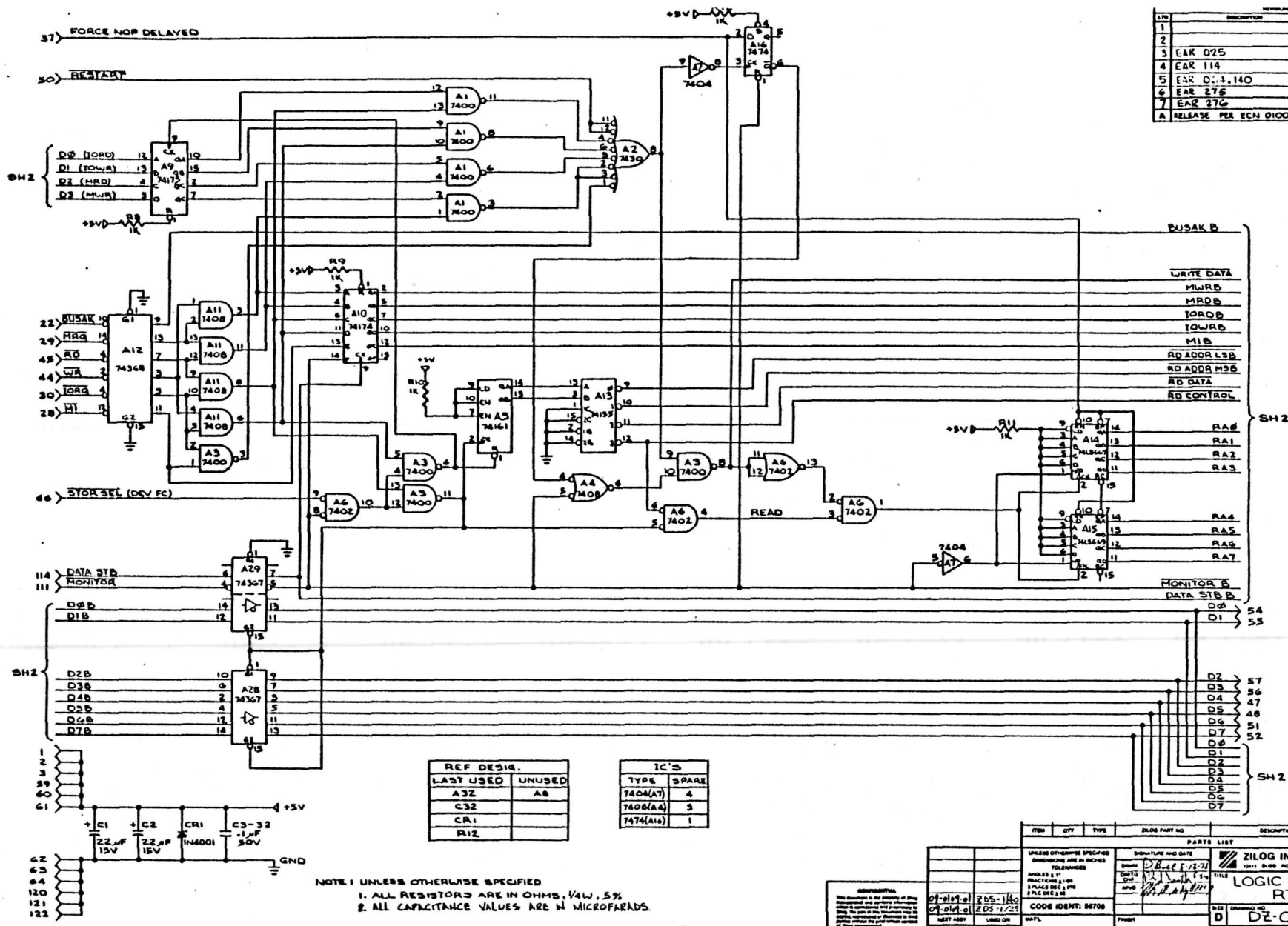


BREAKPOINT REV. D

TOLERANCES UNLESS OTHERWISE SPECIFIED		FRACTIONS DEC ANGLES				CONFIDENTIAL	
APPROVALS		DATE				This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated.	
DRAWN	Malle	4-13-76		SCALE	NONE	SIZE	C
CHECKED	Jc Healer	4/13/78		DRAWING NO.	DZ-0003-02		
	JCH	7/19/77		DO NOT SCALE DRAWING	SHEET 5 OF 5		

LOGIC DIAGRAMS, RTSM2

REV	DESCRIPTION	DATE	APPROVED
1			
2			
3	EAR 025	4-1-78	WJ
4	EAR 114	3-1-78	WJ
5	EAR 014, 140	3-1-78	WJ
6	EAR 275	10-16-78	WJ
7	EAR 276	10-16-78	WJ
A	RELEASE PER ECN 01006	4-1-79	WJ

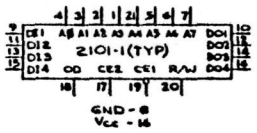
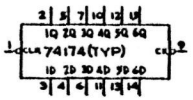
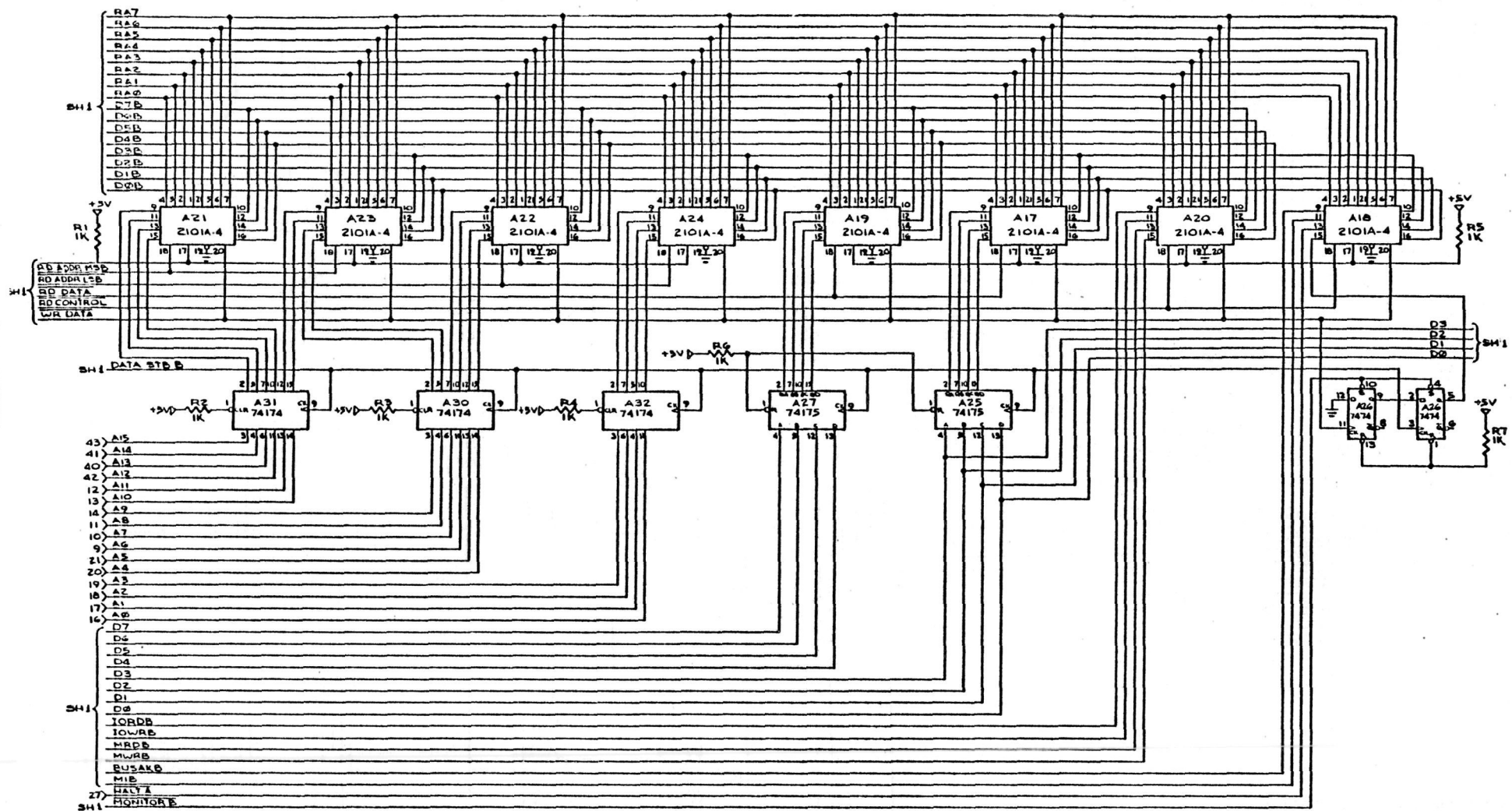


REF DESIG.		IC'S	
LAST USED	UNUSED	TYPE	SPARE
A32	A8	7404(A7)	4
C32		7408(A4)	3
CR1		7474(A14)	1
R12			

NOTE: UNLESS OTHERWISE SPECIFIED  
 1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REV DES
PARTS LIST					
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES					
TOLERANCES					
ANGLES 1:1					
FRACTIONS 1/16					
SPACE DECIMALS					
ZPL DECIMALS					
CODE IDENT: 94708					
SIGNATURE AND DATE					
DESIGNED BY: DZ-1140					
CHECKED BY: DZ-1140					
DATE: 10-16-78					
SCALE: 1:1					
ZILOG INC. 10411 BLOSS ROAD, CUPERTINO, CALIFORNIA 95014					
LOGIC DIAGRAM					
RTSMZ					
DRAWING NO. DZ-0109-01					
SHEET 1 OF 2					

REV	DESCRIPTION	DATE	BY
1	SEE SH. 1	4-17-71	MO



GND - 8  
Vcc - 16

ITEM	QTY	TYPE	SOLE PART NO	DESCRIPTION	REF DES
UNLESS OTHERWISE SPECIFIED					
DIMENSIONS ARE IN INCHES					
TOLERANCES					
DIMENSIONS IN PARENTHESES ARE					
DIMENSIONS IN MILLIMETERS					
MATERIALS					
FINISHES					
MOUNTING					
PACKAGING					
ELECTRICALS					
OTHER					
REVISIONS					
DATE					
BY					
CHECKED					
APPROVED					
TITLE					
DRAWN					
DESIGNED					
CODE IDENT: 88788					
PART NO: DZ-0109-01					
REV: A					
PAGE: 2 OF 2					

ZILOG INC.  
3841 BLUE BIRD CIRCLE, CALIFORNIA 95040

LOGIC DIAGRAM  
RTSM2



# DOCUMENT CHANGE NOTICE

DATE: 04-03-80

DCN NUMBER: E3-3018-03, Rev. C

PUBLICATION NUMBER: 03-3018-03

TITLE: ZDS-1/40 Hardware Reference Manual

PREVIOUS DCNs BY NUMBER: E3-3018-03, Rev.A  
E3-3018-03, Rev.B

EFFECTIVE DATE: 04-03-80

This Document Change Notice provides replacement pages for the publication specified above. These replacement pages contain changes to the technical contents of the manual specified above, and will remain in effect unless specifically amended or superseded by another DCN, or merged into the manual by a publication revision. The following pages are to be treated as described.

Replace Logic Diagram Set DZ-0056-02, Rev. D  
with DZ-0056-03, Rev. A.

Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of manual to provide a record of changes.



# DOCUMENT CHANGE NOTICE

DATE: 2/1/80

DCN NUMBER: E3-3018-03, Rev. B

PUBLICATION NUMBER: 03-3018-03

TITLE: ZDS-1/40 Hardware Reference Manual

PREVIOUS DCNs BY NUMBER: E3-3018-03, Rev. A

EFFECTIVE DATE: 2/1/80

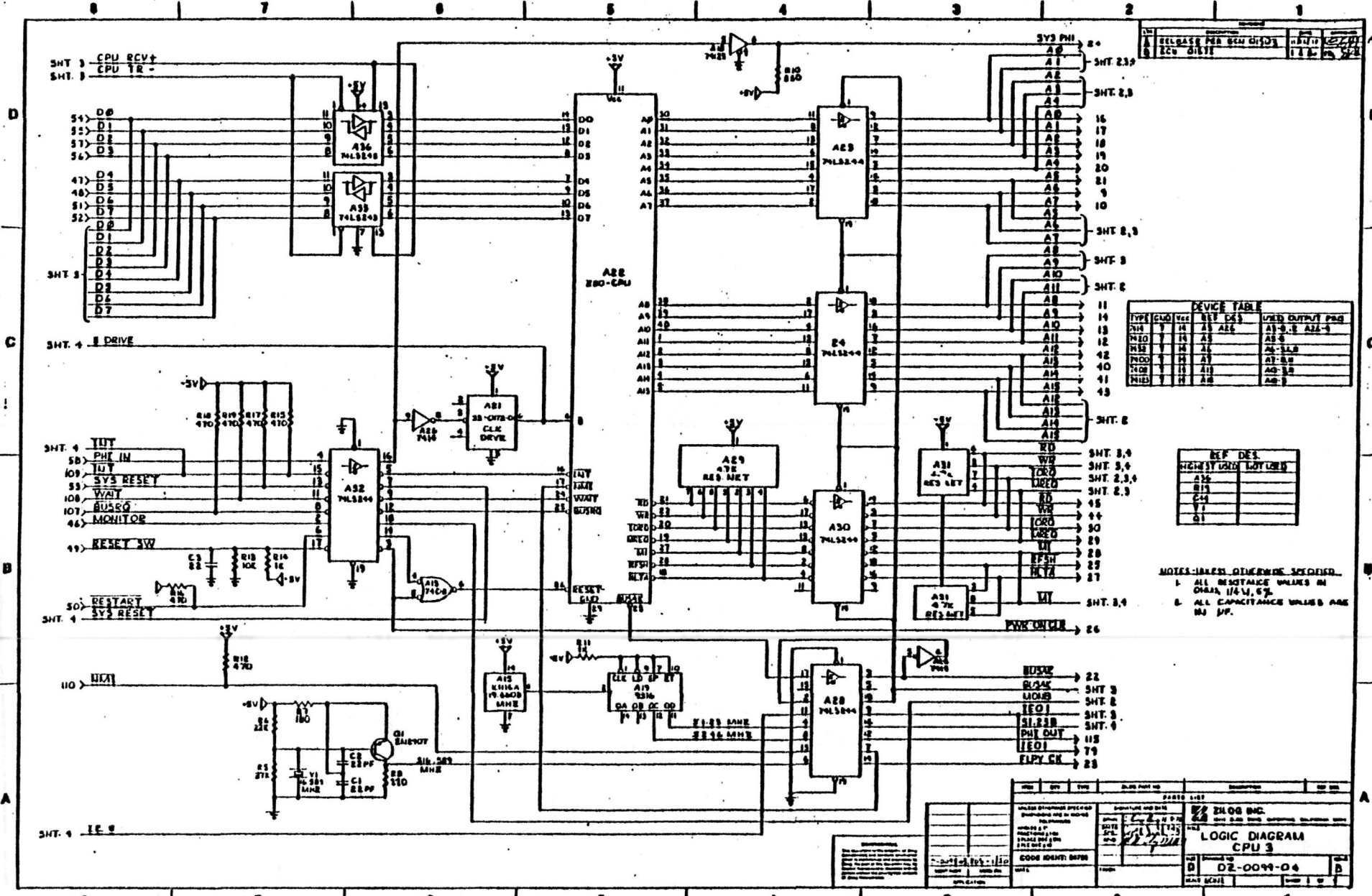
This Document Change Notice provides change pages for the publication specified above. These change pages contain changes to the technical contents of the manual specified above, and will remain in effect unless specifically amended or superseded by another DCN, or merged into the manual by a publication revision. The following pages are to be treated as described.

Replace Logic Diagram Set DZ-0099-04, Rev. A  
with DZ-0099-04, Rev. B

Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of the manual to provide a record of changes.





REV	DATE	BY	CHKD
1	11/11/67	JTB	WJ

TYPE	QTY	REF DES	USED	OUTPUT	PKG
74LS00	14	A36		A1-A15	A36-1
74LS00	14	A39		A1-A15	A39-1
74LS00	14	A32		A1-A15	A32-1
74LS00	14	A29		A1-A15	A29-1
74LS00	14	A30		A1-A15	A30-1
74LS00	14	A31		A1-A15	A31-1
74LS00	14	A28		A1-A15	A28-1

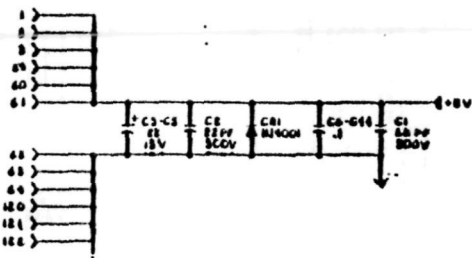
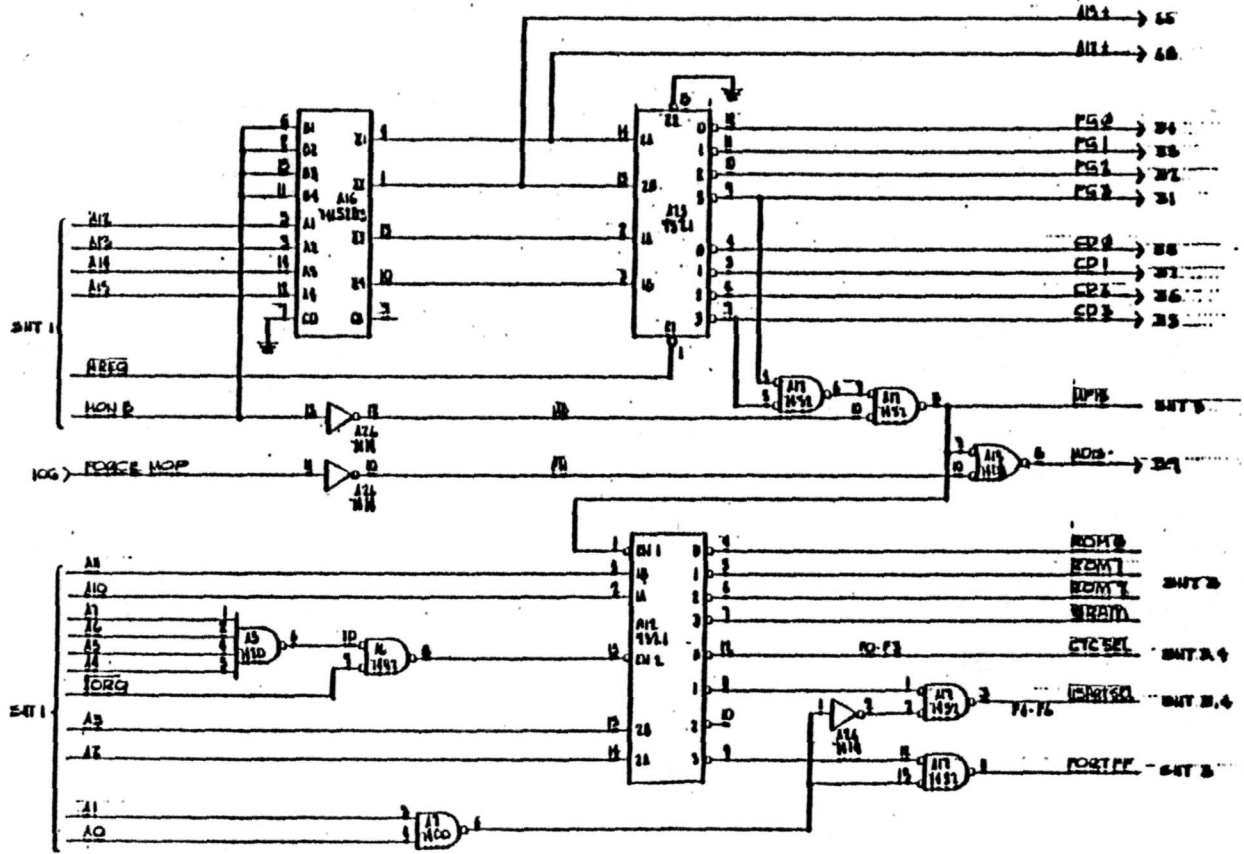
REF DES	QTY	DESCRIPTION
A36	14	74LS00
A39	14	74LS00
A32	14	74LS00
A29	14	74LS00
A30	14	74LS00
A31	14	74LS00
A28	14	74LS00

NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. ALL RESISTANCE VALUES IN OHMS, 1/4W, 5%.  
 2. ALL CAPACITANCE VALUES ARE IN  $\mu$ F.

REV	QTY	TYPE	DESCRIPTION	REF DES
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1	14	74LS00	74LS00	A39
1	14	74LS00	74LS00	A32
1	14	74LS00	74LS00	A29
1	14	74LS00	74LS00	A30
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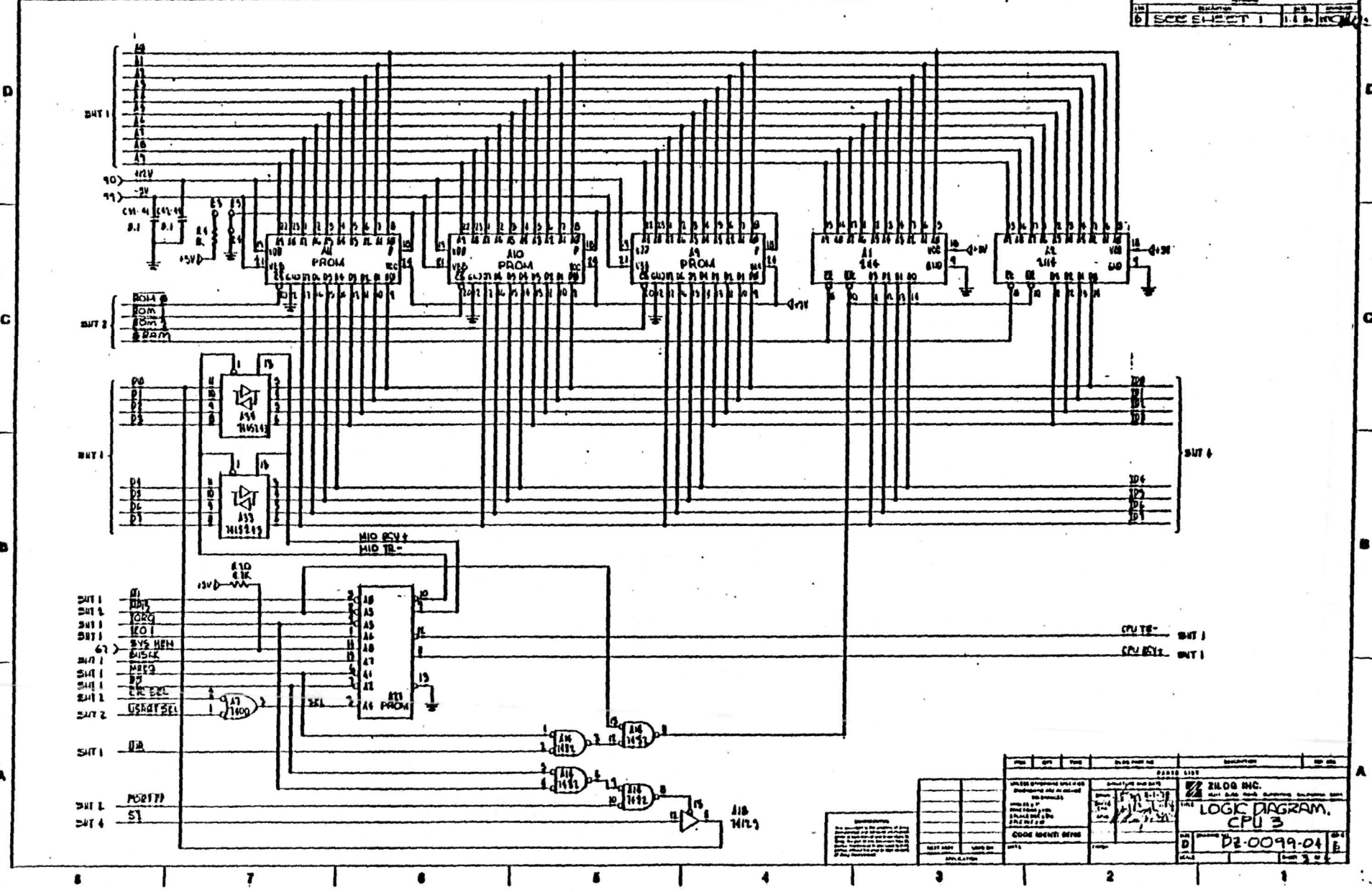
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1	14	74LS00	74LS00	A29
1	14	74LS00	74LS00	A30
1	14	74LS00	74LS00	A31
1	14	74LS00	74LS00	A28

LOGIC DIAGRAM  
 CPU 3  
 DZ-0044-04



<p>REVISIONS</p> <p>1. Initial Design</p> <p>2. Final Design</p>	<p>DATE</p> <p>11-16-74</p>	<p>DESIGNED BY</p> <p>11-16-74</p>	<p>CHECKED BY</p> <p>11-16-74</p>	<p>APPROVED BY</p> <p>11-16-74</p>	<p>REVISIONS</p> <p>1. Initial Design</p> <p>2. Final Design</p>	<p>DATE</p> <p>11-16-74</p>	<p>DESIGNED BY</p> <p>11-16-74</p>	<p>CHECKED BY</p> <p>11-16-74</p>	<p>APPROVED BY</p> <p>11-16-74</p>	<p>REVISIONS</p> <p>1. Initial Design</p> <p>2. Final Design</p>	<p>DATE</p> <p>11-16-74</p>	<p>DESIGNED BY</p> <p>11-16-74</p>	<p>CHECKED BY</p> <p>11-16-74</p>	<p>APPROVED BY</p> <p>11-16-74</p>
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**LOGIC DIAGRAM, CPU 3**  
 P2-0079-01



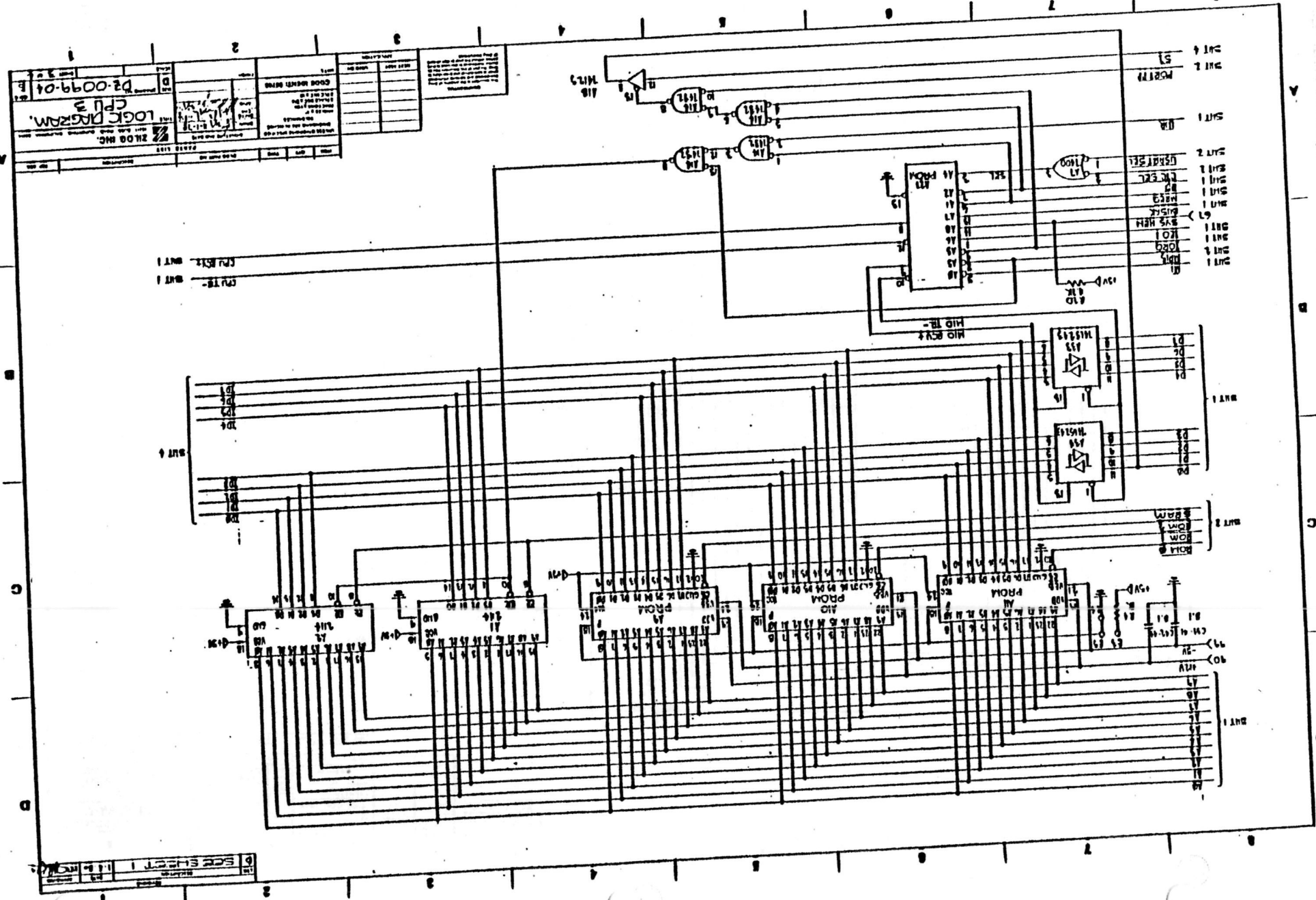
REV	DATE	DESCRIPTION	BY
D	1.1.80	SCHEMATIC 1	TRC/ML

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED	DATE: 1.1.80 TIME: 11:14 DRAWN BY: TRC/ML CHECKED BY: TRC/ML TITLE: LOGIC DIAGRAM, CPU 3	<b>ZILOG INC.</b> 2800 ZILOG DRIVE FOLSOM, CALIF. 95630 (916) 438-2000
---	--	---

PROJECT: 0099-01 DRAWING NO: 0099-01-01 SHEET NO: 1 OF 1	TITLE: LOGIC DIAGRAM, CPU 3 DATE: 1.1.80 TIME: 11:14 DRAWN BY: TRC/ML CHECKED BY: TRC/ML
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<b>LOGIC DIAGRAM</b> CPU 3 D2-0099-04		<b>GOOD WORKS SHEET</b> DATE: _____ BY: _____ CHECKED: _____ APPROVED: _____
<b>REVISIONS</b> NO. 1 DATE: _____ BY: _____	<b>DESCRIPTION</b> _____ _____ _____	<b>APPROVED</b> _____ _____



# DOCUMENT CHANGE NOTICE

DATE: 12-07-79

DCN NUMBER: E3-3018-03, Rev. A

PUBLICATION NUMBER: 03-3018-03

TITLE: ZDS-1/40 HARDWARE REFERENCE MANUAL

PREVIOUS DCN's BY NUMBER: None

EFFECTIVE DATE: 12-07-79

This Document Change Notice provides change pages for the publication specified above. These change pages contain changes to the technical contents of the manual specified above, and will remain in effect unless specifically amended or superseded by another DCN, or merged into the manual by a publication revision. The following pages are to be treated as described.

Replace page D-22 in manual with change page attached.

Replace CONTENTS page of APPENDIX E with change page attached.

Replace page E-33 in manual with change page attached.

Replace Logic Diagram Set DZ-0099-03, Rev. A with DZ-0099-04, Rev. A

Changes to text are indicated by a vertical line in the right margin, opposite the changed text portion.

NOTE: Please file this DCN at the back of the manual to provide a record of changes.

PINOUT FOR 60K MEMORY BOARD - 09-0101-04 (cont.)  
J08

PIN #	SIGNAL NAME
093	+12V.2
094	+12V.2
095	+12V.2
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	.
110	.
111	.
112	.
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.PRINTED.DISTRIBUTION)
121	(GND.PRINTED.DISTRIBUTION)
122	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR CPU BOARD - 09-0099-01 or 09-0099-04  
J09

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	RCVR.OUT-
005	(SERIAL.OUT)
006	RCV.CLK
007	RCV.CLK.(XMIT.CLK)
008	SERIAL.IN
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	SERIAL.OUT
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	BUSAK-
023	8.PHI.(8X.SYSTEM.CLOCK)
024	PHI.(SYSTEM.CLOCK)
025	REFRESH-
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	CD.3-
036	CD.2-
037	CD.1-
038	CD.0-
039	PG.15-.(MDIS-)
040	A13
041	A14
042	A12
043	A15
044	WR-
045	RD-
046	TY.HI.(MONITOR)

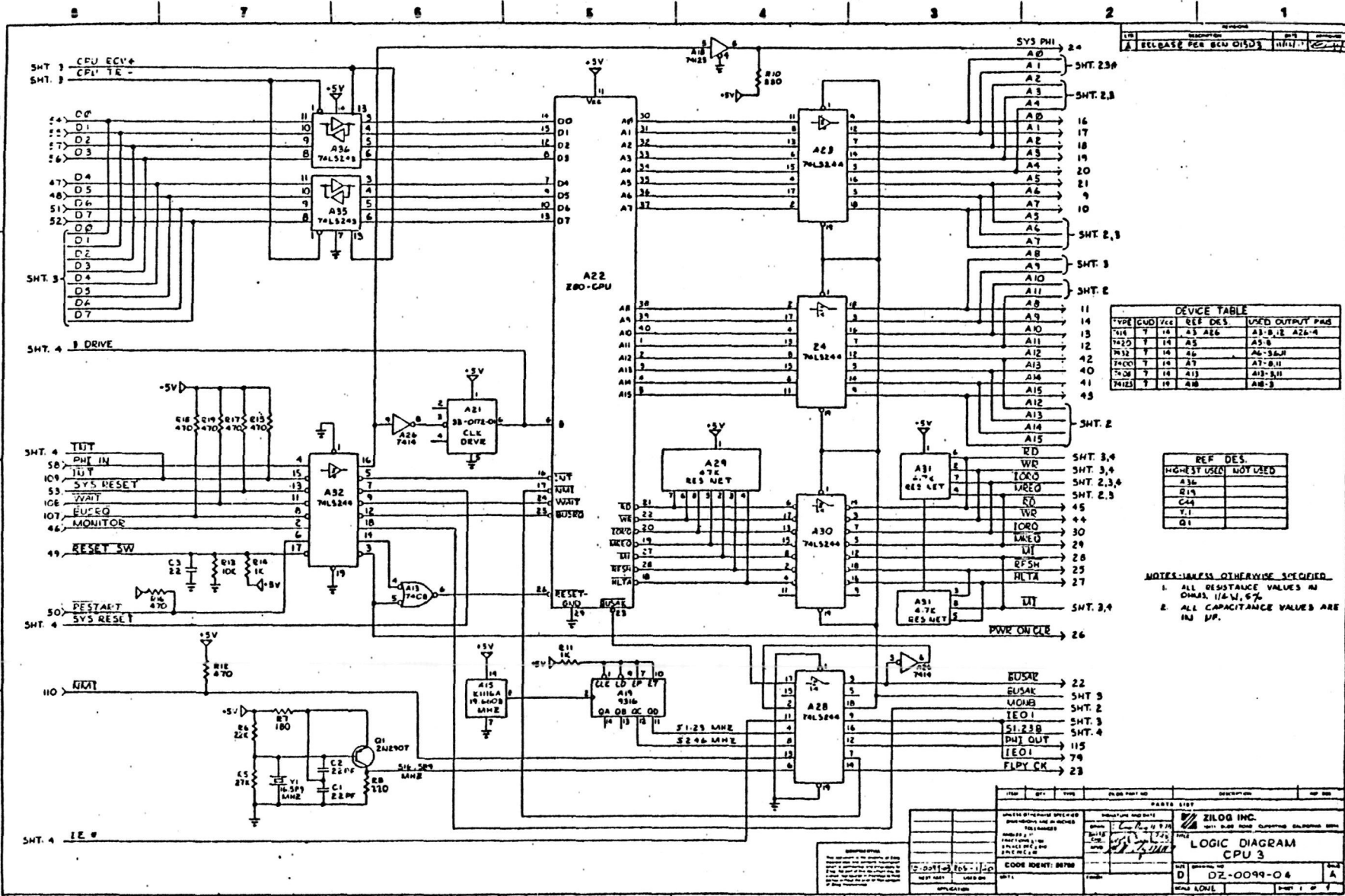
APPENDIX E  
LOGIC DIAGRAMS





## CONTENTS

LOGIC DIAGRAMS, USER POD CONTROLLER . . . . .	E-1
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LOGIC DIAGRAMS, BREAKPOINT . . . . .	E-49
LOGIC DIAGRAMS, RTSM.2 . . . . .	E-57



LIB	DESCRIPTION	QTY	REVISION
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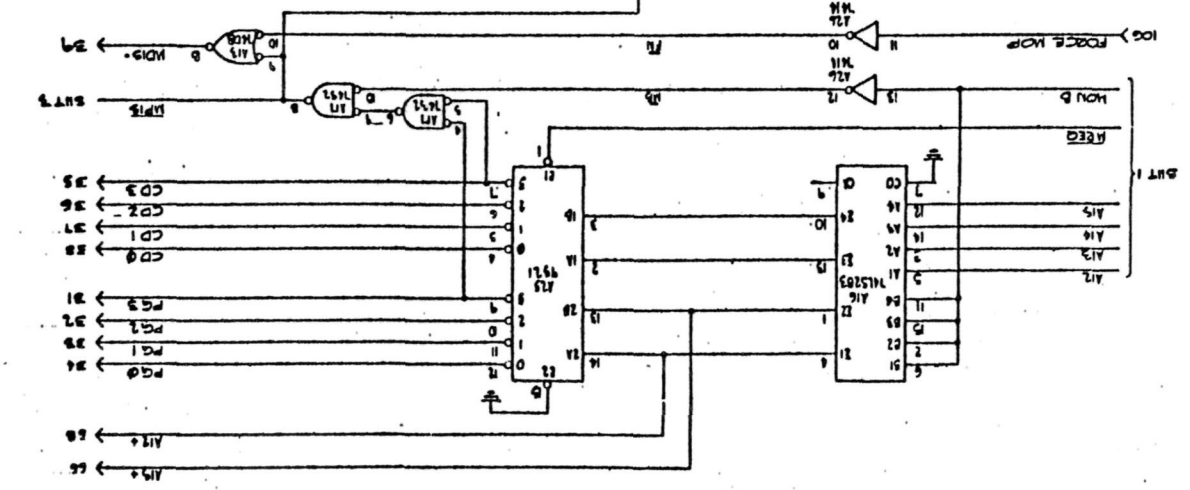
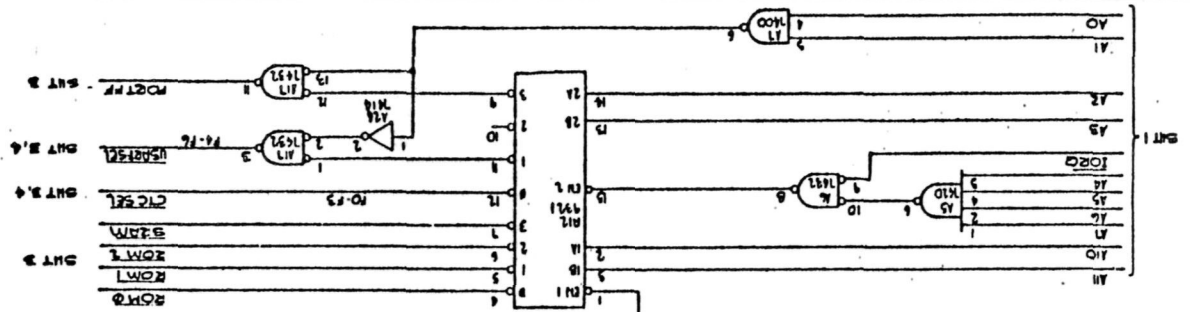
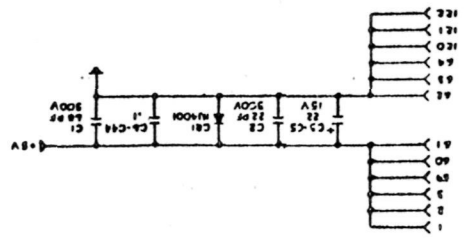
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7412	1	14	A5	A3, B
7412	1	14	A6	A4-B, A, H
7400	1	14	A7	A7-B, H
7408	1	14	A13	A13-B, H
74123	1	14	A8	A8-B

HIGHEST USED	NOT USED
A36	
A19	
C41	
T.1	
Q1	

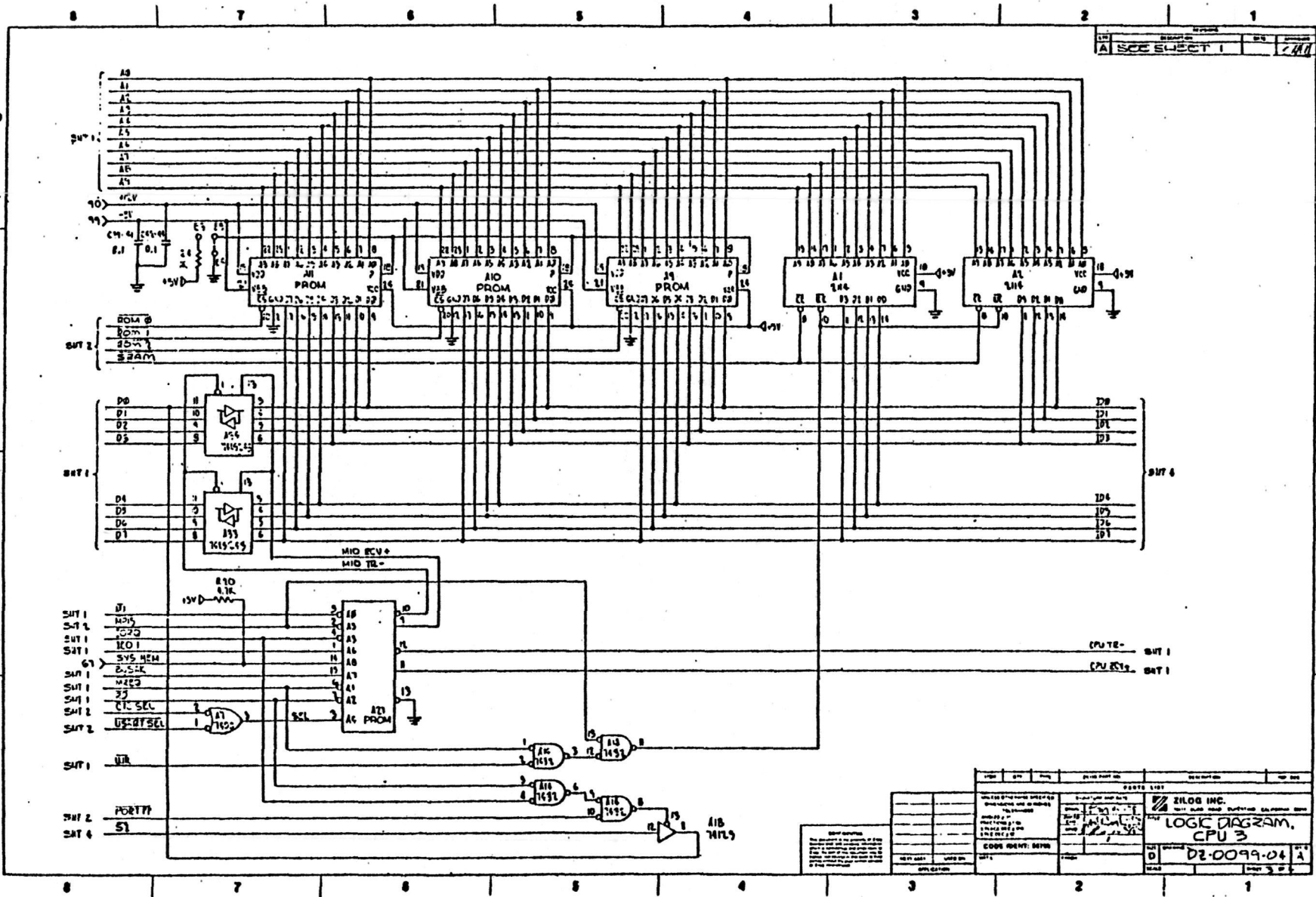
NOTES: UNLESS OTHERWISE SPECIFIED:  
 1. ALL RESISTANCE VALUES IN OHMS, 1% TOL.  
 2. ALL CAPACITANCE VALUES ARE IN PF.

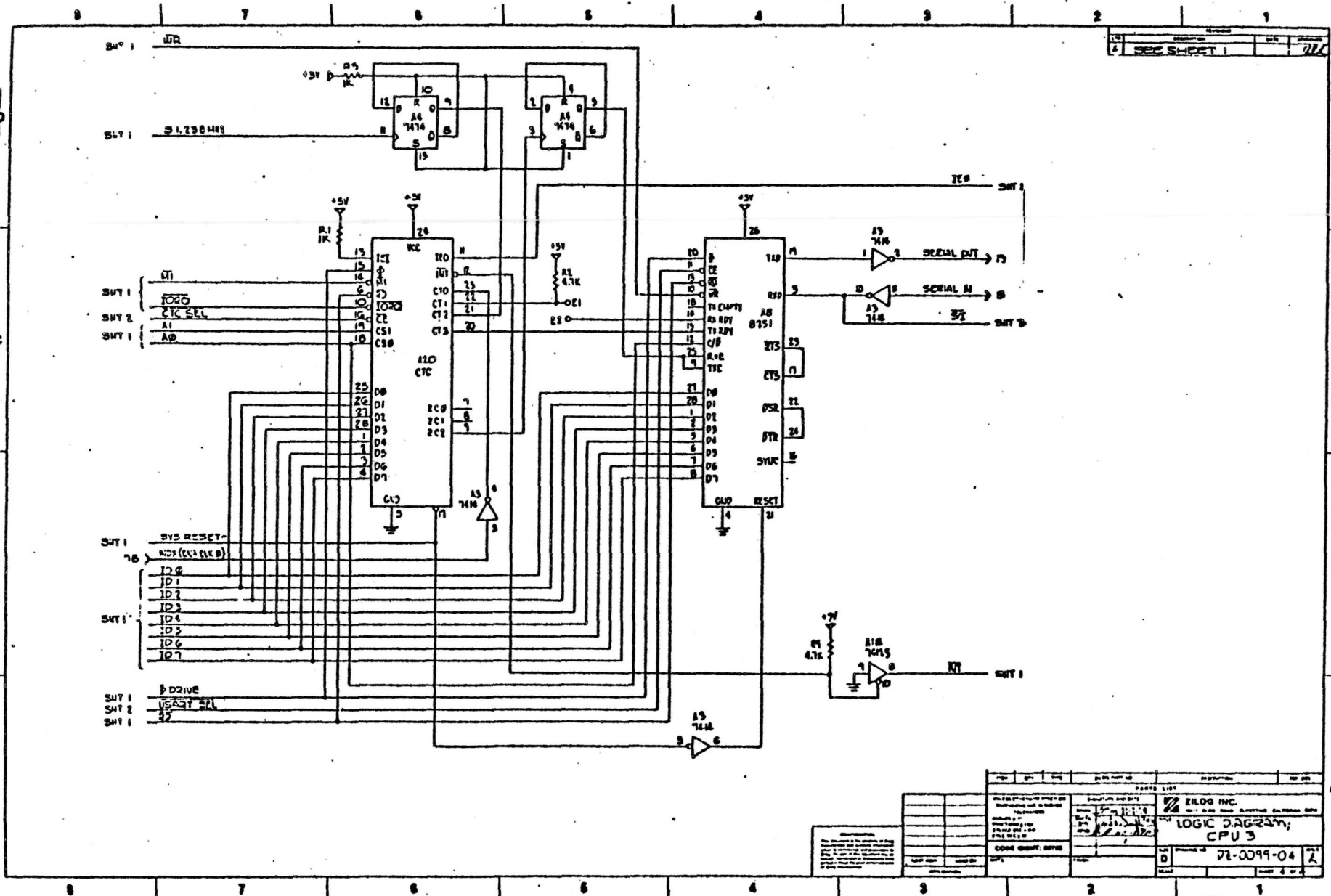
ITEM	QTY	TYPE	MANUFACTURE AND DATE	DESCRIPTION	REF DES
PARTS LIST					
ZILOG INC. LOGIC DIAGRAM CPU 3 DZ-0099-04					

<b>LOGIC DIAGRAM</b> <b>CPU 3</b> 02-0094-001	
ZILCO INC. 1100 S. 10th Street Lincoln, Nebraska 68502	DATE: 11/19/71 DRAWN BY: J. J. ... CHECKED BY: ... APPROVED BY: ...
CODE DEPT: 3010 PART NO: ... REV: ...	TITLE: ... PART NO: ... REV: ...



SEE SHEET 1





REV	DATE	BY	CHKD	DESCRIPTION

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PROJECT: 72-0099-04 SHEET: 4 OF 4 TITLE: LOGIC DIAGRAM, CPU 3		DATE: 12/11/72 BY: [Signature] CHKD: [Signature]